NEC

MOS FIELD EFFECT TRANSISTOR
2SK3224

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3224	TO-251
2SK3224-Z	TO-252

FEATURES

- Low On-State Resistance
  $R_{DS(on)1}$ = 40 mΩ MAX. (V_{GS} = 10 V, I_D = 10 A)
  $R_{DS(on)2}$ = 60 mΩ MAX. (V_{GS} = 4.0 V, I_D = 10 A)
- Low C_{iss} : C_{iss} = 790 pF TYP.
- Built-in Gate Protection Diode
- TO-251/TO-252 package

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	$V_{GSS(AC)}$	±20	V
Gate to Source Voltage	$V_{GSS(DC)}$	+20, –10	V
Drain Current (DC)	$I_{D(DC)}$	±20	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±70	A
Total Power Dissipation (T_C = 25°C)	P_T	25	W
Total Power Dissipation (T_A = 25°C)	P_T	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	10	A
Single Avalanche Energy Note2	E_{AS}	10	mJ

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1 %

2. Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0 V

THERMAL RESISTANCE

Channel to Case	$R_{th(ch-C)}$	5.0	°C/W
Channel to Ambient	$R_{th(ch-A)}$	125	°C/W

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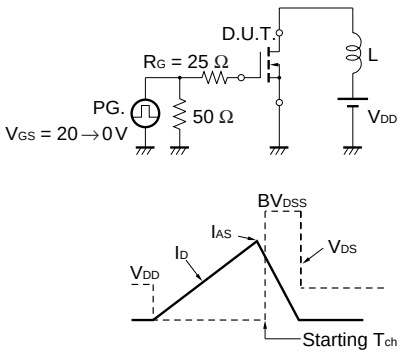
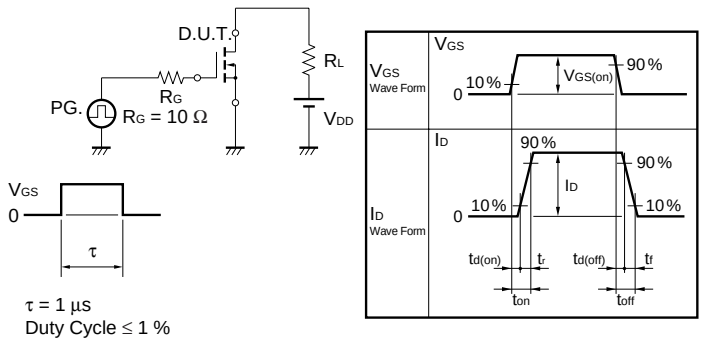
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 10 A		24	40	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.0 V, I_D = 10 A		33	60	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 10 A	8.0	15		S
Drain Leakage Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V		790		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		240		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		100		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 10 A		19		ns
Rise Time	t_r	$V_{GS(on)}$ = 10 V		165		ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = 30 V		62		ns
Fall Time	t_f	R_G = 10 Ω		71		ns
Total Gate Charge	Q_G	I_D = 20 A		20		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 48 V		3		nC
Gate to Drain Charge	Q_{GD}	$V_{GS(on)}$ = 10 V		6.5		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 20 A, V_{GS} = 0 V		0.93		V
Reverse Recovery Time	t_{rr}	If = 20 A, V_{GS} = 0 V		40		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		45		nC

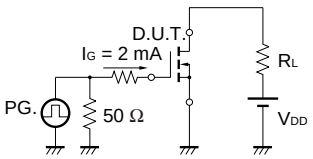
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

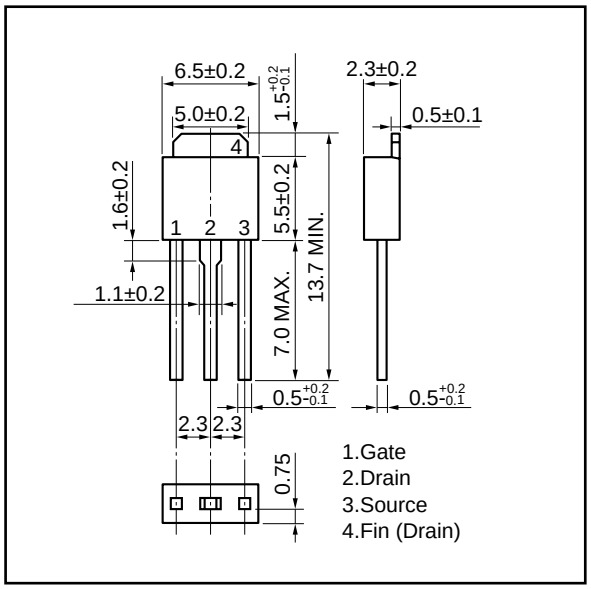


TEST CIRCUIT 3 GATE CHARGE

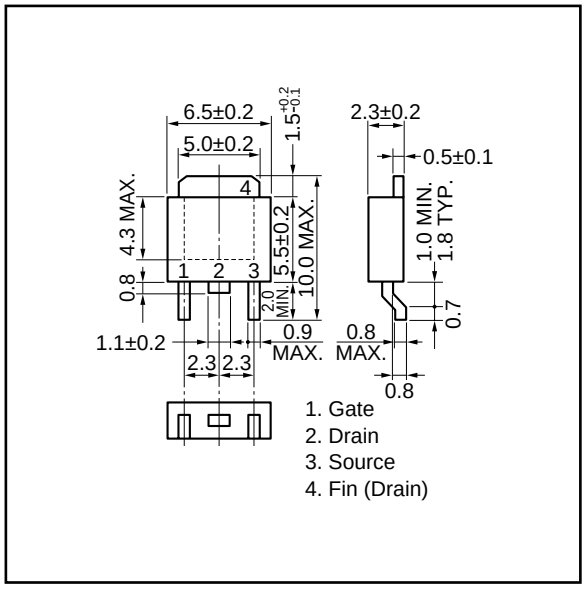


PACKAGE DRAWINGS (Unit : mm)

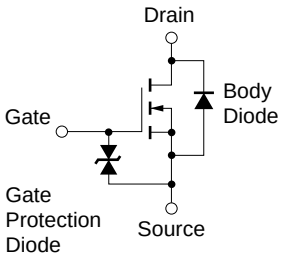
1) TO-251 (MP-3)



2) TO-252 (MP-3Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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