74ABT544

Octal latched transceiver with dual enable; inverting; 3-state

Rev. 03 — 20 April 2005 Product data sheet

1. General description

The 74ABT544 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT544 octal latched transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable ($\overline{LEAB}$ and $\overline{LEBA}$) and output enable ($\overline{OEAB}$ and $\overline{OEBA}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64 mA.

The 74ABT544 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B enable ($\overline{EAB}$) input and the A-to-B latch enable ($\overline{LEAB}$) input are LOW, the A-to-B path is transparent. A subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and invert the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

2. Features

- Combines 74ABT640 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64 mA and –32 mA
- Live insertion and extraction permitted
- Power-up 3-state
- Power-up reset
- Latch-up protection:
  - JESD78: exceeds 500 mA
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - Machine model: exceeds 200 V

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3. Quick reference data

Table 1: Quick reference data

T_{amb} = 25 °C; GND = 0 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay An to Bn or Bn to An	C_L = 50 pF; V_{CC} = 5 V	-	3.0	-	ns
t_{PHL}	propagation delay An to Bn or Bn to An	C_L = 50 pF; V_{CC} = 5 V	-	3.6	-	ns
C_I	input capacitance	V_I = 0 V or V_{CC}	-	4	-	pF
$C_{I/O}$	I/O capacitance	outputs disabled; V_O = 0 V or V_{CC}	-	7	-	pF
I_{CC}	quiescent supply current	outputs 3-state; V_{CC} = 5.5 V	-	110	-	µA

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT544D	–40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74ABT544N	–40 °C to +85 °C	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222-1
74ABT544DB	–40 °C to +85 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74ABT544PW	–40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

5. Functional diagram

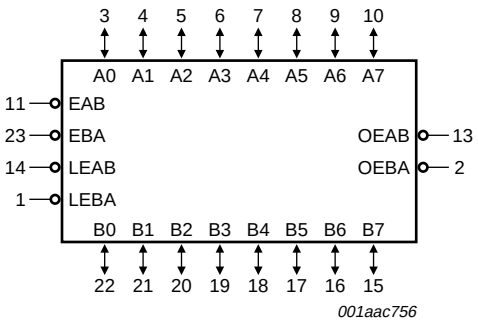

Fig 1. Logic symbol

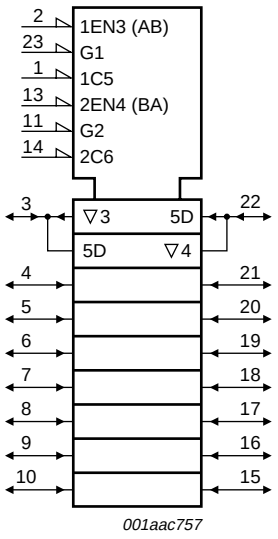

Fig 2. IEC logic symbol

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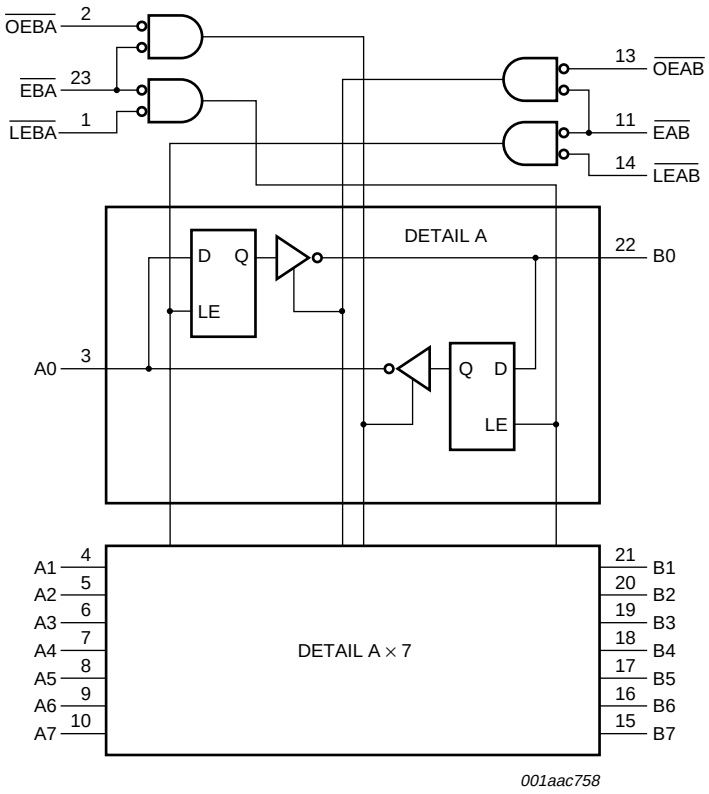

Fig 3. Logic diagram

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6. Pinning information

6.1 Pinning

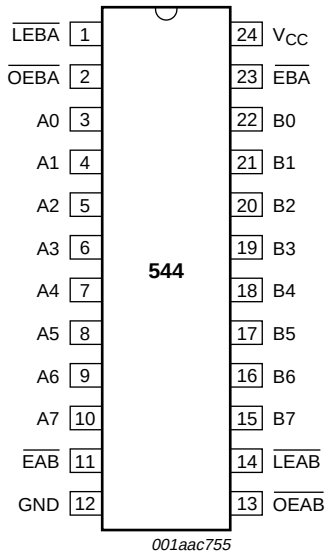

Fig 4. Pin configuration

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
$\overline{LEBA}$	1	B-to-A latch enable input (active LOW)
$\overline{OEBA}$	2	B-to-A output enable input (active LOW)
A0	3	port A, 3-state output 0
A1	4	port A, 3-state output 1
A2	5	port A, 3-state output 2
A3	6	port A, 3-state output 3
A4	7	port A, 3-state output 4
A5	8	port A, 3-state output 5
A6	9	port A, 3-state output 6
A7	10	port A, 3-state output 7
$\overline{EAB}$	11	A-to-B enable input (active LOW)
GND	12	ground (0 V)
$\overline{OEAB}$	13	A-to-B output enable input (active LOW)
$\overline{LEAB}$	14	A-to-B latch enable input (active LOW)
B7	15	port B, 3-state output 7
B6	16	port B, 3-state output 6
B5	17	port B, 3-state output 5
B4	18	port B, 3-state output 4

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Table 3: Pin description *...continued*

Symbol	Pin	Description
B3	19	port B, 3-state output 3
B2	20	port B, 3-state output 2
B1	21	port B, 3-state output 1
B0	22	port B, 3-state output 0
$\overline{EBA}$	23	B-to-A enable input (active LOW)
V_{CC}	24	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1]

Status	Control			Input	Output
	$\overline{OExx}$	$\overline{Exx}$	$\overline{LExx}$	An or Bn	An or Bn
Disabled	H	X	X	X	Z
	X	H	X	X	Z
Disabled + latch	L	↑	L	h	Z
				l	Z
Latch + display	L	L	↑	h	L
				l	H
Transparent	L	L	L	H	L
				L	H
Hold	L	L	H	X	NC

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care;
↑ = LOW-to-HIGH clock transition;
NC = no change;
Z = high-impedance OFF-state.

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8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage		[1]	–1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	–0.5	+5.5	V
I_{IK}	input diode current	$V_I < 0$ V		-	–18	mA
I_{OK}	output diode current	$V_O < 0$ V		-	–50	mA
I_O	output current	output in LOW-state		-	128	mA
T_j	junction temperature		[2]	-	150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level Input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	–32	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise or fall rate		0	-	10	ns/V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C

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10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
V_{IK}	input diode voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		-	–0.9	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}					
		I_{OH} = –3 mA		2.5	3.2	-	V
		I_{OH} = –32 mA		2.0	2.3	-	V
		V_{CC} = 5.0 V; V_I = V_{IL} or V_{IH}					
		I_{OH} = –3 mA		3.0	3.7	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}		-	0.42	0.55	V
V_{RST}	restart LOW-level output voltage	V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}	[1]	-	0.13	0.55	V
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V					
	control pins			-	±0.01	±1.0	µA
	data pins			-	±5	±100	µA
I_{OFF}	power-down leakage current	V_{CC} = 0 V; V_I or V_O ≤ 4.5 V		-	±5.0	±100	µA
I_{PU}, I_{PD}	power-up or power-down 3-state output current	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; V_{OEXX} = don't care	[2]	-	±5.0	±50	µA
I_{OZ}	3-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}					
		output HIGH-state at V_O = 2.7 V		-	5.0	50	µA
		output LOW-state at V_O = 0.5 V		-	–5.0	–50	µA
I_{CEX}	output HIGH-state leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}		-	5.0	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[3]	–50	–65	–180	mA
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}					
		outputs HIGH-state		-	110	250	µA
		outputs LOW-state		-	20	30	mA
		outputs 3-state		-	110	250	µA
ΔI_{CC}	additional supply current per input pin	V_{CC} = 5.5 V; one input at 3.4 V and other inputs at V_{CC} or GND; V_{CC} = 5.5 V	[4]	-	0.3	1.5	mA
C_I	input capacitance	V_I = 0 V or V_{CC}		-	4	-	pF
$C_{I/O}$	I/O capacitance	outputs disabled; V_O = 0 V or V_{CC}		-	7	-	pF
T_{amb} = –40 °C to +85 °C							
V_{IK}	input diode voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		-	-	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}					
		I_{OH} = –3 mA		2.5	-	-	V
		I_{OH} = –32 mA		2.0	-	-	V
		V_{CC} = 5.0 V; V_I = V_{IL} or V_{IH}					
		I_{OH} = –3 mA		3.0	-	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}		-	-	0.55	V
V_{RST}	restart LOW-level output voltage	V_{CC} = 5.5 V; I_O = 1 mA; V_I = GND or V_{CC}	[1]	-	-	0.55	V

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Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V					
	control pins			-	-	±1.0	µA
	data pins			-	-	±100	µA
I_{OFF}	power-down leakage current	V_{CC} = 0 V; V_I or $V_O \leq$ 4.5 V		-	-	±100	µA
I_{PU}, I_{PD}	power-up or power-down 3-state output current	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; V_{OExx} = don't care	[2]	-	-	±50	µA
I_{OZ}	3-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}					
		output HIGH-state at V_O = 2.7 V		-	-	50	µA
		output LOW-state at V_O = 0.5 V		-	-	–50	µA
I_{CEX}	output HIGH-state leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}		-	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[3]	–50	-	–180	mA
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}					
		outputs HIGH-state		-	-	250	µA
		outputs LOW-state		-	-	30	mA
		outputs 3-state		-	-	250	µA
ΔI_{CC}	additional supply current per input pin	V_{CC} = 5.5 V; one input at 3.4 V and other inputs at V_{CC} or GND; V_{CC} = 5.5 V	[4]	-	-	1.5	mA

[1] For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

[2] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 % a transition time of up to 100 µs is permitted.

[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[4] This is the increase in supply current for each input at 3.4 V.

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C; V_{CC} = 5.0 V						
t_{PLH}	propagation delay					
	An to Bn, Bn to An	see Figure 5	1.7	3.0	3.8	ns
	$\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	see Figure 5 and 6	2.1	3.5	4.2	ns
t_{PHL}	propagation delay					
	An to Bn, Bn to An	see Figure 5	2.4	3.6	4.5	ns
	$\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	see Figure 5 and 6	3.0	4.4	5.3	ns
t_{PZH}	output enable time to HIGH-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 7	1.8	3.0	3.9	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 7	1.9	3.4	4.1	ns
t_{PZL}	output enable time to LOW-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 8	2.9	4.2	5.2	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 8	3.1	4.6	5.5	ns

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Table 8: Dynamic characteristics *…continued*

GND = 0 V; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}	output disable time from HIGH-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 7	2.0	3.3	4.3	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 7	2.1	3.4	4.5	ns
t_{PLZ}	output disable time from LOW-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 8	2.0	2.8	5.8	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 8	2.0	3.0	6.2	ns
$t_{su(H)}$	set-up time HIGH					
	An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	see Figure 9	3.0	1.5	-	ns
	An to $\overline{EAB}$, Bn to $\overline{EBA}$	see Figure 9	3.0	1.5	-	ns
$t_{su(L)}$	set-up time LOW					
	An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	see Figure 9	3.0	0.6	-	ns
	An to $\overline{EAB}$, Bn to $\overline{EBA}$	see Figure 9	3.0	0.6	-	ns
$t_{h(H)}$	hold time HIGH					
	An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	see Figure 9	0.5	–0.3	-	ns
	An to $\overline{EAB}$, Bn to $\overline{EBA}$	see Figure 9	0.5	–0.2	-	ns
$t_{h(L)}$	hold time LOW					
	An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	see Figure 9	0.5	–1.3	-	ns
	An to $\overline{EAB}$, Bn to $\overline{EBA}$	see Figure 9	0.5	–1.3	-	ns
t_{wL}	pulse width LOW $\overline{LEAB}$ and $\overline{LEBA}$	see Figure 9	3.5	1.8	-	ns
T_{amb} = –40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V						
t_{PLH}	propagation delay					
	An to Bn, Bn to An	see Figure 5	1.7	-	4.7	ns
	$\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	see Figure 5 and 6	2.1	-	5.2	ns
t_{PHL}	propagation delay					
	An to Bn, Bn to An	see Figure 5	2.4	-	5.2	ns
	$\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	see Figure 5 and 6	3.0	-	6.2	ns
t_{PZH}	output enable time to HIGH-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 7	1.8	-	4.7	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 7	1.9	-	5.0	ns
t_{PZL}	output enable time to LOW-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 8	2.9	-	6.1	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 8	3.1	-	6.5	ns
t_{PHZ}	output disable time from HIGH-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 7	2.0	-	4.9	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 7	2.1	-	5.2	ns
t_{PLZ}	output disable time from LOW-level					
	$\overline{OEBA}$ to An, $\overline{OEAB}$ to Bn	see Figure 8	2.0	-	6.3	ns
	$\overline{EBA}$ to An, $\overline{EAB}$ to Bn	see Figure 8	2.0	-	6.7	ns

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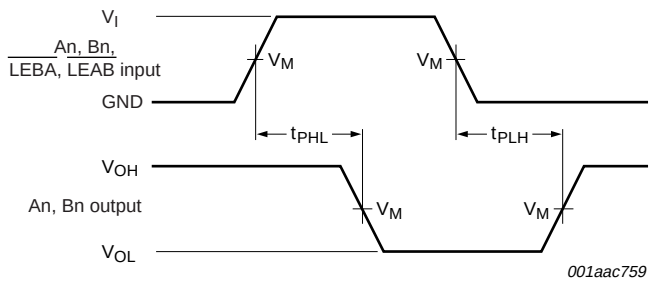
Table 8: Dynamic characteristics *…continued*

GND = 0 V; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(H)}$	set-up time HIGH					
	An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	see Figure 9	3.0	-	-	ns
	An to $\overline{EAB}$, Bn to $\overline{EBA}$	see Figure 9	3.0	-	-	ns
$t_{su(L)}$	set-up time LOW					
	An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	see Figure 9	3.0	-	-	ns
	An to $\overline{EAB}$, Bn to $\overline{EBA}$	see Figure 9	3.0	-	-	ns
$t_{h(H)}$	hold time HIGH					
	An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	see Figure 9	0.5	-	-	ns
	An to $\overline{EAB}$, Bn to $\overline{EBA}$	see Figure 9	0.5	-	-	ns
$t_{h(L)}$	hold time LOW					
	An to $\overline{LEAB}$, Bn to $\overline{LEBA}$	see Figure 9	0.5	-	-	ns
	An to $\overline{EAB}$, Bn to $\overline{EBA}$	see Figure 9	0.5	-	-	ns
t_{wL}	pulse width LOW $\overline{LEAB}$ and $\overline{LEBA}$	see Figure 9	3.5	-	-	ns

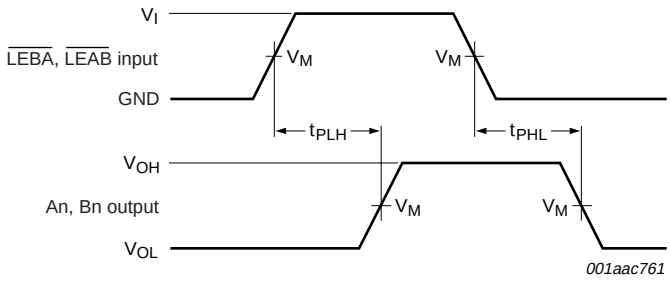
12. Waveforms



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 5. Propagation delay for inverting output



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 6. Propagation delay for non-inverting output

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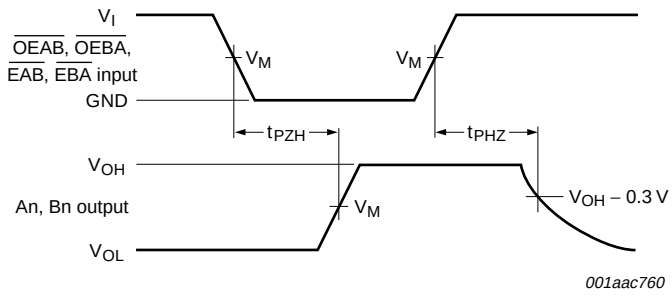
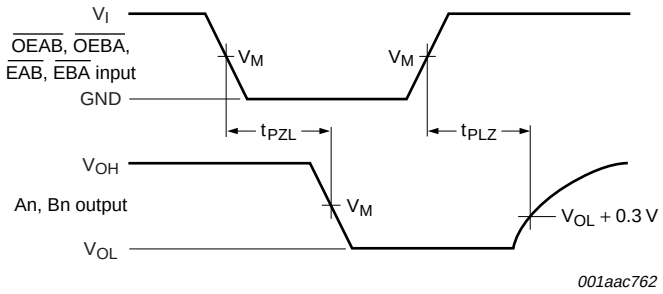


V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

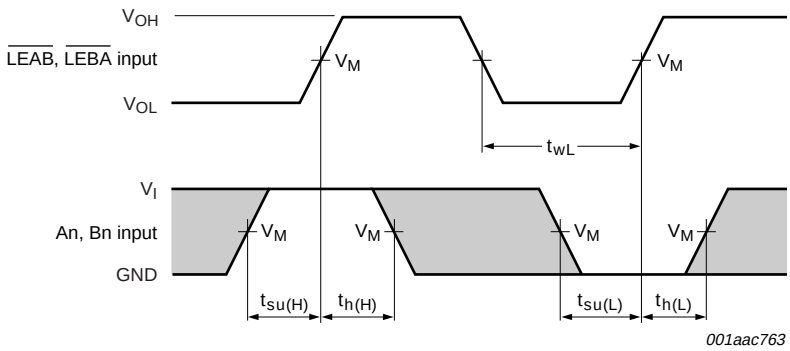
Fig 7. 3-state output enable time to HIGH-level and output disable time from HIGH-level



V_M = 1.5 V.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 8. 3-state output enable time to LOW-level and output disable time from LOW-level



V_M = 1.5 V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 9. Data set-up and hold times and latch enable pulse width

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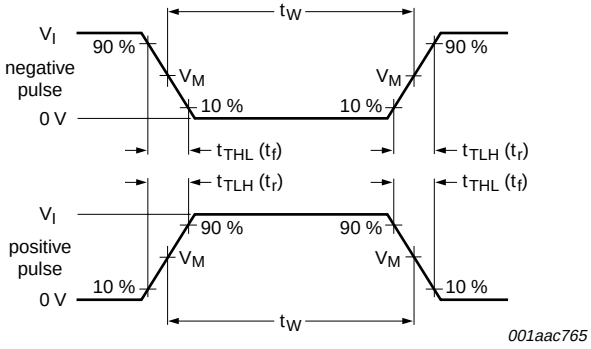
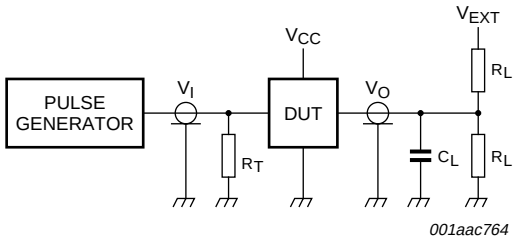
13. Test information



V_M = 1.5 V.

a. Input pulse definition



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

b. Test circuit for 3-state outputs

Fig 10. Load circuitry for switching times

Table 9: Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
3.0 V	1 MHz	500 ns	2.5 ns	50 pF	500 Ω	open	7.0 V	open

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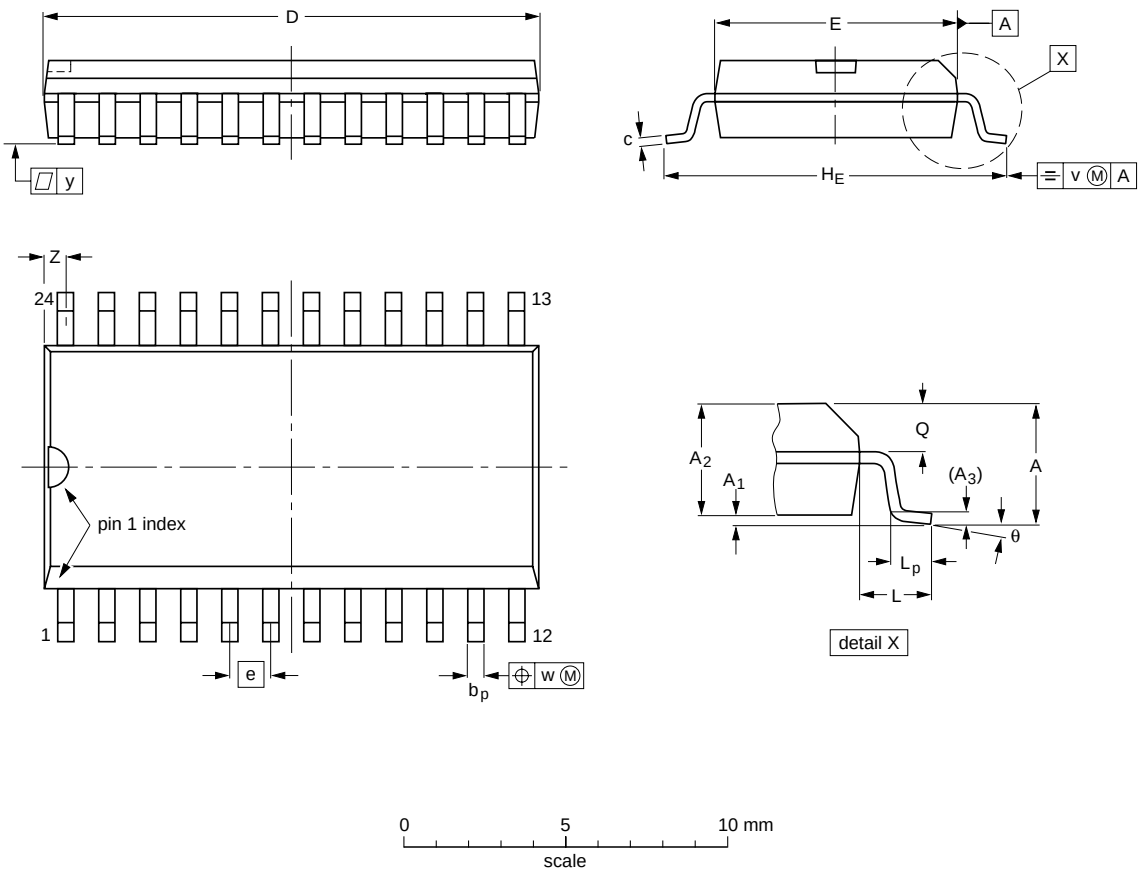
14. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT137-1 (SO24)

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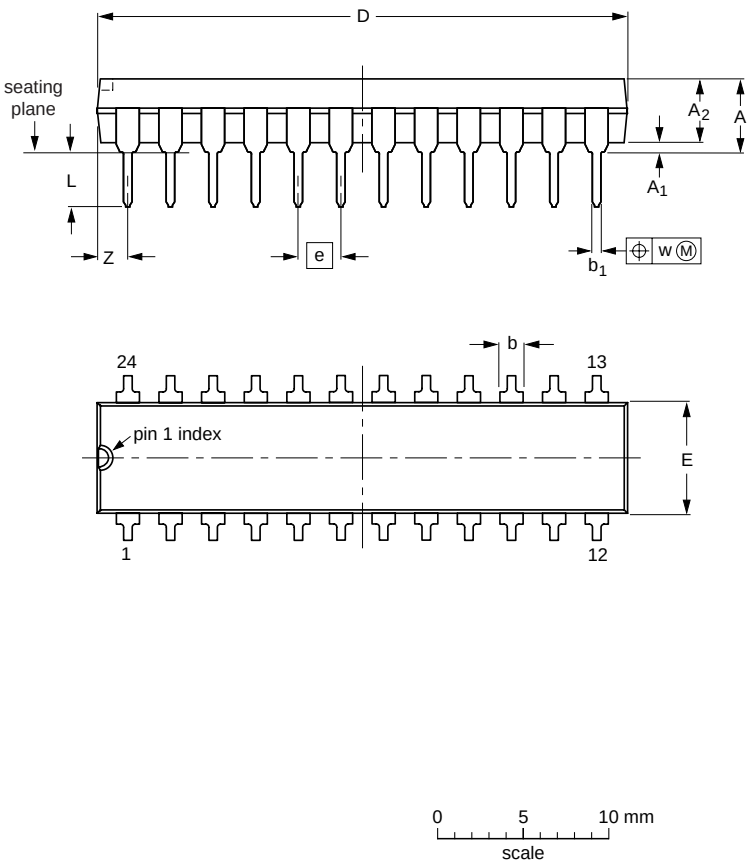
DIP24: plastic dual in-line package; 24 leads (300 mil) **SOT222-1**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.1	0.3	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT222-1		MS-001				~~99-12-27~~ 03-03-12

Fig 12. Package outline SOT222-1 (DIP24)

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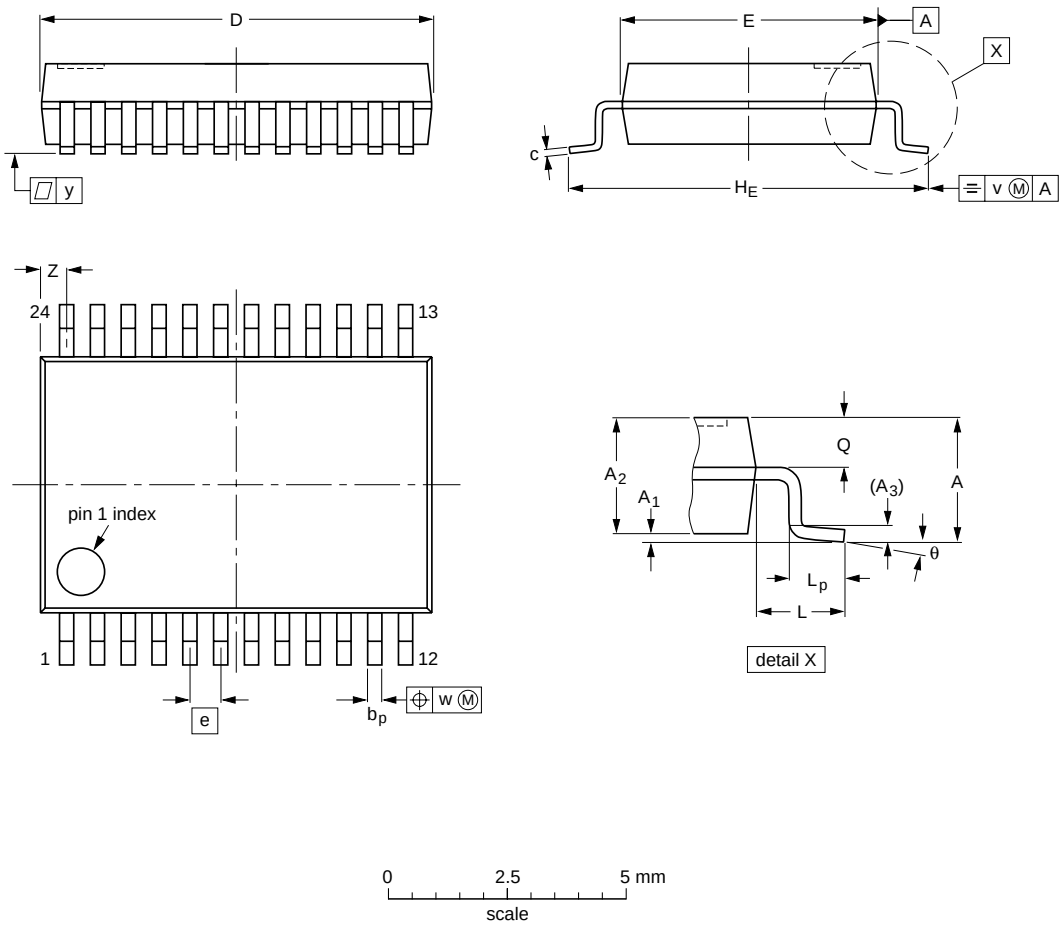
SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT340-1 (SSOP24)

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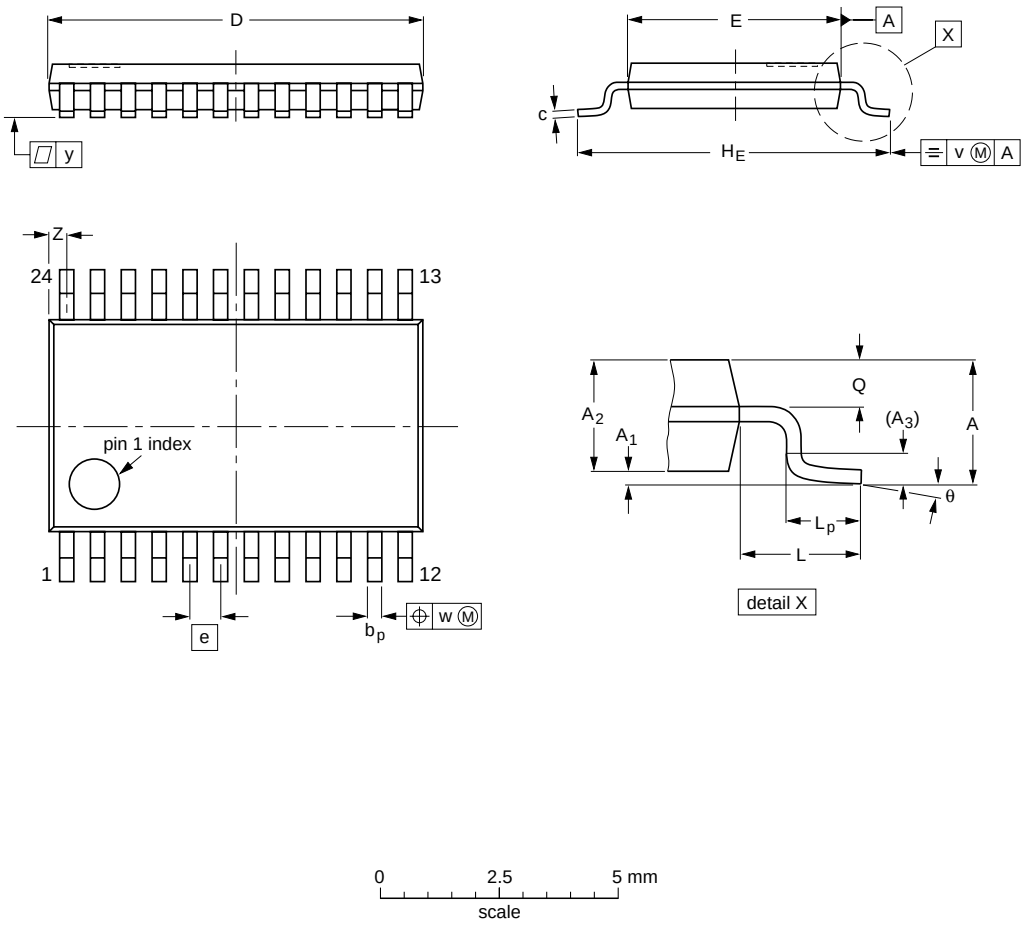
TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 14. Package outline SOT355-1 (TSSOP24)

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15. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74ABT544_3	20050420	Product data sheet	-	9397 750 14756	74ABT544_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 2; changed latch-up protection to JESD78. • Table 1; changed typical values for propagation delay. • Table 8; changed values for propagation delay, output enable time and output disable time.				
74ABT544_2	20021118	Product specification	-	9397 750 10752	74ABT544
74ABT544	19930701	Product specification	-	-	-

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16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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