74AHC1G09

2-input AND gate with open-drain output

Rev. 01 — 26 September 2005 **Product data sheet**

1. General description

The 74AHC1G09 is a high-speed Si-gate CMOS device.

The 74AHC1G09 provides the 2-input AND function with open-drain output.

The output of the 74AHC1G09 is an open drain and can be connected to other open-drain outputs to implement active-LOW, wired-OR or active-HIGH wired-AND functions. For digital operation this device must have a pull-up resistor to establish a logic HIGH level.

2. Features

- High noise immunity
- ESD protection:
  - HBM JESD22-A114-C exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Low power dissipation
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C.

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PZL}, t_{PLZ}	propagation delay A and B to Y	V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF		-	3.2	5.5	ns
C_i	input capacitance			-	1.5	10	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[1]	-	5	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$(C_L \times V_{CC}^2 \times f_o)$ = dissipation due to the output if the combination of the pull up voltage and resistance results in V_{CC} at the output.

PHILIPS

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC1G09GW	–40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1

5. Marking

Table 3: Marking

Type number	Marking code
74AHC1G09GW	A9

6. Functional diagram

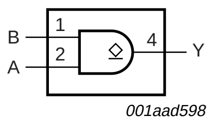


Fig 1. Logic symbol

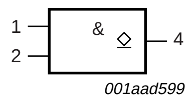


Fig 2. IEC logic symbol

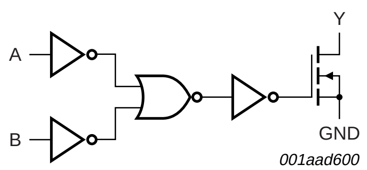


Fig 3. Logic diagram

7. Pinning information

7.1 Pinning

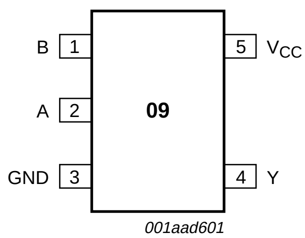


Fig 4. Pin configuration SOT353-1 (TSSOP5)

7.2 Pin description

Table 4: Pin description

Symbol	Pin	Description
B	1	data input B
A	2	data input A
GND	3	ground (0 V)
Y	4	data output Y
V_{CC}	5	supply voltage

8. Functional description

8.1 Function table

Table 5: Function table [1]

Input		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
Z = high-impedance OFF-state.

9. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage		[1]	–0.5	+7.0	V
V_O	output voltage	active mode	[1]	–0.5	+7.0	V
		high-impedance mode	[1]	–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1]	-	–20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O > -0.5$ V		-	25	mA
I_{CC}	quiescent supply current			-	±75	mA
I_{GND}	GND current			-	±75	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP5 packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

10. Recommended operating conditions

Table 7: Recommended operating operations

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	active mode	0	-	V_{CC}	V
		high-impedance mode	0	-	6.0	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 3.0 V to 3.6 V	-	-	100	ns/V
		V_{CC} = 4.5 V to 5.5 V	-	-	20	ns/V

11. Static characteristics

Table 8: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 3.0 V	2.1	-	-	V
		V_{CC} = 5.5 V	3.85	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 50 μA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 50 μA; V_{CC} = 3.0 V	-	0	0.1	V
		I_O = 50 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.25	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	1.0	μA
C_i	input capacitance		-	1.5	10	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 3.0 V	2.1	-	-	V
		V_{CC} = 5.5 V	3.85	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	V

Table 8: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50\ \mu A$; $V_{CC} = 2.0\ V$	-	-	0.1	V
		$I_O = 50\ \mu A$; $V_{CC} = 3.0\ V$	-	-	0.1	V
		$I_O = 50\ \mu A$; $V_{CC} = 4.5\ V$	-	-	0.1	V
		$I_O = 4.0\ mA$; $V_{CC} = 3.0\ V$	-	-	0.44	V
		$I_O = 8.0\ mA$; $V_{CC} = 4.5\ V$	-	-	0.44	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\ V$	-	-	±1.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5\ V$	-	-	±2.5	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0\ A$; $V_{CC} = 5.5\ V$	-	-	10	μA
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\ V$	1.5	-	-	V
		$V_{CC} = 3.0\ V$	2.1	-	-	V
		$V_{CC} = 5.5\ V$	3.85	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\ V$	-	-	0.5	V
		$V_{CC} = 3.0\ V$	-	-	0.9	V
		$V_{CC} = 5.5\ V$	-	-	1.65	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50\ \mu A$; $V_{CC} = 2.0\ V$	-	-	0.1	V
		$I_O = 50\ \mu A$; $V_{CC} = 3.0\ V$	-	-	0.1	V
		$I_O = 50\ \mu A$; $V_{CC} = 4.5\ V$	-	-	0.1	V
		$I_O = 4.0\ mA$; $V_{CC} = 3.0\ V$	-	-	0.55	V
		$I_O = 8.0\ mA$; $V_{CC} = 4.5\ V$	-	-	0.55	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\ V$	-	-	±2.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5\ V$	-	-	±10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0\ A$; $V_{CC} = 5.5\ V$	-	-	20	μA

12. Dynamic characteristics

Table 9: Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $t_r = t_f \leq 3.0$ ns; see Figure 6.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
t_{PZL}, t_{PLZ}	propagation delay A and B to Y	see Figure 5					
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	[1]	-	4.6	7.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	[1]	-	3.2	5.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	[1]	-	6.5	11.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	[1]	-	4.6	7.5	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC}	[2]	-	5	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PZL}, t_{PLZ}	propagation delay A and B to Y	see Figure 5					
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF		1.0	-	8.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF		1.0	-	6.5	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF		1.5	-	12.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF		1.5	-	8.0	ns
T_{amb} = −40 °C to +125 °C							
t_{PZL}, t_{PLZ}	propagation delay A and B to Y	see Figure 5					
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF		1.0	-	9.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF		1.0	-	7.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF		1.5	-	12.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF		1.5	-	8.5	ns

[1] All typical values are measured at nominal V_{CC}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

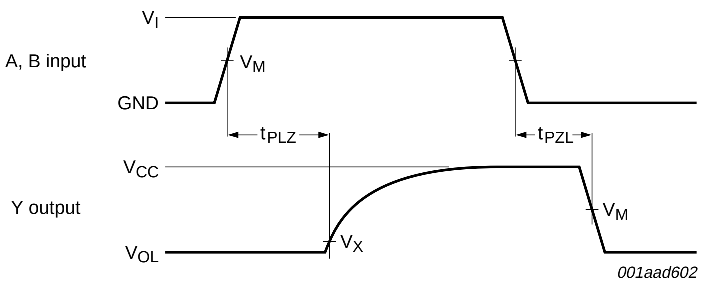
C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = number of inputs switching;

$(C_L \times V_{CC}^2 \times f_o)$ = dissipation due to the output if the combination of the pull up voltage and resistance results in V_{CC} at the output.

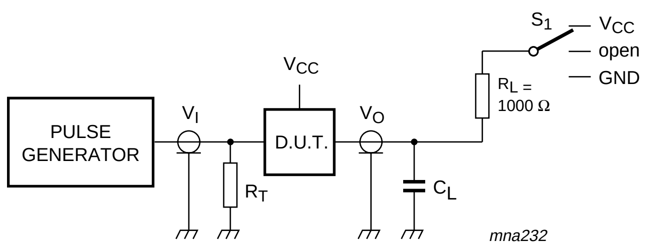
13. Waveforms



$V_M = 0.5V_{CC}$; V_I = GND to V_{CC}.

V_{OL} is the typical voltage output drop that occur with the output load.

Fig 5. The data input (A, B) to output (Y) propagation delays



Test data is given in Table 10.

Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

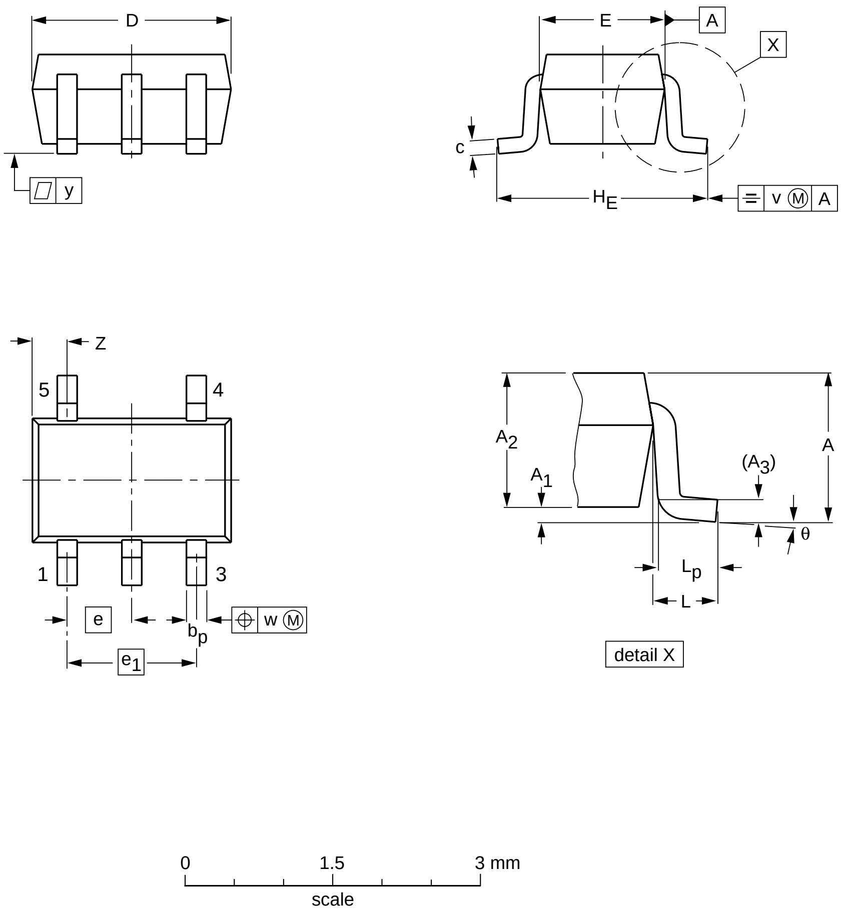
Fig 6. Load circuitry for switching times

Table 10: Test data

Input		Load		S_1		
V_I	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
GND to V_{CC}	≤ 3.0 ns	1000 Ω	15 pF	GND	V_{CC}	open
GND to V_{CC}	≤ 3.0 ns	1000 Ω	50 pF	GND	V_{CC}	open

14. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	e_1	H_E	L	L_p	v	w	y	Z(1)	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~00-09-01~~ 03-02-19

Fig 7. Package outline SOT353-1 (TSSOP5)

15. Abbreviations

Table 11: Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

16. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74AHC1G09_1	20050926	Product data sheet	-	-	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

19. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

20. Trademarks

Notice — All referenced brands, product names, service names and trademarks are the property of their respective owners.

21. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

22. Contents

Date of release: 26 September 2005
Document number: 74AHC1G09_1

Published in The Netherlands