

DATA SHEET

74LV368

Hex buffer/line driver; inverting (3-State)

Product specification
Supersedes data of 1997 Apr 07
IC24 Data Handbook

1998 May 29

Hex buffer/line driver; inverting (3-State)

74LV368

FEATURES

- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between $V_{CC} = 2.7V$ and $V_{CC} = 3.6V$
- Typical V_{OLP} (output ground bounce) $< 0.8V$ @ $V_{CC} = 3.3V$, $T_{amb} = 25^{\circ}C$
- Typical V_{OHV} (output V_{OH} undershoot) $> 2V$ @ $V_{CC} = 3.3V$, $T_{amb} = 25^{\circ}C$
- Inverting outputs
- Output capability: bus driver
- I_{CC} category: SSI

DESCRIPTION

The 74LV368 a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT368.

The 74LV368 is a hex inverting buffer/line driver with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state.

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^{\circ}C$; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA to nY	$C_L = 15pF$ $V_{CC} = 3.3V$	9.0	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per buffer	Notes 1, 2	30	pF

NOTES:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacitance in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
- The condition is $V_I = GND$ to V_{CC}

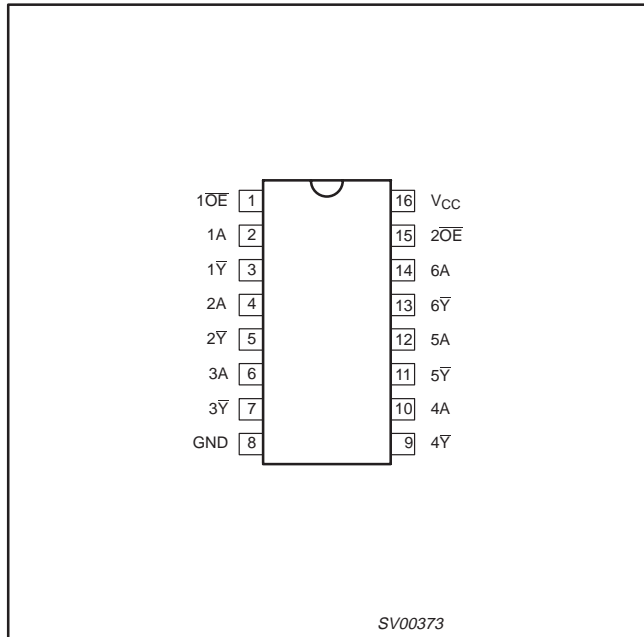
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	-40°C to +125°C	74LV368 N	74LV368 N	SOT38-4
16-Pin Plastic SO	-40°C to +125°C	74LV368 D	74LV368 D	SOT109-1
16-Pin Plastic SSOP Type II	-40°C to +125°C	74LV368 DB	74LV368 DB	SOT338-1
16-Pin Plastic TSSOP Type I	-40°C to +125°C	74LV368 PW	74LV368PW DH	SOT403-1

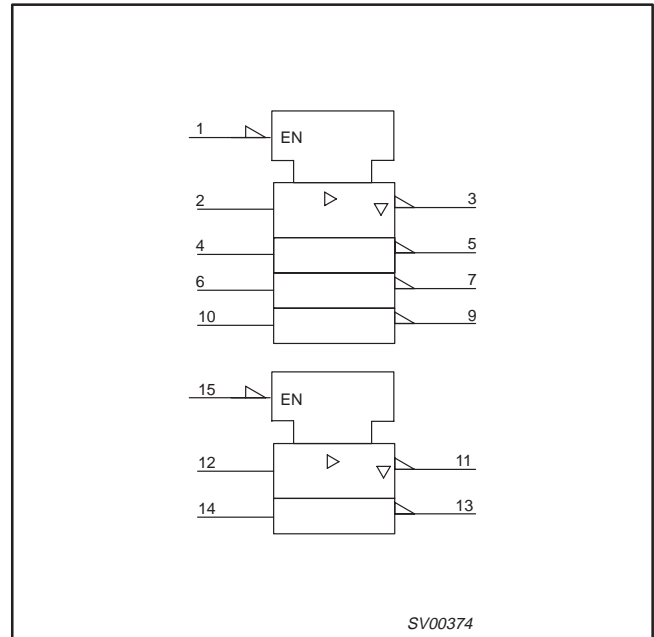
Hex buffer/line driver; inverting (3-State)

74LV368

PIN CONFIGURATION



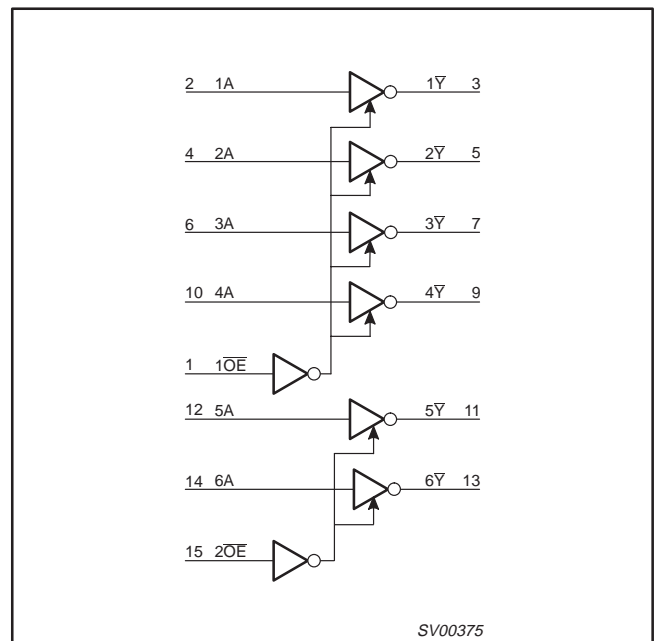
LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 15	1OE to 2OE	Output enable inputs (active LOW)
2, 4, 6, 10, 12, 14	1A to 6A	Data inputs
3, 5, 7, 9, 11, 13	1Y to 6Y	Bus outputs
8	GND	Ground (0V)
16	VCC	Positive supply voltage

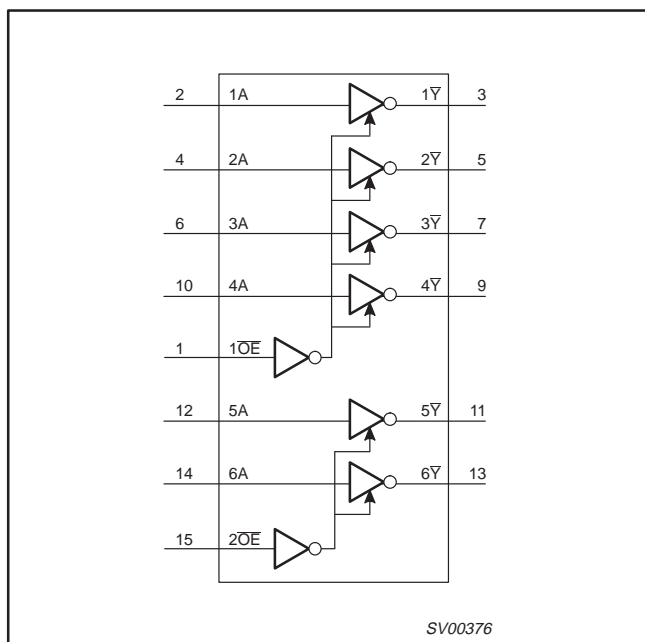
LOGIC SYMBOL



Hex buffer/line driver; inverting (3-State)

74LV368

FUNCTIONAL DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUT
nOE	nA	nY
L	L	H
L	H	L
H	X	Z

NOTES:
 H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 Z = High impedance OFF-state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note ¹	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$	– – –	– – –	500 200 100	ns/V

NOTES:
 1 The LV is guaranteed to function down to $V_{CC} = 1.0V$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2V$ to $V_{CC} = 3.6V$.

ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134); Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – bus driver outputs	$-0.5V < V_O < V_{CC} + 0.5V$	35	mA
$\pm I_{GND}, \pm I_{CC}$	DC V_{CC} or GND current for types with –bus driver outputs		70	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic DIL –plastic mini-pack (SO) –plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: –40 to +125°C above +70°C derate linearly with 12mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:
 1 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 2 The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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74LV368

DC CHARACTERISTICS FOR THE LV FAMILY

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP ¹	MAX	MIN	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	0.9			0.9		V
		V _{CC} = 2.0V	1.4			1.4		
		V _{CC} = 2.7 to 3.6V	2.0			2.0		
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			0.3		0.3	V
		V _{CC} = 2.0V			0.6		0.6	
		V _{CC} = 2.7 to 3.6V			0.8		0.8	
V _{OH}	HIGH level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA		1.2				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	1.8	2.0		1.8		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	2.5	2.7		2.5		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA	2.8	3.0		2.8		
V _{OH}	HIGH level output voltage; BUS driver outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; -I _O = 8mA	2.40	2.82		2.20		V
V _{OL}	LOW level output voltage; all outputs	V _{CC} = 1.2V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0				V
		V _{CC} = 2.0V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		0	0.2		0.2	
V _{OL}	LOW level output voltage; BUS driver outputs	V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 8mA		0.20	0.40		0.50	V
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND			1.0		1.0	µA
I _{oz}	3-State output OFF-state current	V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND			5		10	µA
I _{CC}	Quiescent supply current; MSI	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0			20.0		160	µA
ΔI _{CC}	Additional quiescent supply current per input	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V			500		850	µA

NOTE:1 All typical values are measured at T_{amb} = 25°C.

Hex buffer/line driver; inverting (3-State)

74LV368

AC CHARACTERISTICS

GND = 0V; $t_r = t_f = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 1\text{K}\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS -40 to +85 °C			LIMITS -40 to +125 °C		UNIT
				V _{CC} (V)	MIN	TYP ¹	MAX	MIN	
t _{PZL} /t _{PLH}	Propagation delay nA, to n \bar{Y}	Figures, 1, 3	1.2	-	55	-	-	-	ns
			2.0	-	19	36	-	44	
			2.7	-	14	26	-	33	
			3.0 to 3.6	-	10 ²	21	-	26	
t _{PZH} /t _{PZL}	3-State output enable time n \bar{OE} to n \bar{Y}	Figures, 2, 3	1.2	-	75	-	-	-	ns
			2.0	-	26	49	-	60	
			2.7	-	19	36	-	44	
			3.0 to 3.6	-	14 ²	29	-	35	
t _{PHZ} /t _{PLZ}	3-State output disable time n \bar{OE} to n \bar{Y}	Figures, 2, 3	1.2	-	90	-	-	-	ns
			2.0	-	32	59	-	70	
			2.7	-	24	44	-	52	
			3.0 to 3.6	-	19 ²	36	-	42	

NOTE:

- 1 Unless otherwise stated, all typical values are at T_{amb} = 25°C.
- 2 Typical value measured at V_{CC} = 3.3V.

AC WAVEFORMS

V_M = 1.5V at V_{CC} ≥ 2.7V
 V_M = 0.5V * V_{CC} at V_{CC} < 2.7V
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 V_X = V_{OL} + 0.3V at V_{CC} ≥ 2.7V
 V_X = V_{OL} + 0.1 * V_{CC} at V_{CC} < 2.7V
 V_Y = V_{OH} - 0.3V at V_{CC} ≥ 2.7V
 V_Y = V_{OH} - 0.1V_{CC} at V_{CC} < 2.7V

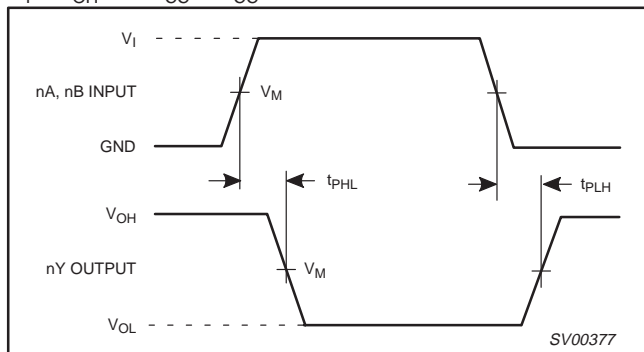


Figure 1. Input (nA) to output (n \bar{Y}) propagation delay

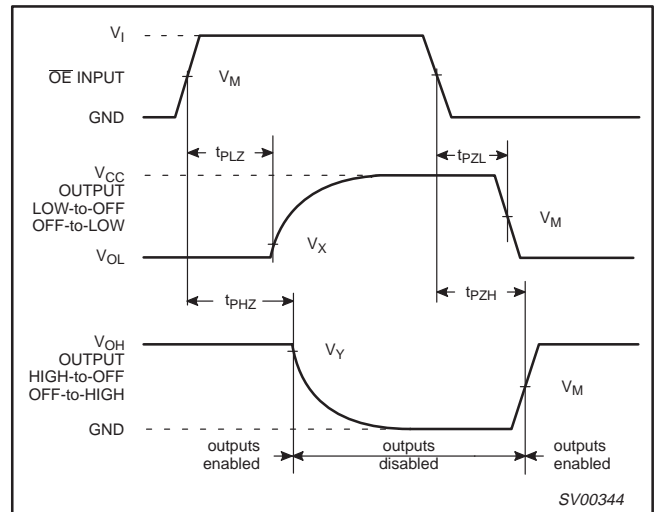


Figure 2. 3-State enable and disable times

Hex buffer/line driver; inverting (3-State)

74LV368

TEST CIRCUIT

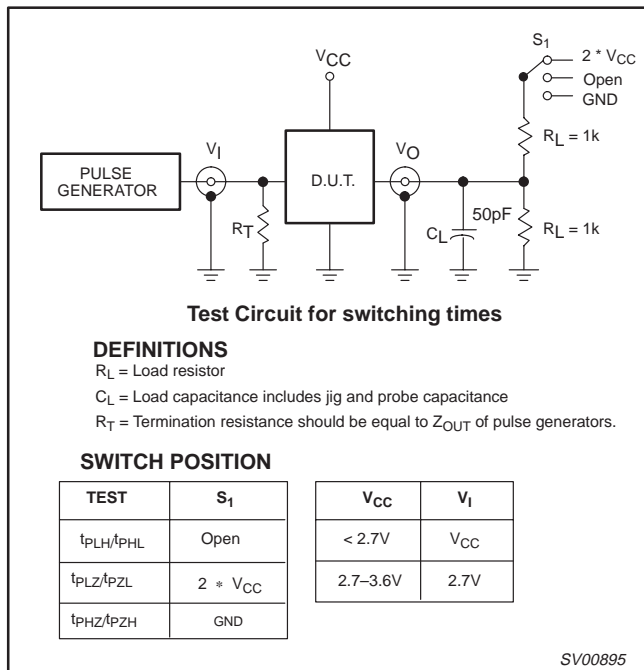


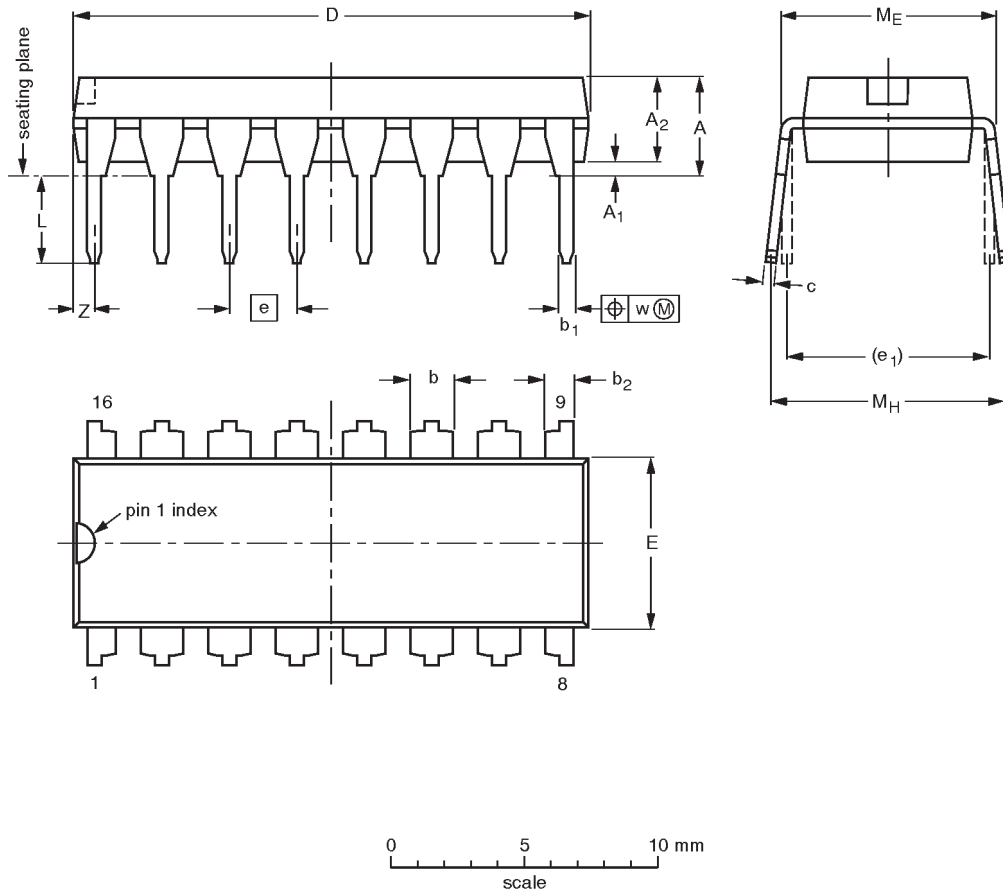
Figure 3. Load circuitry for switching times

Hex buffer/line driver; inverting (3-State)

74LV368

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

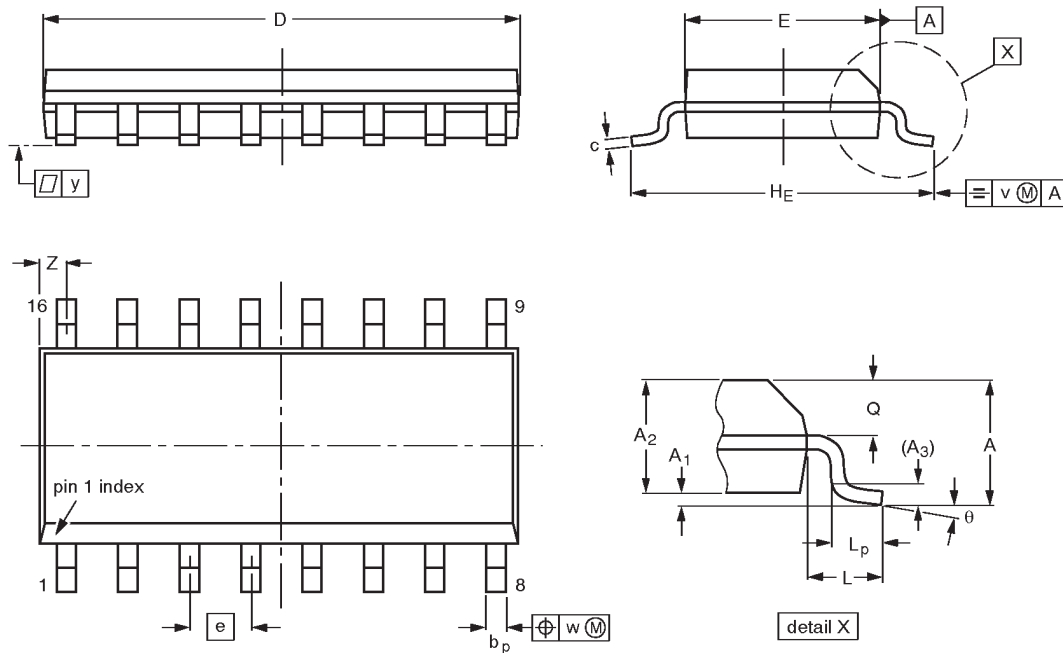
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						-92-11-17 95-01-14

Hex buffer/line driver; inverting (3-State)

74LV368

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

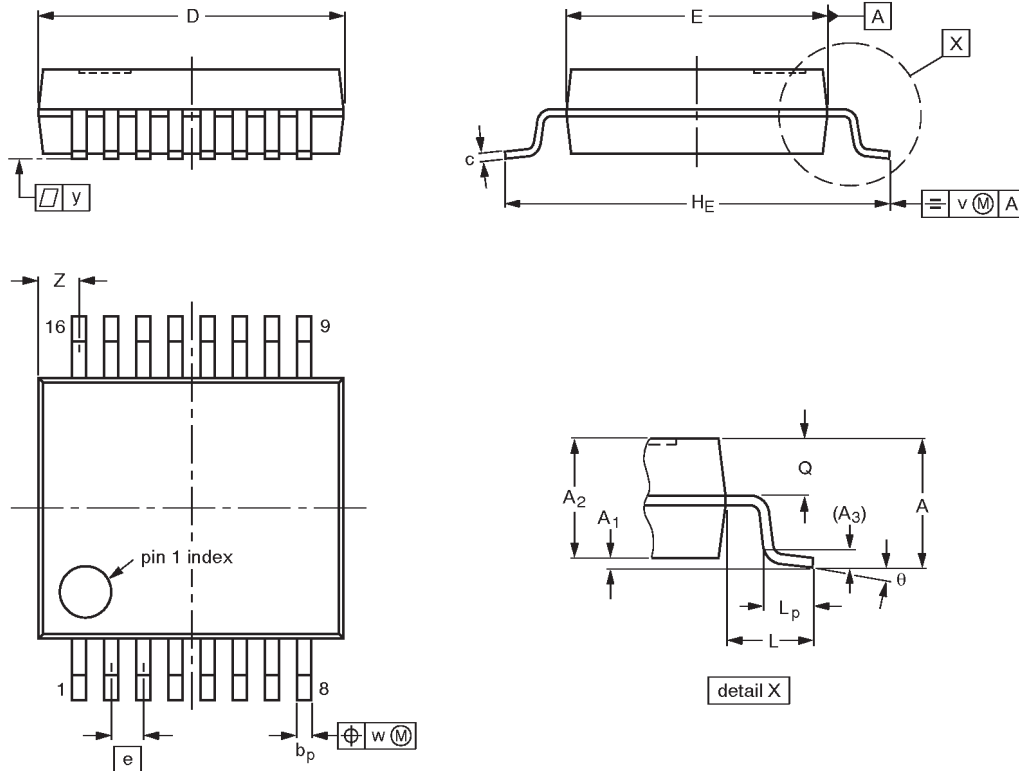
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	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				91-08-13 95-01-23

Hex buffer/line driver; inverting (3-State)

74LV368

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

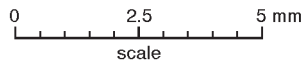
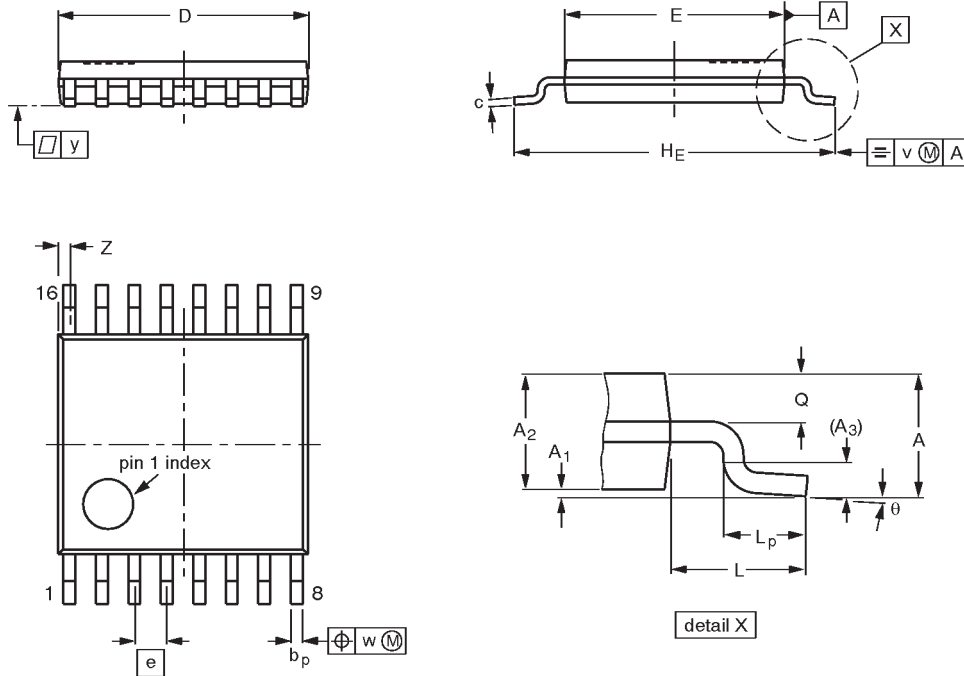
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14- 95-02-04

Hex buffer/line driver; inverting (3-State)

74LV368

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				94-07-12 95-04-04

Hex buffer/line driver; inverting (3-State)

74LV368

DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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