# ACS03MS

## Radiation Hardened Quad 2-Input NAND Gate with Open Drain

January 1996

### Features

- **Devices QML Qualified in Accordance with MIL-PRF-38535**
- **Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96703 and Intersil's QM Plan**
- **1.25 Micron Radiation Hardened SOS CMOS**
- **Total Dose . . . . . >300K RAD (Si)**
- **Single Event Upset (SEU) Immunity: <1 x $10^{-10}$ Errors/Bit/Day (Typ)**
- **SEU LET Threshold . . . . . >100 MEV-$cm^2$/mg**
- **Dose Rate Upset . . . . . >$10^{11}$ RAD (Si)/s, 20ns Pulse**
- **Dose Rate Survivability . . . . . >$10^{12}$ RAD (Si)/s, 20ns Pulse**
- **Latch-Up Free Under Any Conditions**
- **Military Temperature Range . . . . . -55°C to +125°C**
- **Significant Power Reduction Compared to ALSTTL Logic**
- **DC Operating Voltage Range . . . . . 4.5V to 5.5V**
- **Input Logic Levels**
  - **VIL = 30% of VCC Max**
  - **VIH = 70% of VCC Min**
- **Input Current ≤ 1μA at VOL, VOH**
- **Fast Propagation Delay . . . . . 15ns (Max), 10ns (Typ)**

### Description

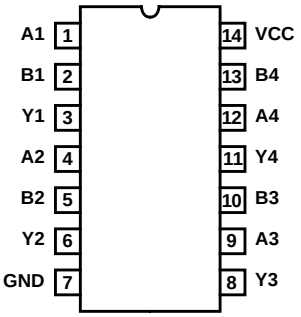
The Intersil ACS03MS is a Radiation Hardened quad 2-input NAND gate with open drain outputs. The open drain output can drive resistive loads from a separate supply voltage.

The ACS03MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of a radiation hardened, high-speed, CMOS/SOS Logic Family.

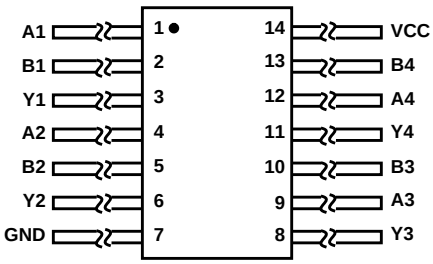
The ACS03MS is supplied in a 14 lead Ceramic Flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

### Pinouts

**14 PIN CERAMIC DUAL-IN-LINE**
**MIL-STD-1835 DESIGNATOR CDIP2-T14,**
**LEAD FINISH C**
TOP VIEW




**14 PIN CERAMIC FLATPACK**
**MIL-STD-1835 DESIGNATOR CDFP3-F14,**
**LEAD FINISH C**
TOP VIEW




### Ordering Information

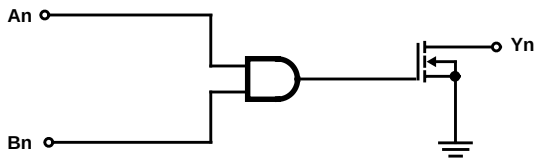
| PART NUMBER | TEMPERATURE RANGE | SCREENING LEVEL | PACKAGE |
|---|---|---|---|
| 5962F9670301VCC | -55°C to +125°C | MIL-PRF-38535 Class V | 14 Lead SBDIP |
| 5962F9670301VXC | -55°C to +125°C | MIL-PRF-38535 Class V | 14 Lead Ceramic Flatpack |
| ACS03D/Sample | 25°C | Sample | 14 Lead SBDIP |
| ACS03K/Sample | 25°C | Sample | 14 Lead Ceramic Flatpack |
| ACS03HMSR | 25°C | Die | Die |





Spec Number **518779**
File Number **3064.1**

## Functional Diagram




**TRUTH TABLE**

| INPUTS | | OUTPUT |
|---|---|---|
| **An** | **Bn** | **Yn** |
| L | L | Z (Note 2), H (Note 3) |
| L | H | Z (Note 2), H (Note 3) |
| H | L | Z (Note 2), H (Note 3) |
| H | H | L |

NOTES:

1. L = Low, H = High, Z = High Impedance
2. Without Pull-up Resistor
3. With Pull-up Resistor

## Die Characteristics

**DIE DIMENSIONS:**

68 mils x 79 mils
1730mm x 2010mm

**METALLIZATION:**

Type: AlSi
Metal 1 Thickness: 7.125kÅ ±1.125kÅ
Metal 2 Thickness: 9kÅ ±1kÅ

**GLASSIVATION:**

Type: $SiO_2$
Thickness: 8kÅ ±1kÅ

**WORST CASE CURRENT DENSITY:**

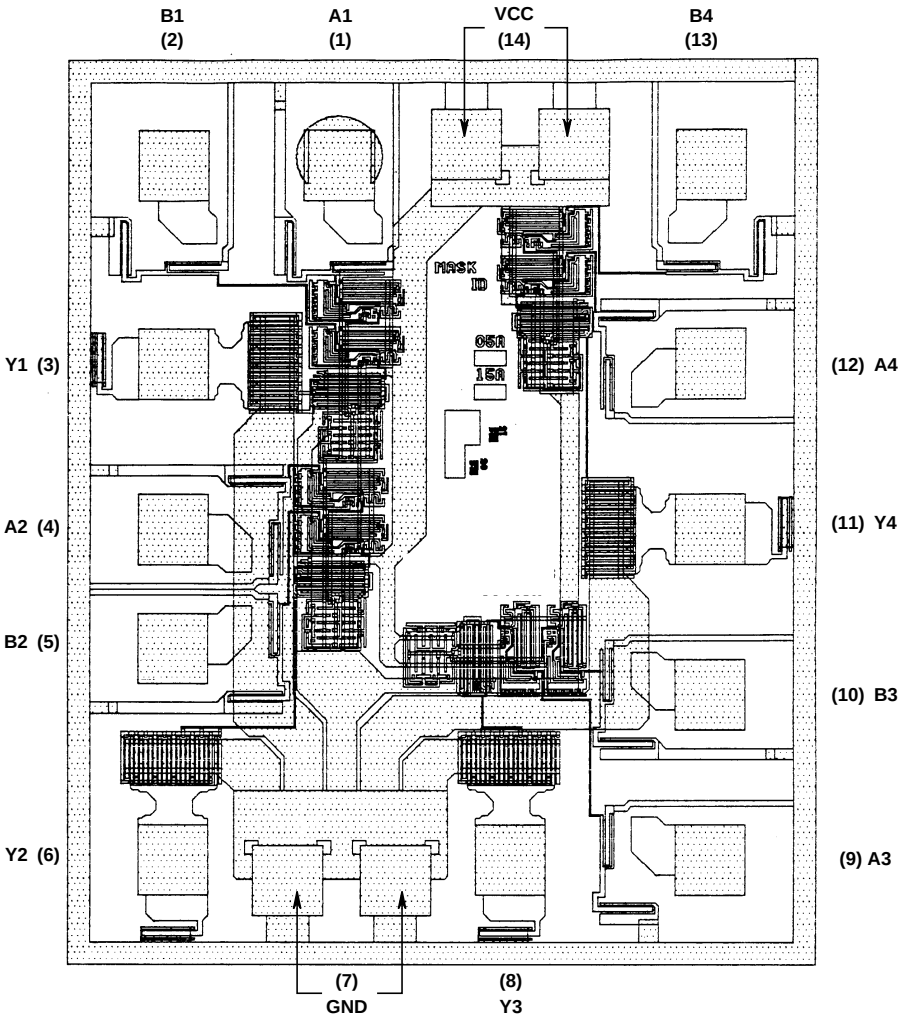
$<2.0 \times 10^5 A/cm^2$

**BOND PAD SIZE:**

110µm x 110µm
4.3 mils x 4.3 mils

## Metallization Mask Layout

**ACS03MS**



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