AKM

AKD4122
Evaluation board Rev.A for AK4122

GENERAL DESCRIPTION

The AKD4122 is an evaluation board for the digital sample rate converter, the AK4122 with built-in digital audio interface receiver (DIR). The AKD4122 has the digital audio interface and can achieve the interface with digital audio system via opt-connector.

■ **Ordering guide**

AKD4122   ---   Evaluation board for AK4122
(Cable for connecting with printer port of IBM-AT compatible PC and control software are packed with this. This control software does not operate on Windows NT.)

FUNCTION

- **DIR/DIT with optical input/output**
- **10pin Header for AKM AD/DA evaluation board**
- **BNC connector for an external clock input**
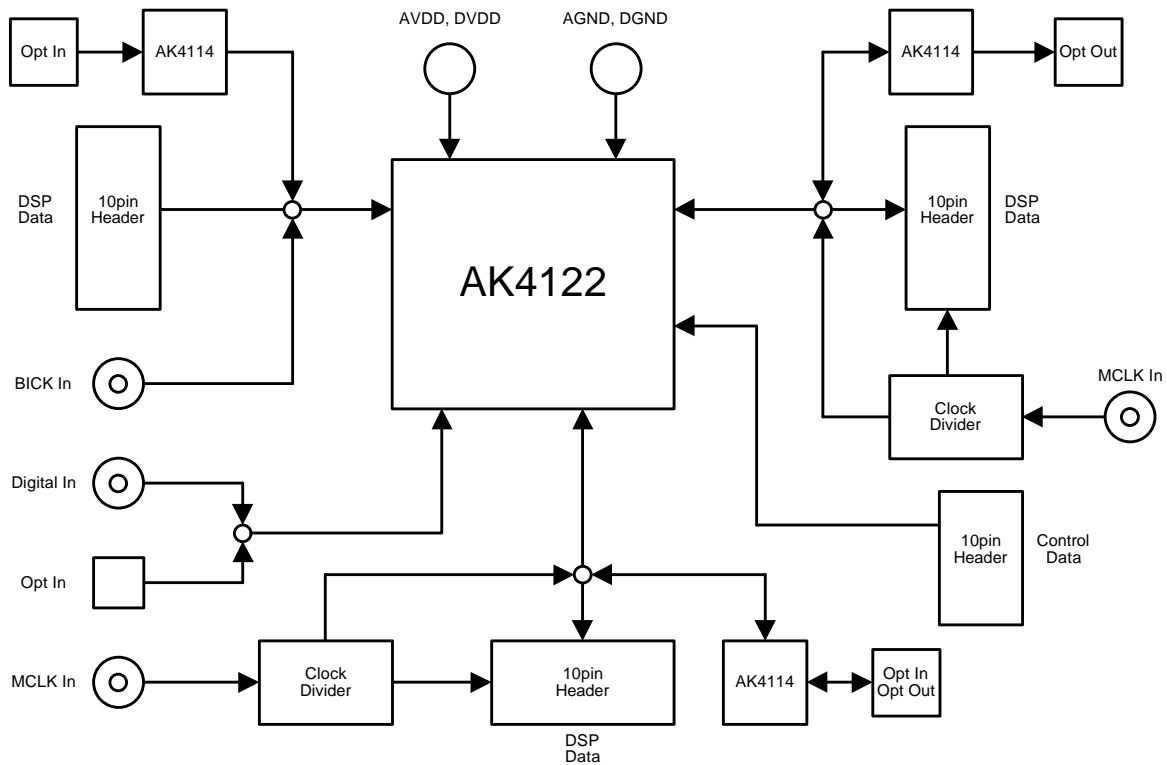- **10pin Header for serial control mode**

Figure 1. AKD4122 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

1. Evaluation Board Manual

■ Operation sequence

1) Set up the power supply lines.
[AVDD]	(red)	= 3.0 ~ 3.6V (typ. 3.3V, AVDD pin)
[DVDD]	(red)	= 3.0 ~ 3.6V (typ. 3.3V, DVDD pin)
[+5V]	(orange)	= +5V (for regulator)
[VCC]	(blue)	= 3.0 ~ 3.6V (typ. 3.3V, for digital logic)
[AGND]	(black)	= 0V
[DGND]	(black)	= 0V

   Each supply line should be distributed from the power supply unit.

2) Set up the evaluation mode, jumper pins. (See the followings.)

3) Power on.
   The AK4122 should be reset once bringing SW6 (PDN) "L" upon power-up.

■ Evaluation mode

I/O ports and jumper pins on the board should be set according to the following explanation in order to evaluate each pass of the AK4122. The block diagram is shown in Figure 2.
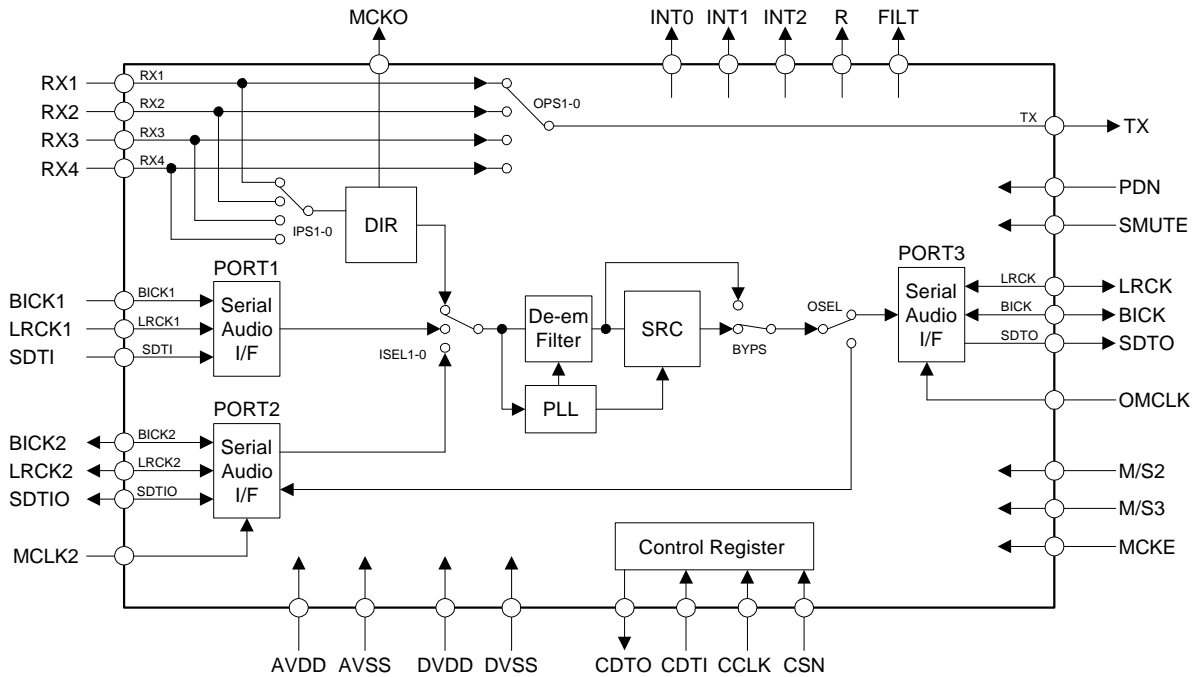

Figure 2. AK4122 Block Diagram

(1) AK4122 PORT1 → SRC → AK4122 PORT3

Refer to page 5 for input port setting, and page 15 ~ 18 for output port setting.
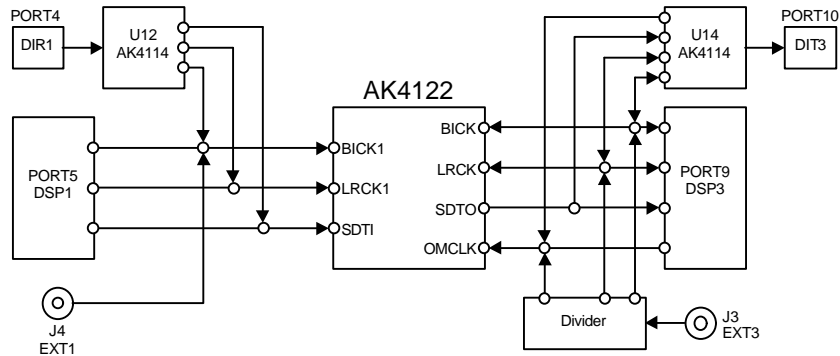

Figure 3. AK4122 PORT1 → SRC → AK4122 PORT3

(2) AK4122 PORT2 → SRC → AK4122 PORT3

Refer to page 6 ~ 9 for input port setting, and page 15 ~ 18 for output port setting.
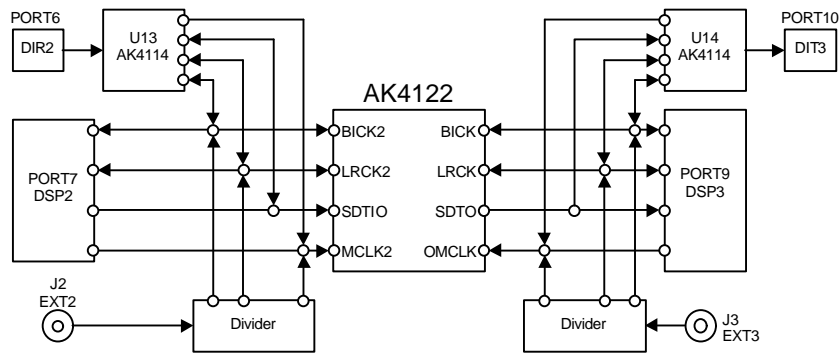

Figure 4. AK4122 PORT2 → SRC → AK4122 PORT3

(3) AK4122 DIR → SRC → AK4122 PORT3

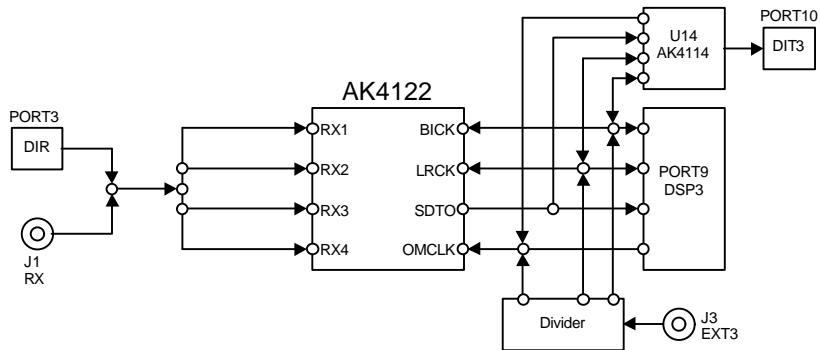Refer to page 10 for input port setting, and page 15 ~ 18 for output port setting.

Figure 5. AK4122 DIR → SRC → AK4122 PORT3

(4) AK4122 PORT1 → SRC → AK4122PORT2

Refer to page 5 for input port setting, and page 11 ~ 14 for output port setting.
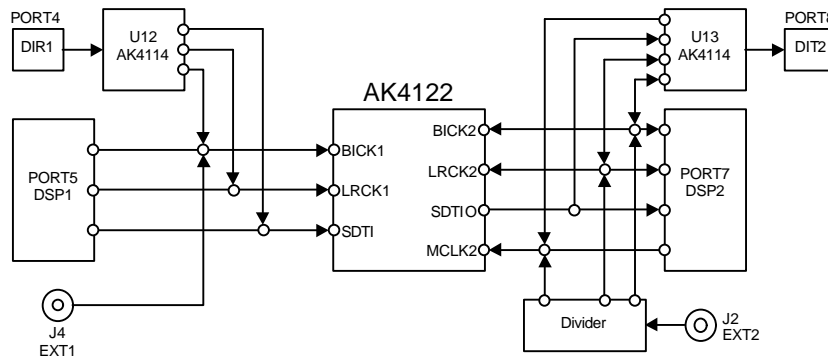

Figure 6. AK4122 PORT1 → SRC → AK4122 PORT2

(5) AK4122 DIR → SRC → AK4122 PORT2

Refer to page 10 for input port setting, and page 11 ~ 14 for output port setting.

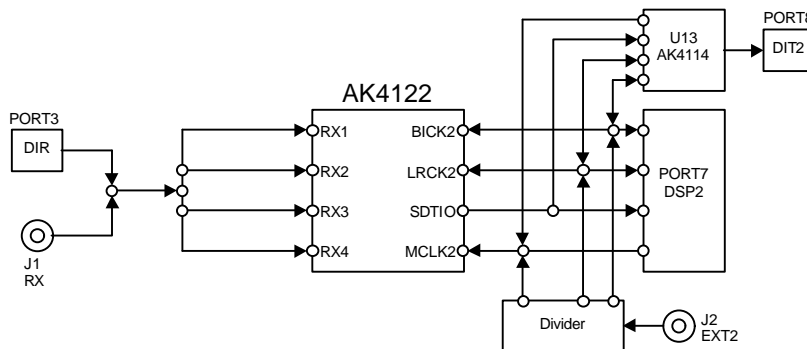Figure 7. AK4122 DIR → SRC → KA4122 PORT2

(6) Bypass Mode

Refer to page 5 ~ 10 for input port setting, and output port setting should be master mode. The bypass mode of the AK4122 is set by the register.

In bypass mode, the DIT function of the AK4114 can not be used as the output port. 10pin PORT should be used instead.
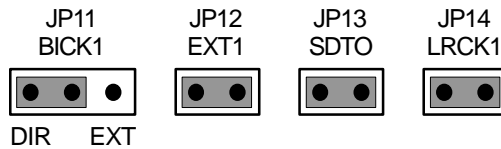
Input BICK, LRCK, and DATA are output from the output port side in the bypass mode.

(1) Setting for Input port (AK4122 PORT1)

(1-1) Slave Mode

1. When using DIR function of AK4114 (U12)

When using PORT4 (DIR1), nothing should be connected to J4 (EXT1) and PORT5 (DSP1). JP12 (EXT1) should be short.

JP11 BICK1 | JP12 EXT1 | JP13 SDTO | JP14 LRCK1

DIR   EXT

• SW2 setting (See Table 1, 2)
     Upper-side is "H" and lower-side is "L".

SW2 No.	Name	ON ("H")	OFF ("L")
1	OCKS	Fixed to "L"	
2	DIF0	AK4114 Audio Format Setting Refer to Table 2	
3	DIF1		
4	DIF2		

Table 1. SW2 setting

| Mode	Audio I/F Format	AK4114			AK4122		
		DIF2	DIF1	DIF0	DIF1	DIF0	
0	16bit, LSB justified	0	0	0	0	0	
1	24bit, MSB justified	1	0	0	0	1	Default
2	24bit, I^2S Compatible	1	0	1	1	0	
3	24bit, LSB justified	0	1	1	1	1	

Table 2. AK4114 Audio interface format setting

* DIF1-0 of the AK4122 is set by the register.

2. When connecting with the serial interface of UPD, ROHDE & SCHWARZ

When using PORT5 (DSP1), nothing should be connected to PORT4 (DIR1). BICK is input from J4 (EXT1), and the LRCK and SDTI are supplied from UPD. JP12 (EXT1) should be open.

JP11 BICK1 | JP12 EXT1 | JP13 SDTO | JP14 LRCK1

DIR   EXT
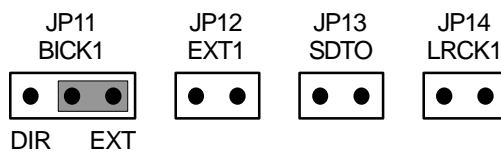
3. All clocks are fed through the 10pin port

When using PORT5 (DSP1), nothing should be connected to J4 (EXT1) and PORT4 (DIR1). JP12 (EXT1) should be short.

JP11 BICK1 | JP12 EXT1 | JP13 SDTO | JP14 LRCK1

DIR   EXT
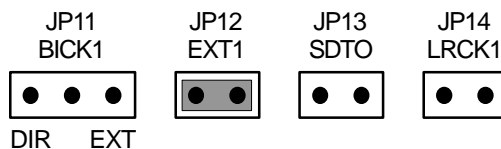
(2) Setting for Input port (AK4122 PORT2)

(2-1) Slave mode

1. When using DIR function of AK4114 (U13)

When using PORT6 (DIR2), nothing should be connected to J2 (EXT2) and PORT7 (DSP2). Set JP18 (MCLK2) to the "DIR" when MCLK is supplied to the AK4122.

JP15	JP16	JP17	JP18
SDTIO	BICK2	LRCK2	MCLK2

DIR EXT   DIR EXT   DIR EXT
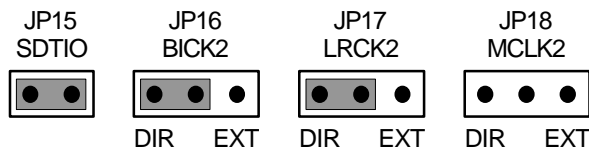
• SW3 setting (See Table 3, 4, 5)
    Upper-side is "H" and lower-side is "L".

SW3 No.	Name	ON ("H")	OFF ("L")
1	OCKS	AK4114 Master Clock Output Setting Refer to Table 4	
2	DIF0	AK4114 Audio Format Setting Refer to Table 5	
3	DIF1		
4	DIF2		

Table 3. SW3 setting

Mode	OCKS	MCKO1	X'tal	fs	
0	0	256fs	256fs	~ 96kHz	Default
1	1	512fs	512fs	~ 48kHz	

Table 4. AK4114 MCKO1 setting

Mode	Audio I/F Format	AK4114			AK4122		
		DIF2	DIF1	DIF0	IDIF1	IDIF0	
0	16bit, LSB justified	0	0	0	0	0	
1	24bit, MSB justified	1	0	0	0	1	Default
2	24bit, I^{2}S Compatible	1	0	1	1	0	
3	24bit, LSB justified	0	1	1	1	1	

Table 5. AK4114 Audio interface format setting

*** IDIF1-0 of the AK4122 is set by the register.**

2. When connecting with the serial interface of UPD, ROHDE & SCHWARZ

When using PORT7 (DSP2), nothing should be connected to PORT6 (DIR2). MCLK is input from J2 (EXT2), BICK is supplied by using the clock dividing circuit on this evaluation board and the LRCK and SDTI are supplied from UPD. Set JP18 (MCLK2) to the "EXT" when MCLK is supplied to the AK4122.
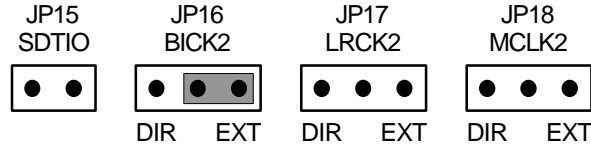
JP15 SDTIO	JP16 BICK2	JP17 LRCK2	JP18 MCLK2
● ●	● ● ●	● ● ●	● ● ●
	DIR EXT	DIR EXT	DIR EXT

• Clock Setting
MCLK is input from J2 (EXT2), BICK is supplied by using the clock dividing circuit. JP4 (DIV2) and JP5 (CLK2) are set by referring to Table 6. JP6 (BCFS) selects the frequency of BICK. JP7 (EXT2) should be open.

JP4 DIV2	JP5 CLK2	JP6 BCFS	JP7 EXT2
● ● ●	● ● ●	● ● ●	● ●
● ● ●	256 384	64fs 32fs	
256 512 768			
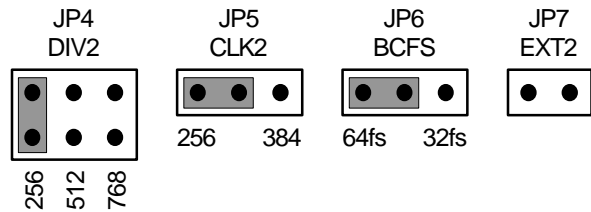
fs	MCLK	JP4(DIV2)	JP5(CLK2)
8kHz	256fs = 2.048MHz	256	256
	384fs = 3.072MHz	Open	384
	512fs = 4.096MHz	512	256
	768fs = 6.144MHz	768	256
32kHz	256fs = 8.192MHz	256	256
	384fs = 12.288MHz	Open	384
	512fs = 16.384MHz	512	256
	768fs = 24.576MHz	768	256
44.1kHz	256fs = 11.2896MHz	256	256
	384fs = 16.9344MHz	Open	384
	512fs = 22.5792MHz	512	256
	768fs = 33.8688MHz	768	256
48kHz	256fs = 12.288MHz	256	256
	384fs = 18.432MHz	Open	384
	512fs = 24.576MHz	512	256
	768fs = 36.864MHz	768	256
88.2kHz	256fs = 22.5792MHz	256	256
	384fs = 33.8688MHz	Open	384
96kHz	256fs = 24.576MHz	256	256
	384fs = 36.864MHz	Open	384

Table 6. Example for Clock setting

3. All clocks are fed through the 10pin port

When using PORT7 (DSP2), nothing should be connected to J2 (EXT2) and PORT6 (DIR2). JP7 (EXT2) should be short.

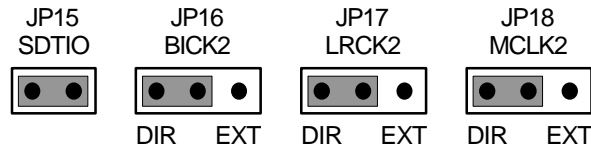| JP15	JP16	JP17	JP18
SDTIO	BICK2	LRCK2	MCLK2
● ●	● ● ●	● ● ●	● ● ●
	DIR EXT	DIR EXT	DIR EXT
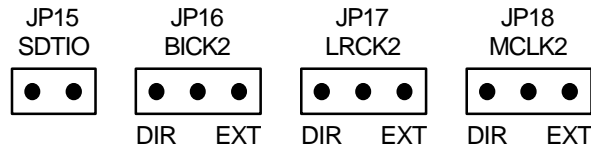
(2-2) Master mode

 MCLK must be provided in the master mode.

 1. When using DIR function of AK4114 (U13)

When using PORT6 (DIR2), nothing should be connected to J2 (EXT2) and PORT7 (DSP2). Set JP18 (MCLK2) to the "DIR" in order to supply MCLK to the AK4122.

JP15	JP16	JP17	JP18
SDTIO	BICK2	LRCK2	MCLK2
● ●	● ● ●	● ● ●	● ● ●
	DIR EXT	DIR EXT	DIR EXT

• SW3 setting (See Table 7, 8, 9)
     Upper-side is "H" and lower-side is "L".

SW3 No.	Name	ON ("H")	OFF ("L")
1	OCKS	AK4114 Master Clock Output Setting Refer to Table 8	
2	DIF0	AK4114 Audio Format Setting Refer to Table 9	
3	DIF1		
4	DIF2		

Table 7. SW3 setting

Mode	OCKS	MCKO1	X'tal	fs
0	0	256fs	256fs	~ 96kHz
1	1	512fs	512fs	~ 48kHz

Table 8. AK4114 MCKO1 setting

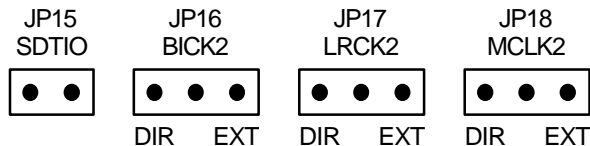| Mode	Audio I/F Format	AK4114			AK4122	
		DIF2	DIF1	DIF0	IDIF1	IDIF0
0	24bit, MSB justified	1	1	0	0	1
1	24bit, I^{2}S Compatible	1	1	1	1	0

Table 9. AK4114 Audio interface format setting

   * IDIF1-0 of the AK4122 is set by the register.

2. All clocks are fed through the 10pin port

When using PORT7 (DSP2), nothing should be connected to J2 (EXT2) and PORT6 (DIR2). JP7 (EXT2) should be short. MCLK is supplied to the AK4122, and the DATA that synchronizes with BICK and LRCK output from the AK4122 is supplied to the AK4122.

```
JP15            JP16              JP17              JP18
SDTIO           BICK2             LRCK2             MCLK2

┌─────────┐  ┌──────────────┐  ┌──────────────┐  ┌──────────────┐
│  ●   ●  │  │ ●    ●    ●  │  │ ●    ●    ●  │  │ ●    ●    ●  │
└─────────┘  └──────────────┘  └──────────────┘  └──────────────┘
              DIR      EXT       DIR      EXT       DIR      EXT
```

(2-3) SW1 setting

Set SW1 according to the mode of the AK4122 PORT2.

SW1 No.	Name	ON ("H")	OFF ("L")	Default
1	**M/S2**	**Master Mode**	**Slave Mode**	L
2	M/S3	Master Mode	Slave Mode	L
3	TST4	Fixed to "L"		L

Table 10. SW1 setting

(3) Setting for Input port (AK4122 DIR)

(3-1) Setting for DIR input

The signal source of AK4122's DIR can be set by JP2 (RX) and JP3 (RX1-4).
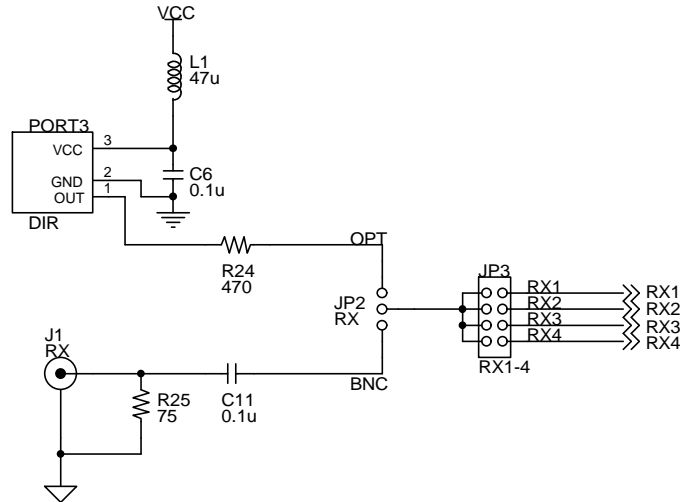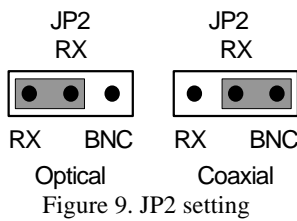

Figure 8. DIR input circuit
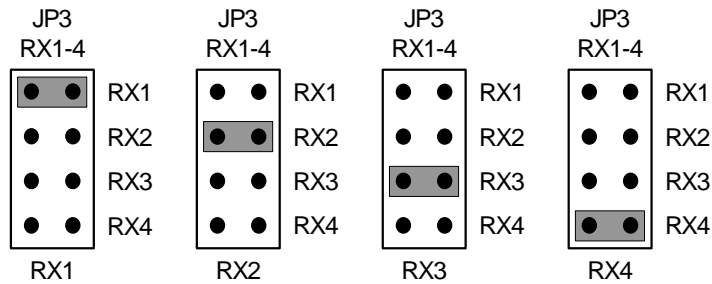

Figure 9. JP2 setting

Figure 10. JP3 setting

(3-2) Setting for DIR through signal

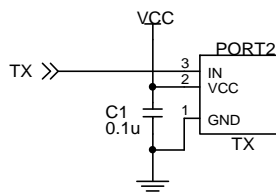DIR through signal of the AK4122 is output to TX pin via PORT2 (TX).

Figure 11. DIR through signal

(4) Setting for Output port (AK4122 PORT2)

(4-1) Slave mode

1. When using DIT function of AK4114 (U13)

When using X'tal (X1) and PORT8 (DIT2), nothing should be connected to PORT6 (DIR2) and PORT7 (DSP2). Set JP18 (MCLK2) to the "DIR" when MCLK is supplied to the AK4122. When MCLK frequency is changed, the value of X'tal (X1) frequency should be changed according to MCLK frequency.

JP15	JP16	JP17	JP18
SDTIO	BICK2	LRCK2	MCLK2
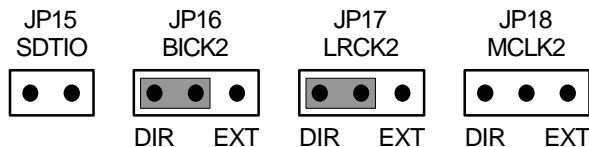
- SW3 setting (See Table 11, 12, 13)
  Upper-side is "H" and lower-side is "L".

SW3 No.	Name	ON ("H")	OFF ("L")
1	OCKS	AK4114 Master Clock Output Setting Refer to Table 12	
2	DIF0	AK4114 Audio Format Setting Refer to Table 13	
3	DIF1		
4	DIF2		

Table 11. SW3 setting

Mode	OCKS	MCKO1	X'tal	fs	
0	0	256fs	256fs	~ 96kHz	Default
1	1	512fs	512fs	~ 48kHz	

Table 12. AK4114 MCKO1 setting

Mode	Audio I/F Format	AK4114			AK4122		
		DIF2	DIF1	DIF0	IDIF1	IDIF0	
0	24bit, MSB justified	1	0	0	0	0	
1	24bit, MSB justified	1	0	0	0	1	Default
2	24bit, I^2S Compatible	1	0	1	1	0	
3	24bit, MSB justified	1	0	0	1	1	

Table 13. AK4114 Audio interface format setting

*** IDIF1-0 of the AK4122 is set by the register.**

2. When connecting with the serial interface of UPD, ROHDE & SCHWARZ

When using PORT7 (DSP2), nothing should be connected to PORT6 (DIR2). MCLK is input from J2 (EXT2), BICK and LRCK are supplied by using the clock dividing circuit on this evaluation board to the AK4122. Set JP18 (MCLK2) to the "EXT" when MCLK is supplied to the AK4122.

JP15	JP16	JP17	JP18
SDTIO	BICK2	LRCK2	MCLK2

DIR EXT   DIR EXT   DIR EXT
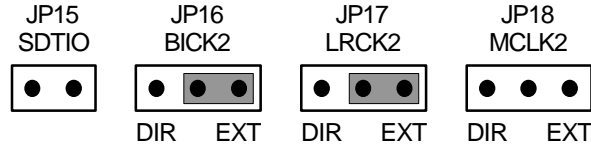
- Clock Setting
  MCLK is input from J2 (EXT2), BICK and LRCK are generated by using the clock dividing circuit. JP4 (DIV2) and JP5 (CLK2) are set by referring to Table 14. JP6 (BCFS) selects the frequency of BICK. JP7 (EXT2) should be open.

JP4	JP5	JP6	JP7
DIV2	CLK2	BCFS	EXT2

256 384   64fs 32fs

256 512 768
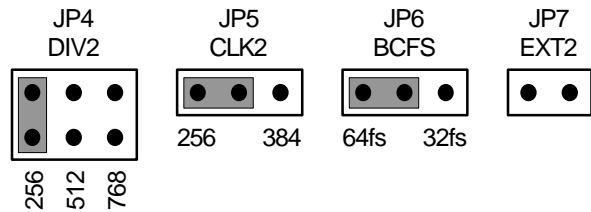
fs	MCLK	JP4(DIV2)	JP5(CLK2)
32kHz	256fs = 8.192MHz	256	256
	384fs = 12.288MHz	Open	384
	512fs = 16.384MHz	512	256
	768fs = 24.576MHz	768	256
44.1kHz	256fs = 11.2896MHz	256	256
	384fs = 16.9344MHz	Open	384
	512fs = 22.5792MHz	512	256
	768fs = 33.8688MHz	768	256
48kHz	256fs = 12.288MHz	256	256
	384fs = 18.432MHz	Open	384
	512fs = 24.576MHz	512	256
	768fs = 36.864MHz	768	256
88.2kHz	256fs = 22.5792MHz	256	256
	384fs = 33.8688MHz	Open	384
96kHz	256fs = 24.576MHz	256	256
	384fs = 36.864MHz	Open	384

Table 14. Example for Clock setting

3. All clocks are fed through the 10pin port

When using PORT7 (DSP2), nothing should be connected to J2 (EXT2) and PORT6 (DIR2). JP7 (EXT2) should be short.

| JP15	JP16	JP17	JP18
SDTIO	BICK2	LRCK2	MCLK2

DIR EXT   DIR EXT   DIR EXT
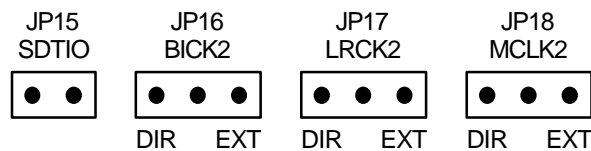
(4-2) Master mode

MCLK must be provided in the master mode.

1. When using DIT function of AK4114 (U13)

When using X'tal (X1) and PORT8 (DIT2), nothing should be connected to PORT6 (DIR2) and PORT7 (DSP2). Set JP18 (MCLK2) to the "DIR" when MCLK is supplied to the AK4122. When MCLK frequency is changed, the value of X'tal (X1) frequency should be changed according to MCLK frequency.
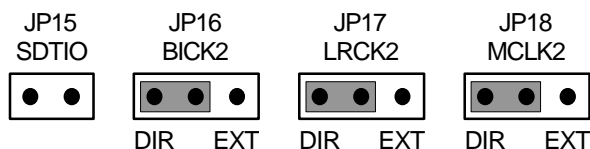
- SW3 setting (See Table 15, 16, 17)
  Upper-side is "H" and lower-side is "L".

SW3 No.	Name	ON ("H")	OFF ("L")
1	OCKS	AK4114 Master Clock Output Setting Refer to Table 16	
2	DIF0	AK4114 Audio Format Setting Refer to Table 17	
3	DIF1		
4	DIF2		

Table 15. SW3 setting

Mode	OCKS	MCKO1	X'tal	fs
0	0	256fs	256fs	~ 96kHz
1	1	512fs	512fs	~ 48kHz

Table 16. AK4114 MCKO1 setting

Mode	Audio I/F Format	AK4114			AK4122	
		DIF2	DIF1	DIF0	IDIF1	IDIF0
0	24bit, MSB justified	1	1	0	0	1
1	24bit, I^2S Compatible	1	1	1	1	0

Table 17. AK4114 Audio interface format setting

* IDIF1-0 of the AK4122 is set by the register.

2. When connecting with the serial interface of UPD, ROHDE & SCHWARZ

When using PORT7 (DSP2), nothing should be connected to PORT6 (DIR2) and PORT8 (DIT2). MCLK is input from J2 (EXT2), BICK LRCK, and DATA are supplied from the AK4122. Set JP18 (MCLK2) to the "EXT" in order to supply MCLK to the AK4122.

JP15	JP16	JP17	JP18
SDTIO	BICK2	LRCK2	MCLK2
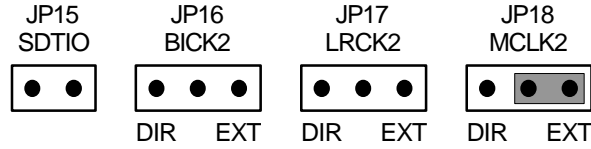
- Clock Setting
  MCLK is input from J2 (EXT2). JP7 (EXT2) should be open.
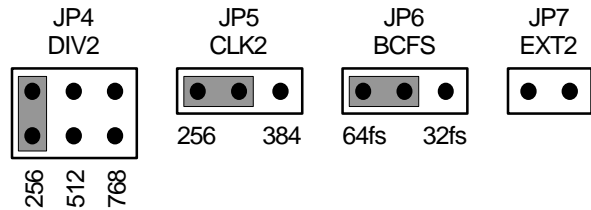
JP4	JP5	JP6	JP7
DIV2	CLK2	BCFS	EXT2

256 512 768

256 384   64fs 32fs

3. All clocks are fed through the 10pin port

When using PORT7 (DSP2), nothing should be connected to J2 (EXT2), PORT6 (DIR2) and PORT8 (DIT2). JP7 (EXT2) should be short. MCLK is supplied to the AK4122, and BICK, LRCK and DATA are supplied from the AK4122.

JP15	JP16	JP17	JP18
SDTIO	BICK2	LRCK2	MCLK2
	DIR EXT	DIR EXT	DIR EXT
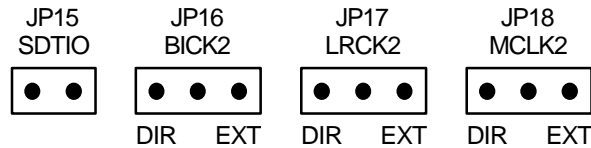
(4-3) SW1 setting

Set SW1 according to the mode of the AK4122 PORT2.

| SW1 No.	Name	ON ("H")	OFF ("L")	Default
1	**M/S2**	**Master Mode**	**Slave Mode**	L
2	M/S3	Master Mode	Slave Mode	L
3	TST4	Fixed to "L"		L

Table 18. SW1 setting

(5) Setting for Output port (AK4122 PORT3)

(5-1) Slave mode

1. When using DIT function of AK4114 (U14)

When using X'tal (X2) and PORT10 (DIT3), nothing should be connected to PORT9 (DSP3). Please set JP21 (OMCLK) to the "DIT" when MCLK is supplied to the AK4122. When MCLK frequency is changed, the value of X'tal (X2) frequency should be changed according to MCLK frequency.

JP19	JP20	JP21	JP25
BICK	LRCK	OMCLK	TST

DIT EXT   DIT EXT   DIT EXT   OMCK TST
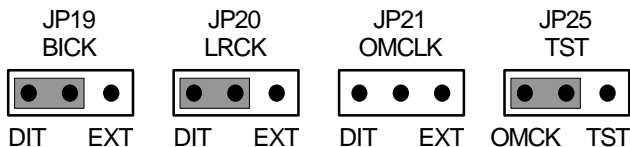
- SW4 setting (See Table 19, 20, 21)
  Upper-side is "H" and lower-side is "L".

SW4 No.	Name	ON ("H")	OFF ("L")
1	OCKS	AK4114 Master Clock Output Setting Refer to Table 20	
2	DIF0	AK4114 Audio Format Setting Refer to Table 21	

Table 19. SW4 setting

Mode	OCKS	MCKO1	X'tal	fs	
0	0	256fs	256fs	~ 96kHz	Default
1	1	512fs	512fs	~ 48kHz	

Table 20. AK4114 MCKO1 setting

Mode	Audio I/F Format	AK4114 DIF0	AK4122 ODIF	
0	24bit, MSB justified	0	0	Default
1	24bit, I^2S Compatible	1	1	

Table 21. AK4114 Audio interface format setting

*** ODIF of the AK4122 is set by the register.**

2. When connecting with the serial interface of UPD, ROHDE & SCHWARZ

When using PORT9 (DSP3), nothing should be connected to PORT10 (DIT3). MCLK is input from J3 (EXT3), BICK and LRCK are supplied by using the clock dividing circuit on this evaluation board to the AK4122. Set JP21 (OMCLK) to the "EXT" when MCLK is supplied to the AK4122.

| JP19 | JP20 | JP21 | JP25 |
| BICK | LRCK | OMCLK | TST |

| DIT EXT | DIT EXT | DIT EXT | OMCK TST |
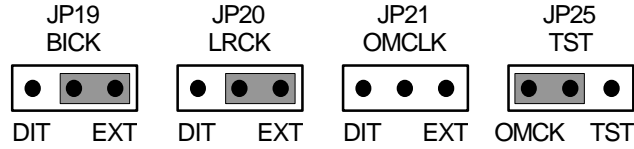
• Clock Setting
MCLK is input from J3 (EXT3), BICK and LRCK are generated by using the clock dividing circuit. JP8 (DIV3) and JP9 (CLK3) are set by referring to Table 22. JP10 (EXT3) should be open.

JP8 DIV3   JP9 CLK3   JP10 EXT3

256 512 768   256   384
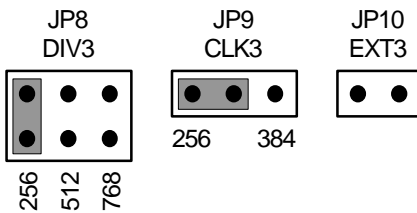
fs	MCLK	JP8(DIV3)	JP9(CLK3)
32kHz	256fs = 8.192MHz	256	256
	384fs = 12.288MHz	Open	384
	512fs = 16.384MHz	512	256
	768fs = 24.576MHz	768	256
44.1kHz	256fs = 11.2896MHz	256	256
	384fs = 16.9344MHz	Open	384
	512fs = 22.5792MHz	512	256
	768fs = 33.8688MHz	768	256
48kHz	256fs = 12.288MHz	256	256
	384fs = 18.432MHz	Open	384
	512fs = 24.576MHz	512	256
	768fs = 36.864MHz	768	256
88.2kHz	256fs = 22.5792MHz	256	256
	384fs = 33.8688MHz	Open	384
96kHz	256fs = 24.576MHz	256	256
	384fs = 36.864MHz	Open	384

Table 22. Example for Clock setting

3. All clocks are fed through the 10pin port

When using PORT9 (DSP3), nothing should be connected to PORT10 (DIT3). Set JP25 (TST) to the "OMCK" when MCLK is supplied to the AK4122. JP10 (EXT3) should be short.

| JP19 | JP20 | JP21 | JP25 |
| BICK | LRCK | OMCLK | TST |

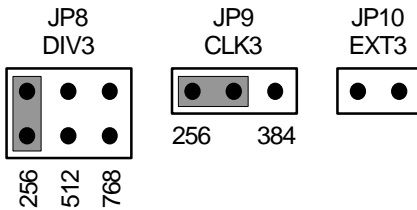| DIT EXT | DIT EXT | DIT EXT | OMCK TST |
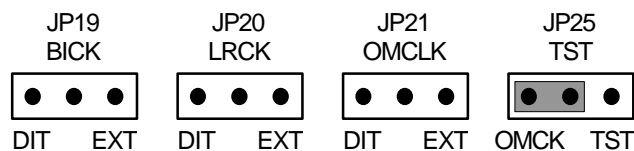
(5-2) Master mode

MCLK must be provided in the master mode.

1. When using DIT function of AK4114 (U14)

When using X'tal (X2) and PORT10 (DIT3), nothing should be connected to PORT9 (DSP3). Set JP21 (OMCLK) to the "DIT" in order to supply MCLK to the AK4122. When MCLK frequency is changed, the value of X'tal (X2) frequency should be changed according to MCLK frequency.

JP19	JP20	JP21	JP25
BICK	LRCK	OMCLK	TST
DIT ● ● ● EXT	DIT ● ● ● EXT	DIT ● ● ● EXT	OMCK ● ● ● TST
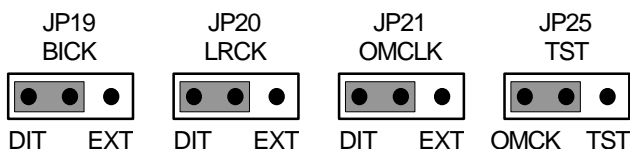
• SW4 setting (See Table 23, 24, 25)
Upper-side is "H" and lower-side is "L".

SW4 No.	Name	ON ("H")	OFF ("L")
1	OCKS	AK4114 Master Clock Output Setting Refer to Table 24	
2	DIF0	AK4114 Audio Format Setting Refer to Table 25	

Table 23. SW4 setting

Mode	OCKS	MCKO1	X'tal	fs
0	0	256fs	256fs	~ 96kHz
1	1	512fs	512fs	~ 48kHz

Table 24. AK4114 MCKO1 setting

Mode	Audio I/F Format	AK4114 DIF0	AK4122 ODIF
0	24bit, MSB justified	0	0
1	24bit, I^{2}S Compatible	1	1

Table 25. AK4114 Audio interface format setting

* ODIF of the AK4122 is set by the register.

2. When connecting with the serial interface of UPD, ROHDE & SCHWARZ

When using PORT9 (DSP3), nothing should be connected to PORT10 (DIT3). MCLK is input from J3 (EXT3), BICK LRCK, and DATA are supplied from the AK4122. Set JP21 (OMCLK) to the "EXT" in order to supply MCLK to the AK4122.

<div align="center">

JP19 BICK	JP20 LRCK	JP21 OMCLK	JP25 TST
DIT EXT	DIT EXT	DIT EXT	OMCK TST

</div>
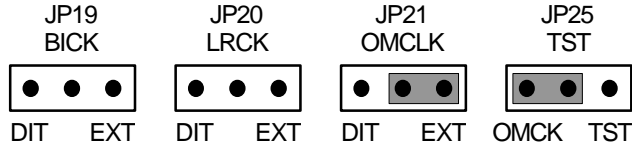
- Clock Setting
  MCLK is input from J3 (EXT3). JP10 (EXT3) should be open.

<div align="center">

JP8 DIV3	JP9 CLK3	JP10 EXT3
256 512 768	256 384	

</div>

3. All clocks are fed through the 10pin port

When using PORT9 (DSP3), nothing should be connected to J3 (EXT3) and PORT10 (DIT3). Set JP25 (TST) to the "OMCK" in order to supply MCLK to the AK4122. JP10 (EXT3) should be short. MCLK is supplied to the AK4122, and BICK, LRCK and DATA are supplied from the AK4122.

<div align="center">

JP19 BICK	JP20 LRCK	JP21 OMCLK	JP25 TST
DIT EXT	DIT EXT	DIT EXT	OMCK TST

</div>
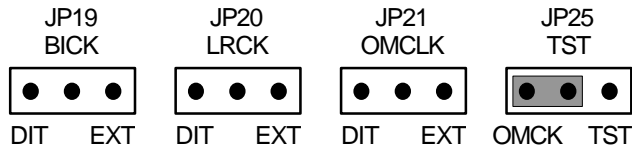
(5-3) SW1 setting

Set SW1 according to the mode of the AK4122 PORT3.

SW1 No.	Name	ON ("H")	OFF ("L")	Default
1	M/S2	Master Mode	Slave Mode	L
2	**M/S3**	**Master Mode**	**Slave Mode**	L
3	TST4	Fixed to "L"		L

Table 26. SW1 setting

■ **Other jumper pins set up**

    1. JP1 (GND) : Analog ground and Digital ground
        OPEN: Separated.
        SHORT: Common. (The connector "DGND" can be open.) <Default>

    2. JP22 (VDD2) : DVDD and VCC
        OPEN: Separated.
        SHORT: Common. (The connector "VCC" can be open.) <Default>

    3. JP23 (VDD1) : AVDD and DVDD
        OPEN: Separated.
        SHORT: Common. (The connector "DVDD" can be open.) <Default>

    4. JP24 (REG) : +5V and AVDD
        OPEN: Separated.
        SHORT: Common. (The connector "AVDD" can be open.) <Default>

The regulator can be supplied 3.3V to all circuits by shorting JP22, 23 and 24 and supplying 5V to +5V connector.

■ **The function of the toggle SW**

Upper-side is "H" and lower-side is "L".

[SW5] (SMUTE): Soft mute of AK4122

[SW6] (PDN): Resets the AK4122. Keep "H" during normal operation.
                The AK4122 should be resets once bringing "L" upon power-up.

[SW7] (PDN1): Resets the AK4114 (U12). Keep "H" during normal operation.
                The AK4114 (U12) should be resets once bringing "L" upon power-up.
                Keep "L" when AK4114 (U12) is not used.

[SW8] (PDN2): Resets the AK4114 (U13). Keep "H" during normal operation.
                The AK4114 (U13) should be resets once bringing "L" upon power-up.
                Keep "L" when AK4114 (U13) is not used.

[SW9] (PDN3): Resets the AK4114 (U14). Keep "H" during normal operation.
                The AK4114 (U14) should be resets once bringing "L" upon power-up.
                Keep "L" when AK4114 (U14) is not used.

■ **Indication for LED**

[LED1] (ERF): Monitor INT0 pin of the AK4114 (U12). LED turns on when unlock or parity error occurs.

[LED2] (ERF): Monitor INT0 pin of the AK4114 (U13). LED turns on when unlock or parity error occurs.

[LED3] (INT0): Monitor INT0 pin of the AK4122.

[LED4] (INT1): Monitor INT1 pin of the AK4122.

[LED5] (INT2): Monitor INT2 pin of the AK4122.

■ **Serial Control**

The AK4122 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT1 (CTRL) with PC by 10 wire flat cable packed with the AKD4122.
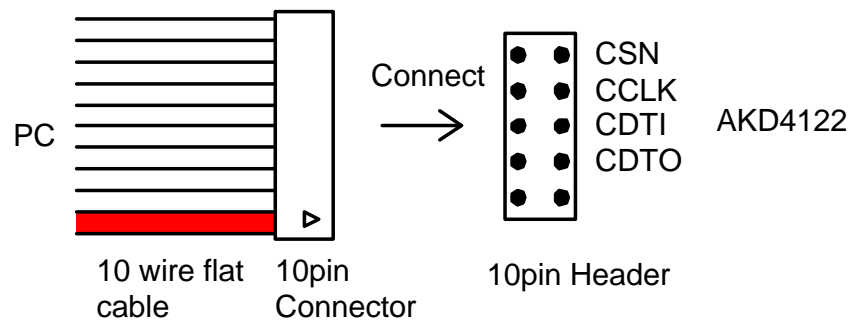
Figure 12. Connection of 10 wire flat cable

2. Control Software Manual

■ **Set-up of evaluation board and control software**

1. Set up the AKD4122 according to previous term.

2. Connect IBM-AT compatible PC with AKD4122 by 10-line type flat cable (packed with AKD4122). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AK4122 Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "akd4122-1.exe" and "akd4122-2"to set up the control program.

5. Then please evaluate according to the follows.

■ **Operation flow**

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Setup" button.
3. Click "Write default" button.

Then set up the dialog and input data.

■ **Explanation of each buttons**

1. [Port Setup] :   Set up the printer port.
2. [Write default] : Initialize the register of AK4122.
3. [All Read] :   Read the all register of AK4122.
4. [Function1] :   Dialog to write data by keyboard operation.
5. [Write] :   Dialog to write data by mouse operation.
6. [Read] :   Read each register data by mouse operation.

■ **Explanation of each dialog**

1. [Function1 Dialog] :   Dialog to write data by keyboard operation

   Address Box: Input register address in 2 figures of hexadecimal.
   Data Box: Input register data in 2 figures of hexadecimal.

   If you want to write the input data to AK4122, click "OK" button. If not, click "Cancel" button.

2. [Write Dialog] : Dialog to write data by mouse operation

   There are dialogs corresponding to each register.

   Click the "Write" button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "1". If not, "L" or "0".

   If you want to write the input data to AK4122, click "OK" button. If not, click "Cancel" button.

■ **Indication of data**

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

MEASUREMENT RESULTS

[Measurement condition]
- Measurement unit   : Audio Precision, System Two Cascade
- Power Supply   : AVDD = DVDD = 3.3V
- Band width   : 10Hz ~ FSO/2
- Temperature   : Room
- Measurement Path   : AK4122 PORT1 → SRC → AK4122 PORT3

[Measurement Result]

SRC Characteristics	Result	Unit
THD+N (Input = 1kHz, 0dBFS)		
FSO/FSI = 44.1kHz/48kHz	113.6	dB
FSO/FSI = 48kHz/44.1kHz	113.3	dB
FSO/FSI = 32kHz/48kHz	114.0	dB
FSO/FSI = 96kHz/32kHz	113.3	dB
Worst Case (FSO/FSI = 48kHz/8kHz)	111.6	dB
Dynamic Range (Input = 1kHz, −60dBFS)		
FSO/FSI = 44.1kHz/48kHz	115.0	dB
FSO/FSI = 48kHz/44.1kHz	115.1	dB
FSO/FSI = 32kHz/48kHz	115.0	dB
FSO/FSI = 96kHz/32kHz	115.1	dB
Worst Case (FSO/FSI = 32kHz/44.1kHz)	115.0	dB
Dynamic Range (Input = 1kHz, −60dBFS, A-weighted)		
FSO/FSI = 44.1kHz/48kHz	117.2	dB

[Plot]

AKM   AK4122 THD+N vs. Input Level
                  AVDD=DVDD=3.3V, FSI=44.1kHz, FSO=48kHz, fin=1kHz
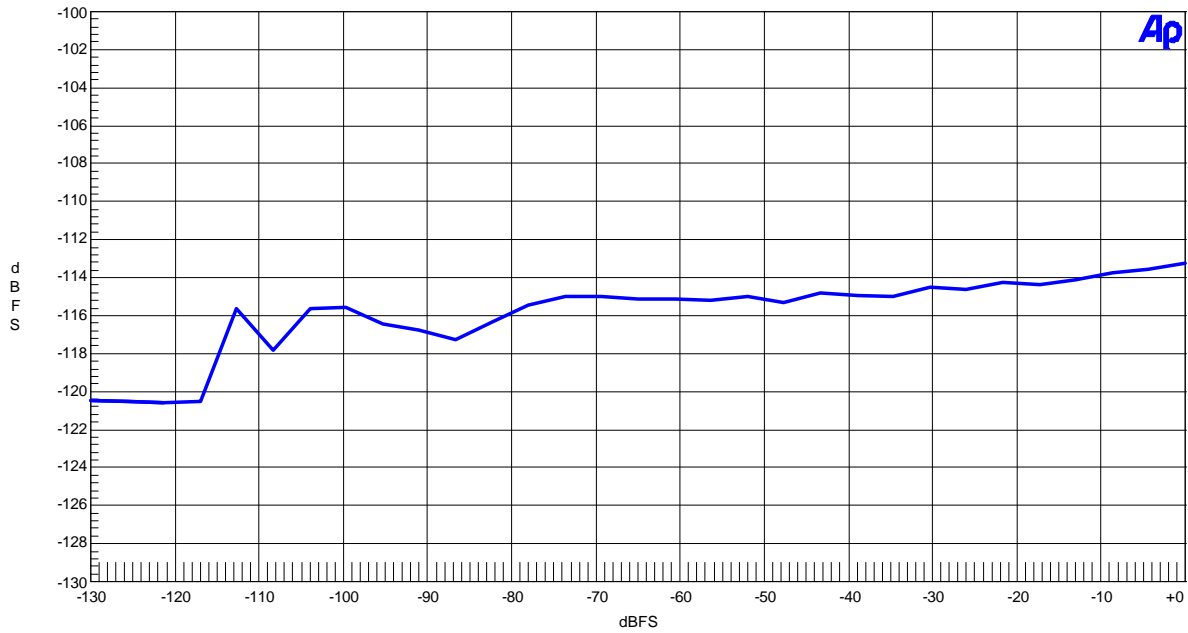
Fig 1. THD+N vs. Input Level

AKM   AK4122 THD+N vs. Input Frequency
                  AVDD=DVDD=3.3V, FSI=44.1kHz, FSO=48kHz, Input=0dBFS
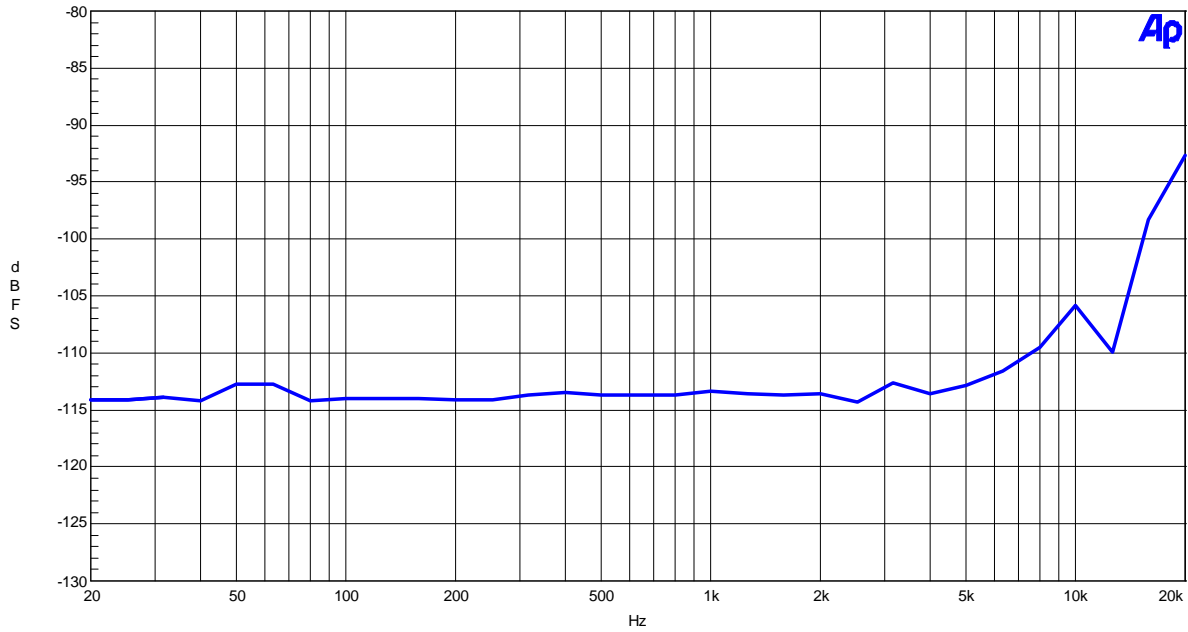
Fig 2. THD+N vs. Input Frequency (Input = 0dBFS)

AKM   AK4122 THD+N vs. Input Frequency
                    AVDD=DVDD=3.3V, FSI=44.1kHz, FSO=48kHz, Input=-60dBFS
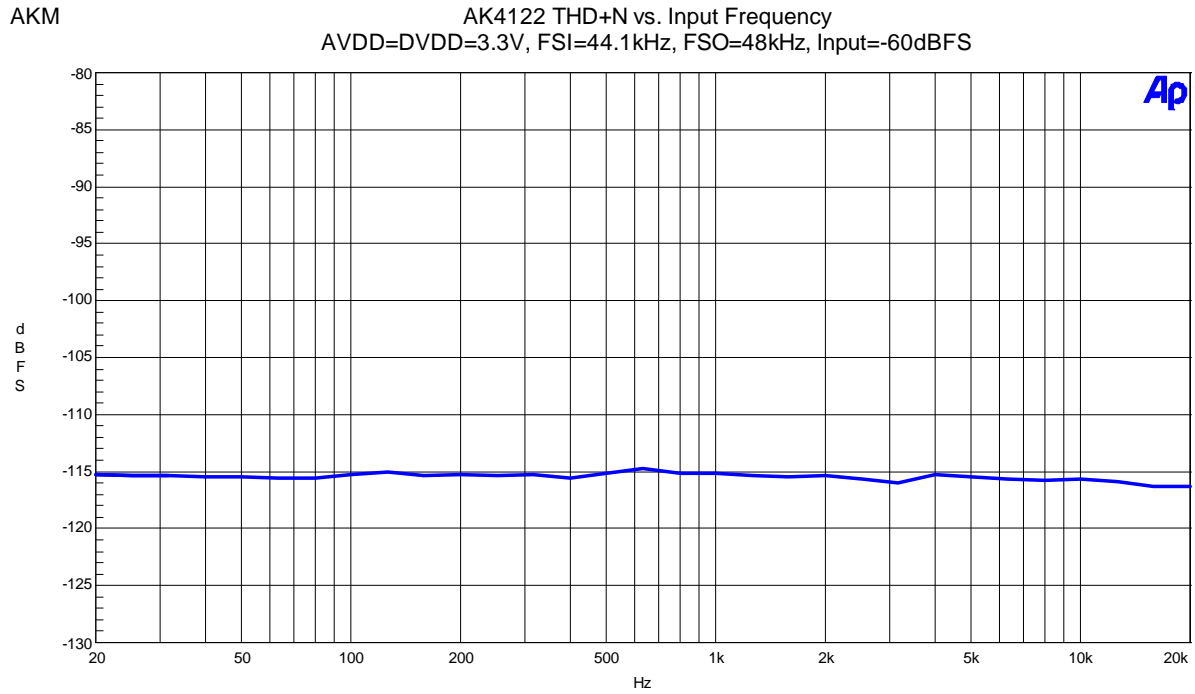
Fig 3. THD+N vs. Input Frequency (Input = -60dBFS)

AKM   AK4122 Linearity
                    AVDD=DVDD=3.3V, FSI=44.1kHz, FSO=48kHz, fin=1kHz

Fig 4. Linearity

AKM

AK4122 Frequency Response
AVDD=DVDD=3.3V, FSI=44.1kHz, FSO=48kHz, Input=0dBFS

Fig 5. Frequency Response

AKM

AK4122 FFT Plot
AVDD=DVDD=3.3V, FSI=44.1kHz, FSO=48kHz, Input=0dBFS, fin=1kHz
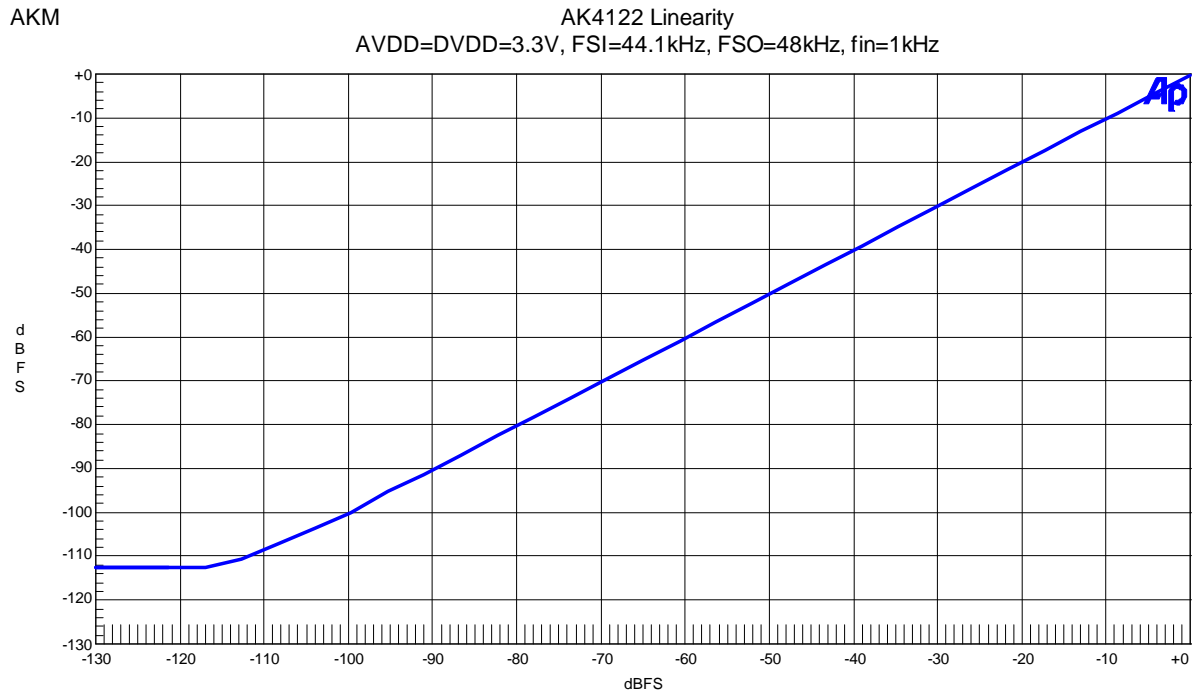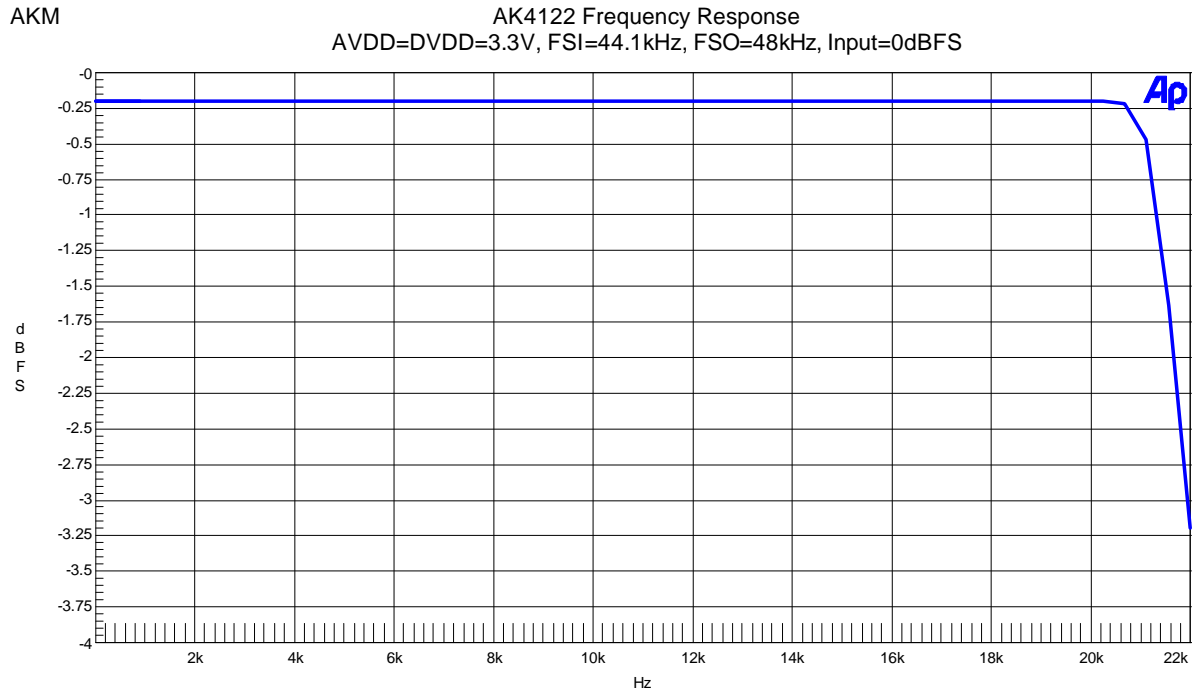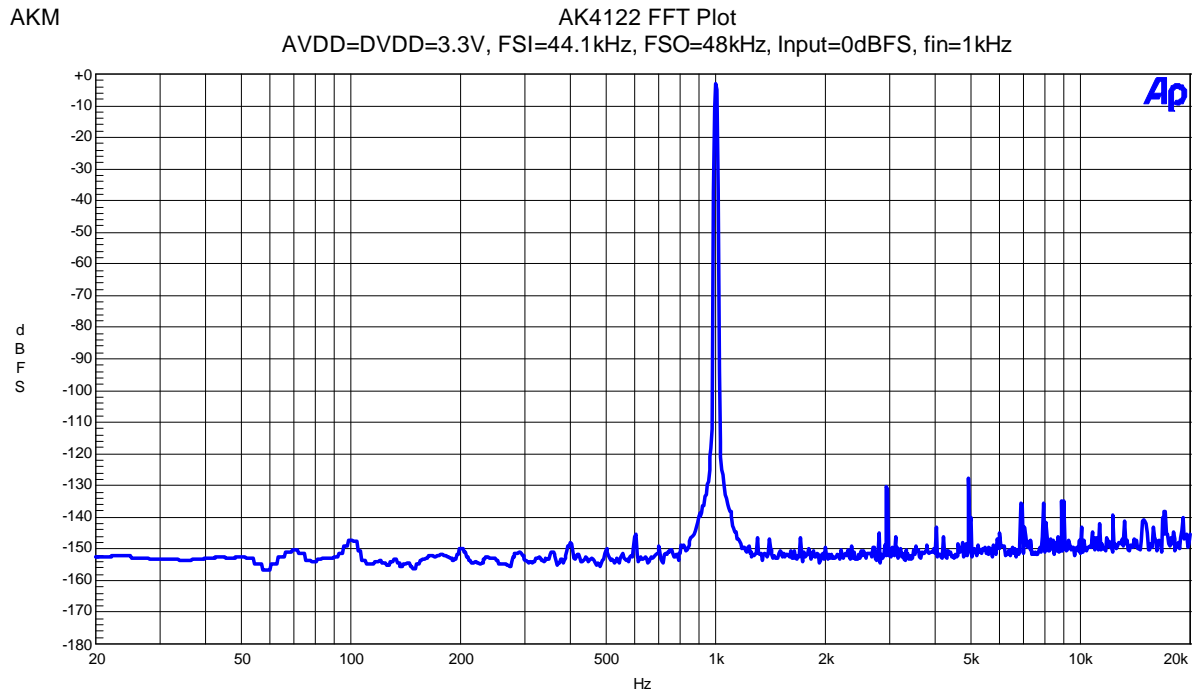
Fig 6. FFT Plot (Input = 0dBFS)

AKM

AK4122 FFT Plot
AVDD=DVDD=3.3V, FSI=44.1kHz, FSO=48kHz, Input=-60dBFS, fin=1kHz
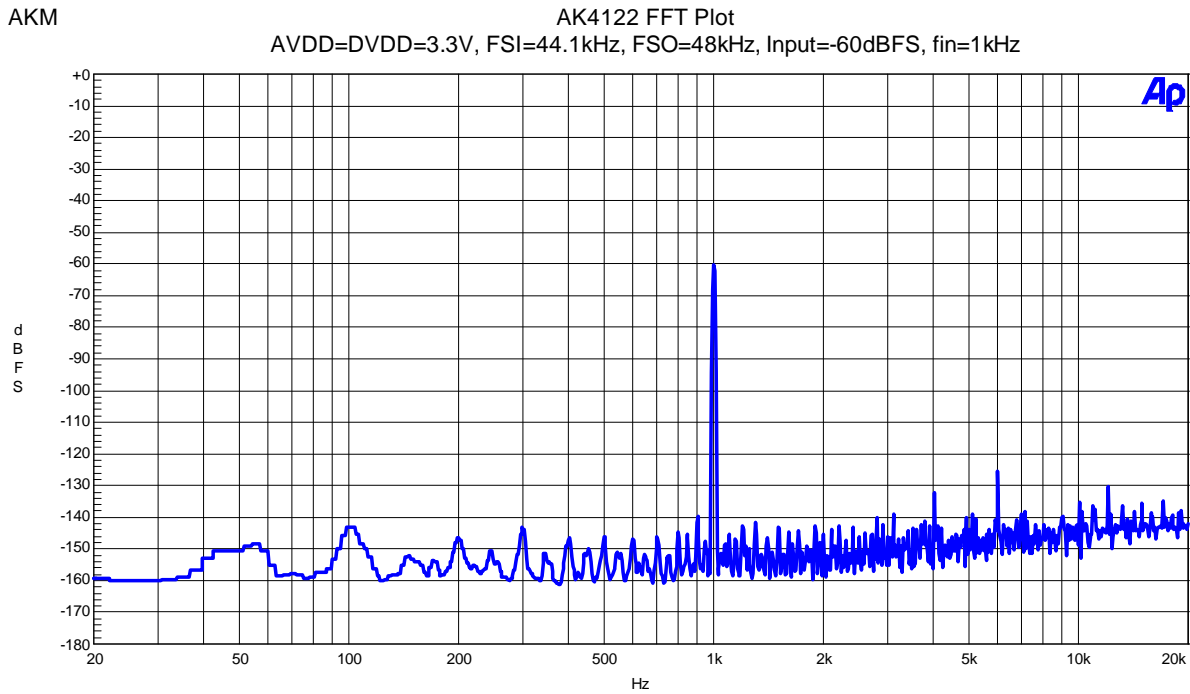
Fig 7. FFT Plot (Input = -60dBFS)

IMPORTANT NOTICE

AK4122

CN1
CN2
CN3
CN4

U1 74LVC541

U2 AK4122

SW1 AK4122

PORT1 CTRL
PORT2 TX
PORT3 DIR

For AK4122 PORT2

For AK4122 PORT3

AK4114

U12

Left pins:
- 1 IPS0
- 2 NC
- 3 DIF0 — PORT1_DIF0
- 4 TEST2
- 5 DIF1 — PORT1_DIF1
- 6 NC
- 7 DIF2 — PORT1_DIF2
- 8 IPS1
- 9 P/SN
- 10 XTL0
- 11 XTL1
- 12 VIN

Top pins:
- 48 RX3
- 47 NC
- 46 RX2
- 45 TEST1
- 44 RX1
- 43 NC
- 42 RX0
- 41 AVSS
- 40 VCOM
- 39 R
- 38 AVDD
- 37 INT1

Right pins:
- 36 INT0
- 35 OCKS0
- 34 OCKS1 — PORT1_OCKS1
- 33 CM1
- 32 CM0
- 31 PDN — 4114_PDN1
- 30 XTI
- 29 XTO
- 28 DAUX
- 27 MCKO2
- 26 BICK
- 25 SDTO

Bottom pins:
- 13 TVDD
- 14 DVSS
- 15 TX0
- 16 TX1
- 17 BOUT
- 18 COUT
- 19 UOUT
- 20 VOUT
- 21 DVDD
- 22 DVSS
- 23 MCKO1
- 24 LRCK

PORT4
VCC 3
GND 2
OUT 1
DIR1

L2 47u
C15 0.1u
C14 10u
C16 0.1u
C17 0.47u
R28 470
R29 18k

VCC

D3 HSU119
R63 10k
U7E 74HC14
U7D 74HC14
4114_PDN1
SW7 PDN1
C61 0.1u

U7C 74HC14
R30 1k
LED1 ERF

BICK1
R31 100
R32 100
R33 100
LRCK1
SDTI
R34 220k
R35 220k
R36 220k

PORT5
BICK1
LRCK1
SDTI
DSP1

U7B 74HC14
U7A 74HC14
J4 EXT1
EXT
R37 51
JP11 BICK1
DIR
JP12 EXT1

JP13 SDTO
JP14 LRCK1

VCC
SW2
OCKS 1
DIF0 2
DIF1 3
DIF2 4
PORT1

R71 47K — PORT1_OCKS1
R72 47K — PORT1_DIF0
R73 47K — PORT1_DIF1
R74 47K — PORT1_DIF2

C18 0.1u
C20 10u
C19 0.1u
C21 10u

U7F 74HC14

Title	AKD4122	
Size A3	Document Number PORT1	Rev A
Date: Tuesday, January 07, 2003	Sheet 3 of 6	

VCC

C33
10u

C34
0.1u

C35
0.47u

R49
18k

VCC

D5
HSU119

R65
10k

SW9
PDN3

C63
0.1u

U15A
74HC14

U15B
74HC14

4114_PDN3

TST1

TST

JP25
TST

OMCK

U14

Pin	Name
48	RX3
47	NC
46	RX2
45	TEST1
44	RX1
43	NC
42	RX0
41	AVSS
40	VCOM
39	R
38	AVDD
37	INT1

1 IPS0
2 NC
3 DIF0   PORT3_DIF0
4 TEST2
5 DIF1   PORT3_DIF1
6 NC
7 DIF2
8 IPS1
9 P/SN
10 XTL0
11 XTL1
12 VIN

AK4114

36 INT0
35 OCKS0
34 OCKS1   PORT3_OCKS1
33 CM1
32 CM0
31 PDN   4114_PDN3
30 XTI
29 XTO
28 DAUX
27 MCKO2
26 BICK
25 SDTO

C36 (open)
X2
24.576MHz
C37 (open)

OMCLK

R50
100

BICK

R51
100

LRCK

R52
100

SDTO

R53
100

PORT9
OMCLK	1	10
BICK	2	9
LRCK	3	8
SDTO	4	7
	5	6

DSP3

R54 R55 R56 R57
220k 220k 220k 220k

13 TVDD
14 DVSS
15 TX0
16 TX1
17 BOUT
18 COUT
19 UOUT
20 VOUT
21 DVDD
22 DVSS
23 MCKO1
24 LRCK

C38
0.1u
C40
10u

C39
0.1u
C41
10u

DIT
JP19
BICK
EXT   EXT_BICK3

DIT
JP20
LRCK
EXT   EXT_LRCK3

DIT
JP21
OMCLK
EXT   EXT_MCLK3

PORT10
3 IN
2 VCC
1 GND
C42
0.1u
DIT3

SW4   VCC
OCKS 1   4
DIF0 2   3
PORT3

R66   47K
R67   47K
PORT3_OCKS1
PORT3_DIF0

Title block
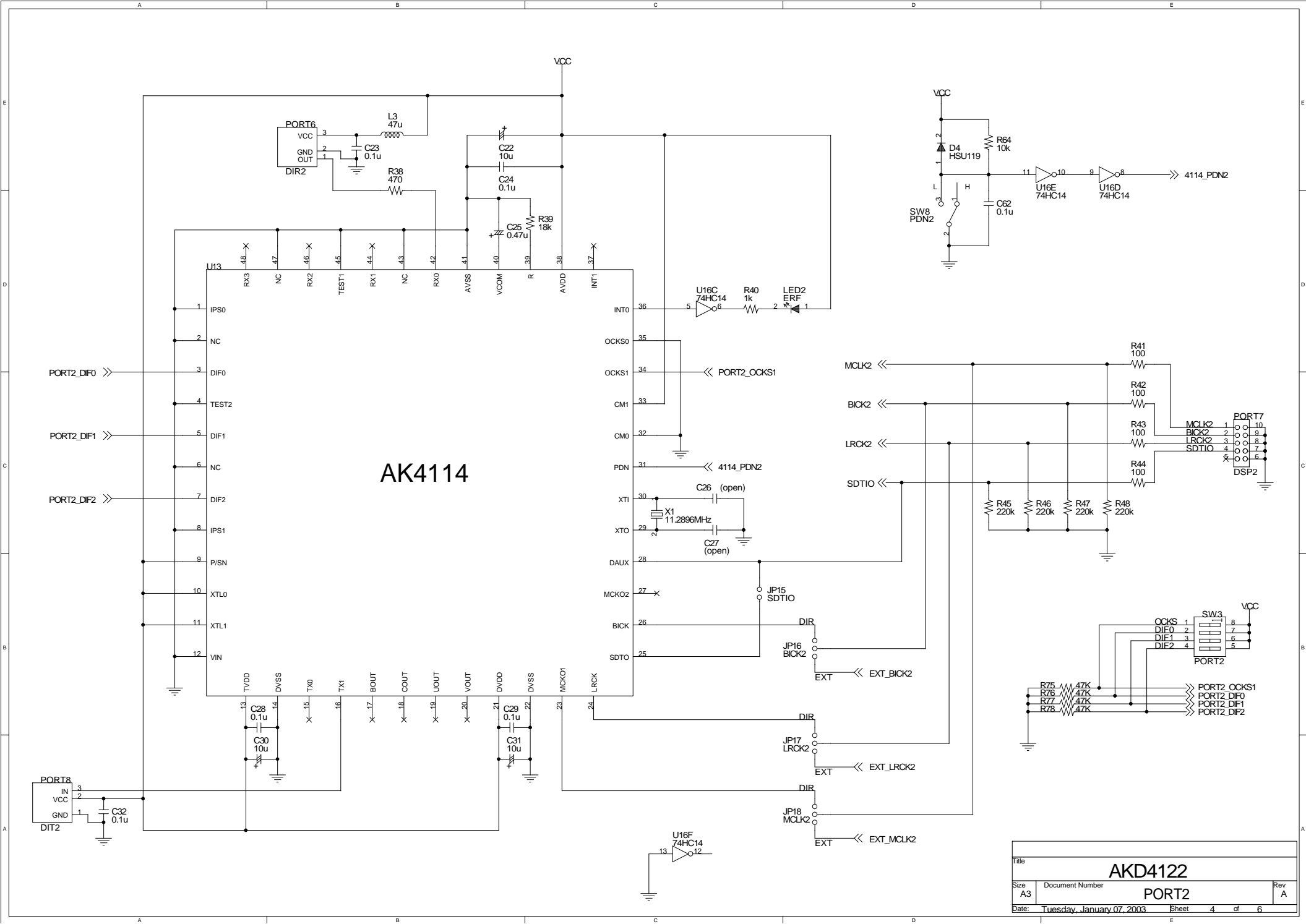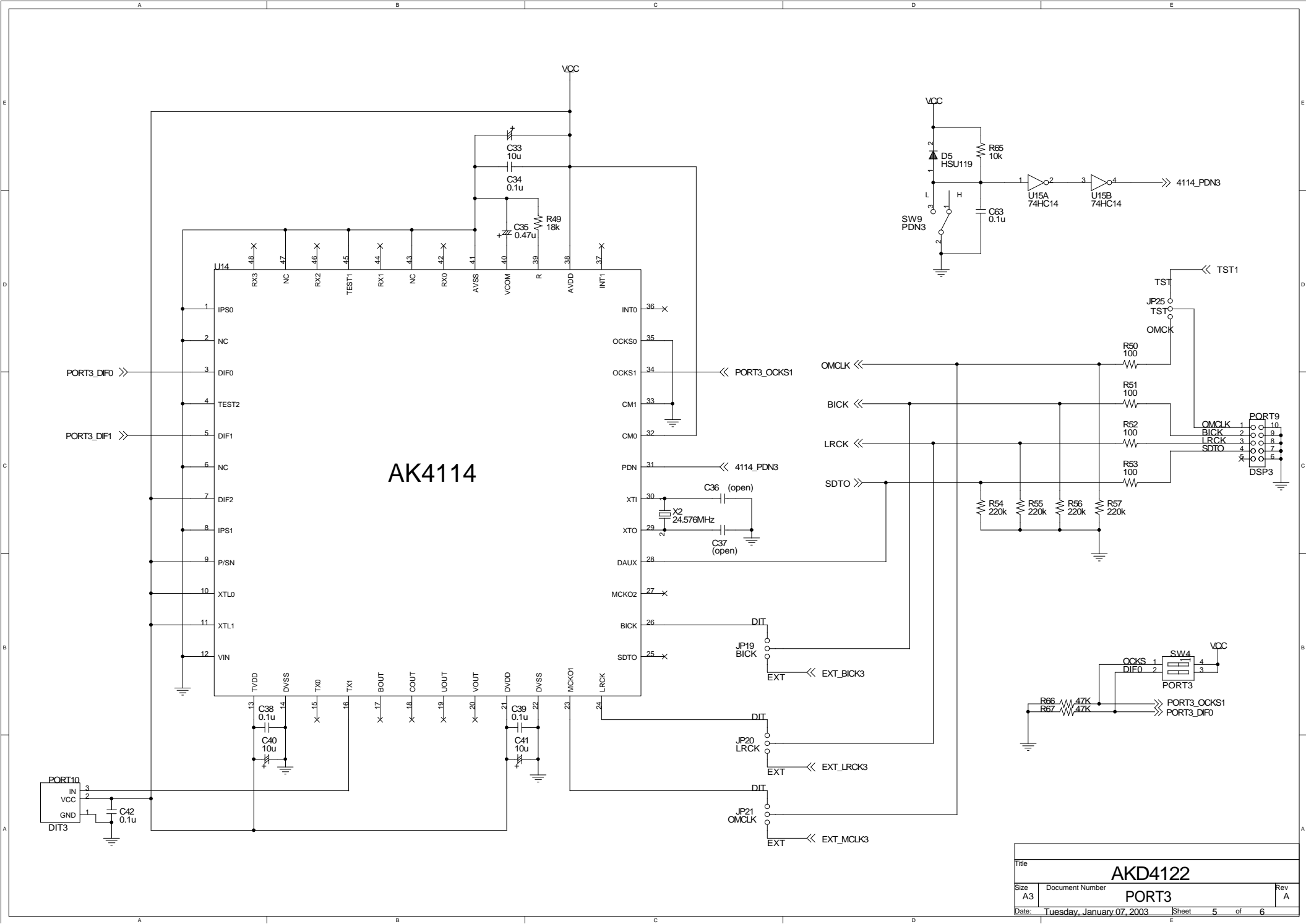
Title
AKD4122
Size A3
Document Number
PORT3
Rev A
Date: Tuesday, January 07, 2003
Sheet 5 of 6

VCC

D1
HSU119

R58
10k

SW5
SMUTE

C43
0.1u
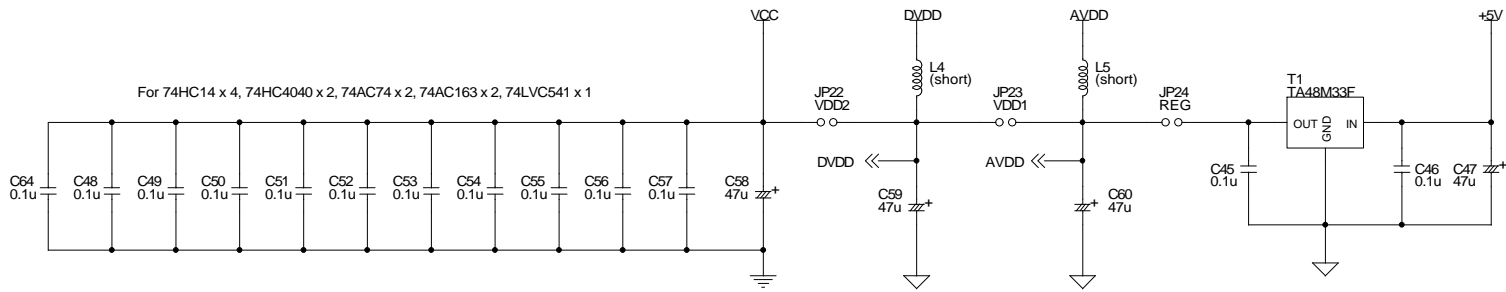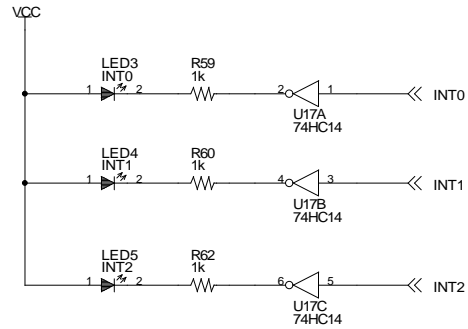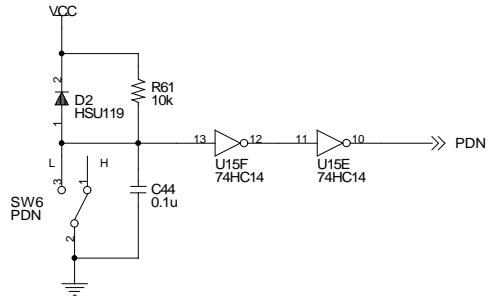
5 6
U15C
74HC14

9 8
U15D
74HC14

SMUTE

VCC

LED3
INT0

R59
1k

2 1
U17A
74HC14

INT0

LED4
INT1

R60
1k

4 3
U17B
74HC14

INT1

LED5
INT2

R62
1k

6 5
U17C
74HC14

INT2

VCC

D2
HSU119

R61
10k

SW6
PDN

C44
0.1u

13 12
U15F
74HC14

11 10
U15E
74HC14

PDN

For 74HC14 x 4, 74HC4040 x 2, 74AC74 x 2, 74AC163 x 2, 74LVC541 x 1

VCC

DVDD

L4
(short)

AVDD

L5
(short)

+5V

JP22
VDD2

JP23
VDD1

JP24
REG

T1
TA48M33F

OUT   IN
GND

C64
0.1u

C48
0.1u

C49
0.1u

C50
0.1u

C51
0.1u

C52
0.1u

C53
0.1u

C54
0.1u

C55
0.1u

C56
0.1u

C57
0.1u

C58
47u

DVDD

C59
47u

AVDD

C60
47u

C45
0.1u

C46
0.1u

C47
47u

U17D
74HC14
9 8

U17E
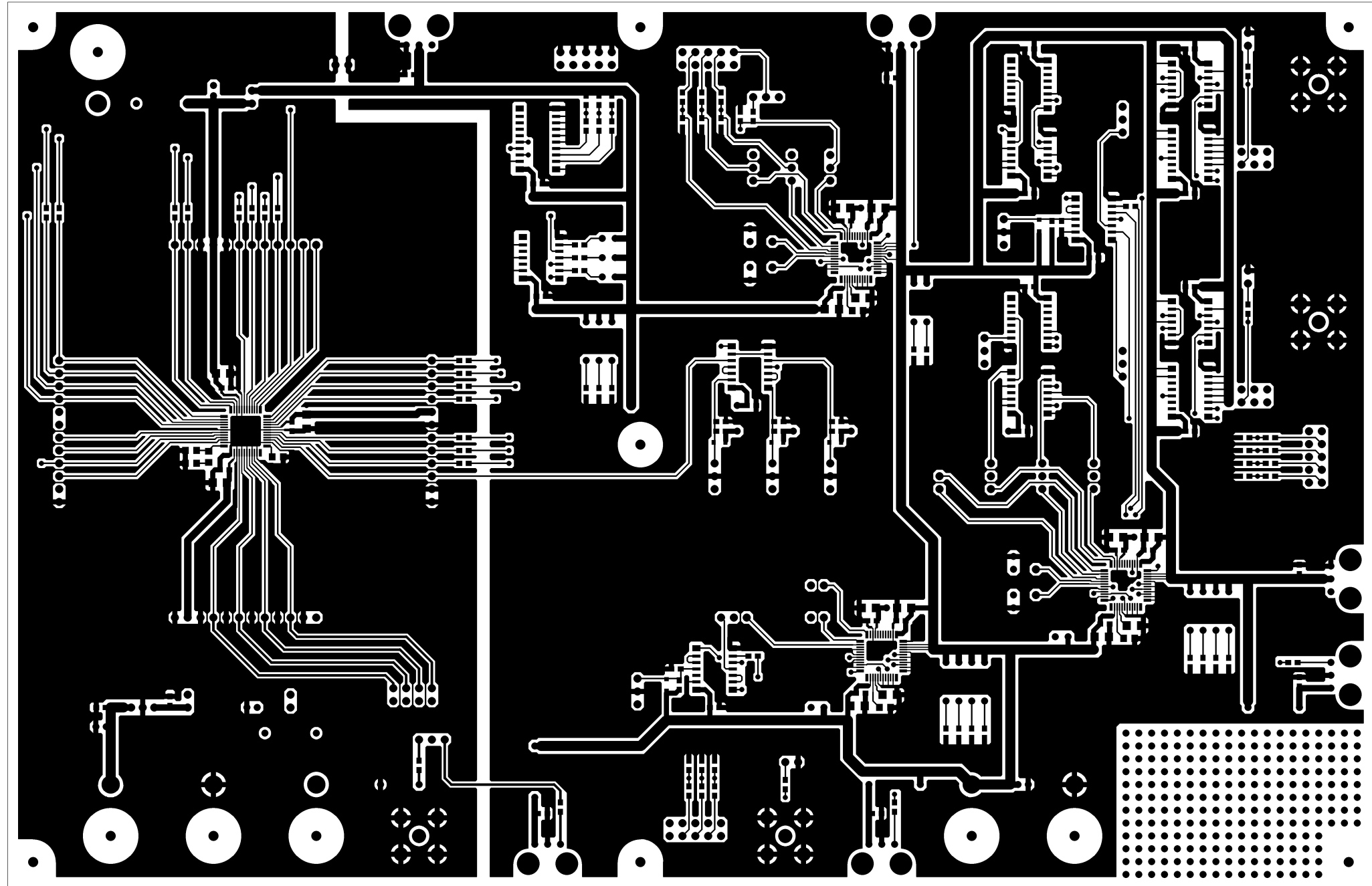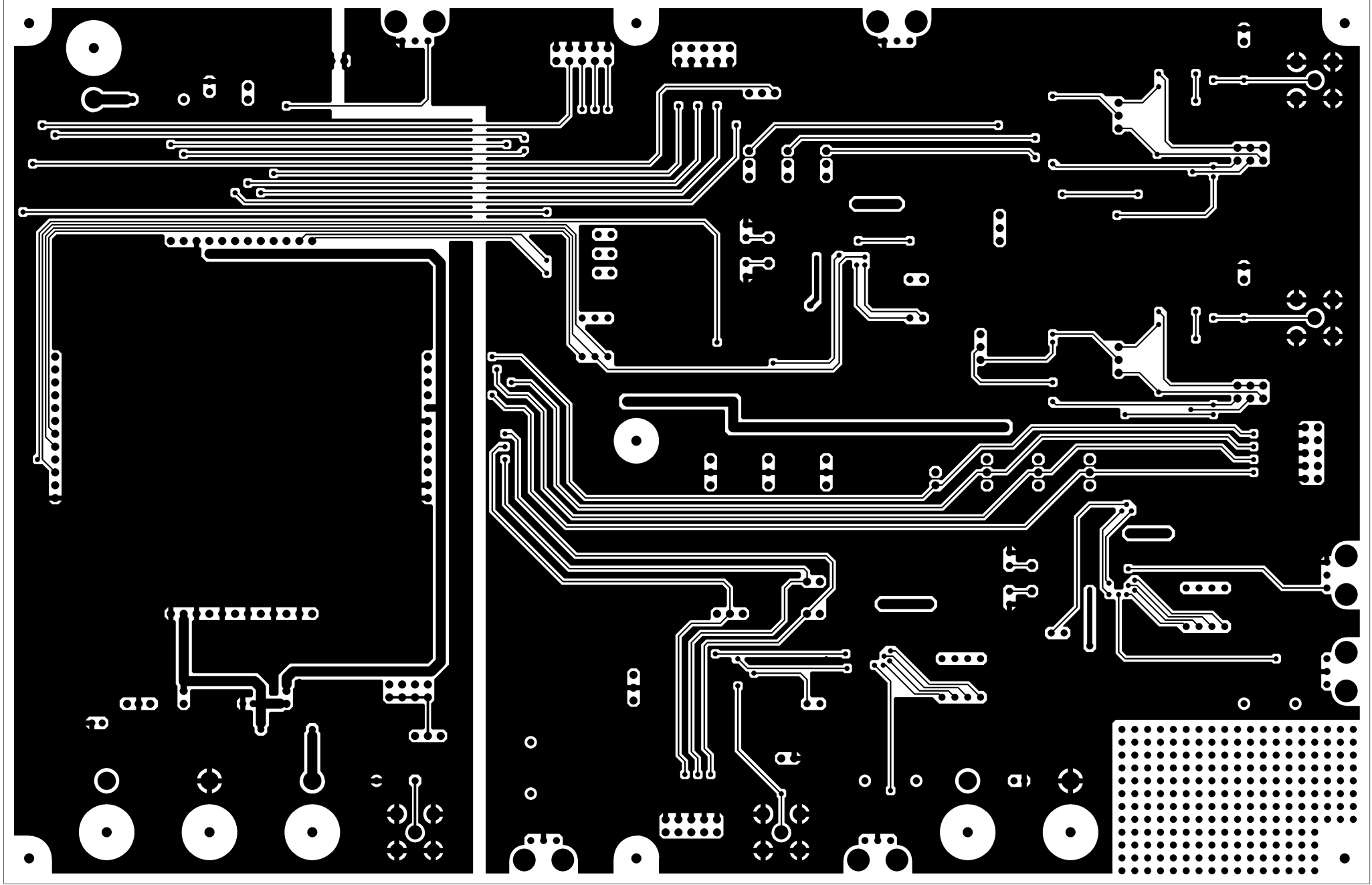74HC14
11 10

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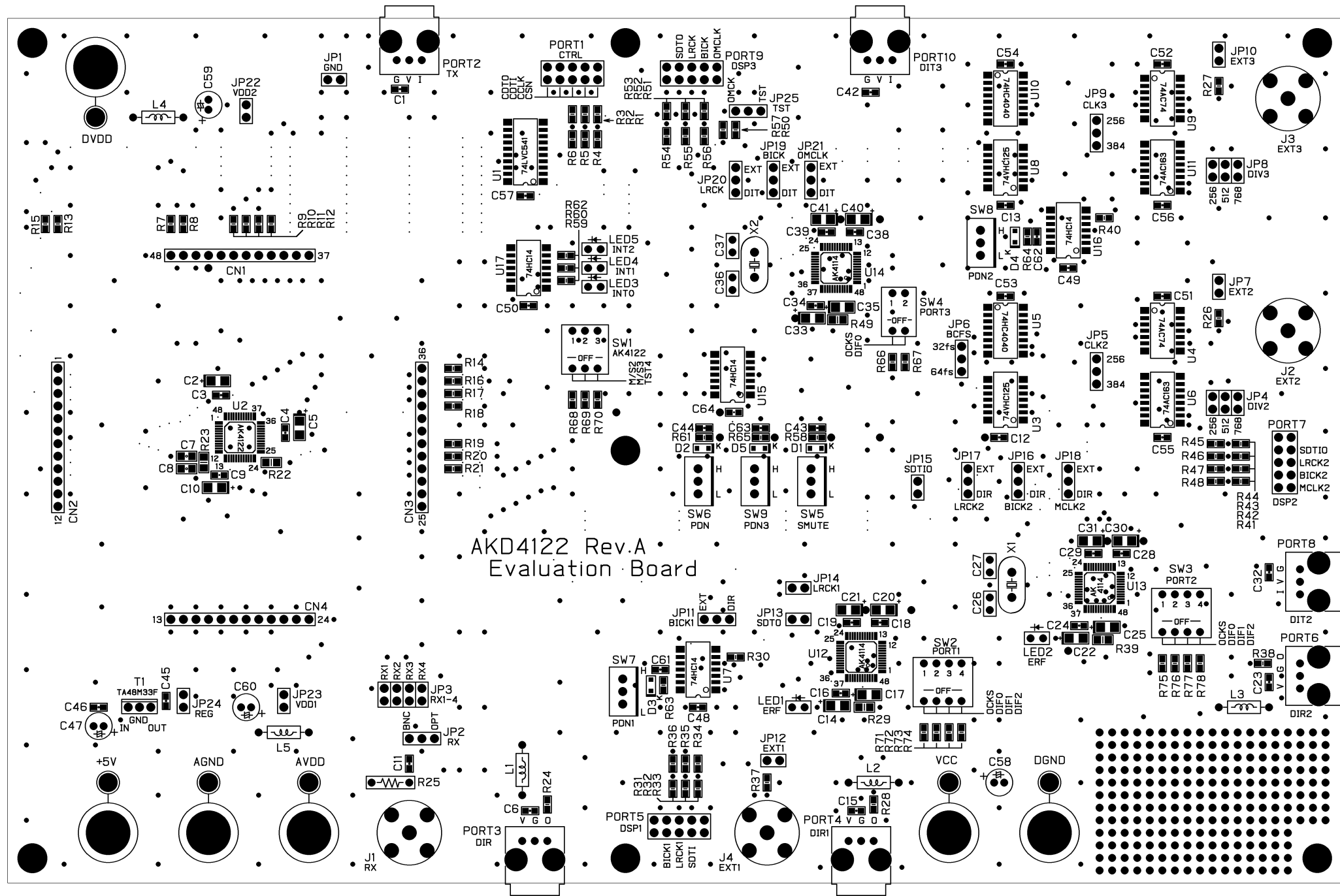
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AKD4122 Rev.A L2