AKD5385B-A
AK5385B Evaluation Board Rev.0

GENERAL DESCRIPTION

AKD5385B-A is an evaluation board for the digital audio 24bit 192kHz A/D converter, AK5385B. The AKD5385B-A includes the input circuit and also has a digital interface transmitter. Further, the AKD5385B-A can achieve the interface with digital audio systems via opt-connector.

■ **Ordering guide**

AKD5385B-A --- AK5385B Evaluation Board

FUNCTION

- **DIT with optical output**
- **BNC connector for an external clock input**

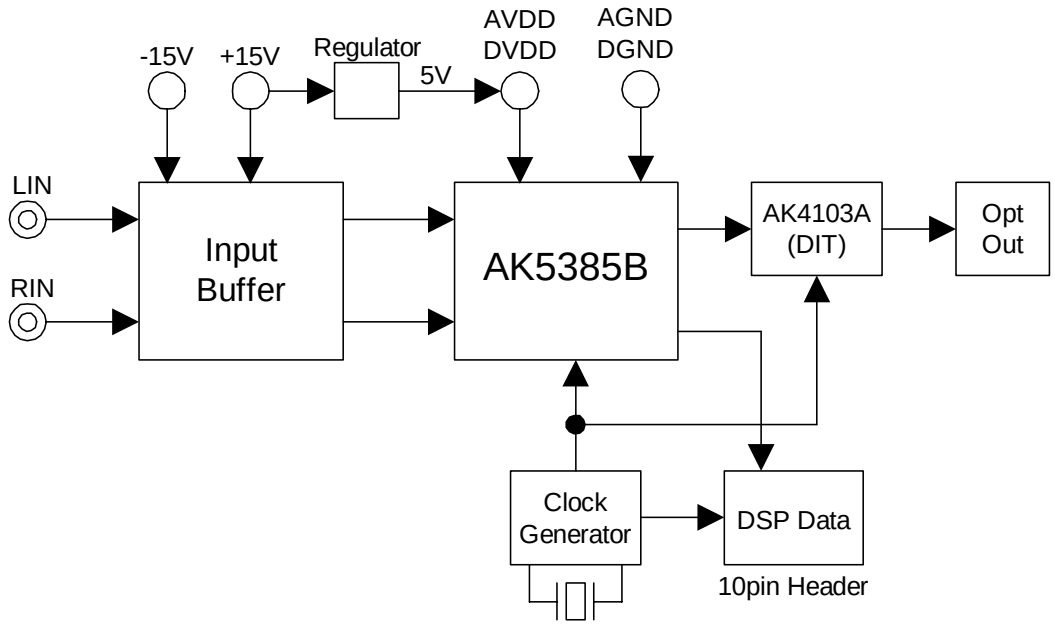


Figure 1. AKD5385B-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation sequence

1) Set up the power supplies lines.

[AVDD]	(red)	= 4.75 ~ 5.25V	: for AVDD of AK5385B (typ. 5.0V)
			(The default setting of JP2 is "REG", so AVDD connector should be open.
			In this case, the AVDD of AK5385B is supplied from regulator.)
[DVDD]	(red)	= 3.0 ~ 5.25V	: for DVDD of AK5385B (typ. 3.3V)
[+15V]	(green)	= +15V	: for Op-amp
[–15V]	(blue)	= –15V	: for Op-amp
[VCC]	(red)	= 5V	: for logic
[AGND]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

Each supply line should be distributed from the power supply unit.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.

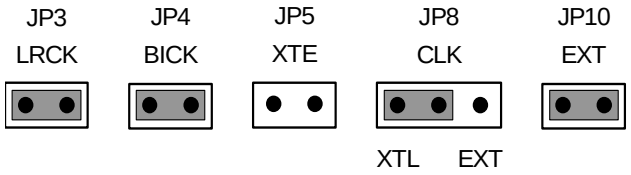
The AK5385B and AK4103A should be reset once bringing SW1 = "L" upon power-up.

■ Evaluation mode

(1) Slave Mode

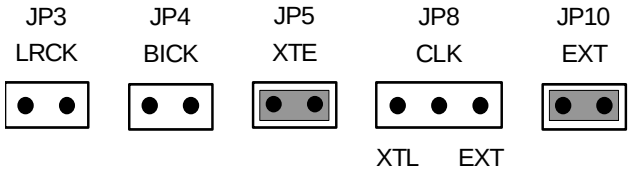
(1-1) A/D evaluation using DIT function of AK4103A

PORT1 (DIT) is used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX176). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier which equips DIR input. Nothing should be connected to PORT2 (DSP). In case of using external clock through a BNC connector (J3), select EXT on JP8 (CLK) and short JP5 (XTE) and open JP10 (EXT).



(1-2) Feeding all clocks from PORT2 (DSP)

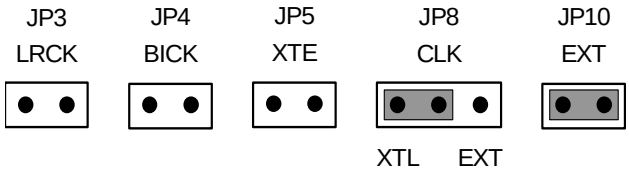
Under the following set-up, all external clocks (MCLK, BICK, LRCK) can be fed through PORT2 (DSP). The A/D converted data is output from SDTO of PORT2 (DSP). Also, the A/D converted data is output through optical connector (TOTX176).



(2) Master Mode

(2-1) A/D evaluation using DIT function of AK4103A

PORT1 (DIT) is used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX176). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier which equips DIR input. Nothing should be connected to PORT2 (DSP). In case of using external clock through a BNC connector (J3), select EXT on JP8 (CLK) and short JP5 (XTE) and open JP10 (EXT).



■ Other jumper pins set up

1. JP1 (GND) : Analog ground and Digital ground
   OPEN : Separated.
   SHORT : Common. (The connector "DGND" can be open.) <Default>

2. JP2 (AVDD) : Select AVDD for AK5385B
   AVDD : Supply from AVDD connector .
   REG : Supply from regulator. <Default>
   In this case, AVDD connector should be open.

3. JP6 (BCFS) : Select BICK frequency
   256 : In case of MCLK=256fs/512fs <Default>
   384 : In case of MCLK=128fs/384fs

4. JP7 (MCLK) : Supply MCLK frequency for 74HC4040
   256 : In case of MCLK=128fs/256fs
   512 : In case of MCLK=512fs <Default>
   384/768 : In case of MCLK=384fs

5. JP9 (LRFS) : Select LRCK frequency
   256 : In case of MCLK=256fs/512fs <Default>
   384 : In case of MCLK=128fs/384fs

■ Clock Setting

Mode	fs	MCLK	JP6(BCFS)	JP7(MCLK)	JP9(LRFS)	
Normal Speed	8kHz	256fs = 2.048MHz	256	256	256	
		384fs = 3.072MHz	384	384/768	384	
		512fs = 4.096MHz	256	512	256	
	32kHz	256fs = 8.192MHz	256	256	256	
		384fs = 12.288MHz	384	384/768	384	
		512fs = 16.384MHz	256	512	256	
	44.1kHz	256fs = 11.2896MHz	256	256	256	
		384fs = 16.9344MHz	384	384/768	384	
		512fs = 22.5792MHz	256	512	256	
	48kHz	256fs = 12.288MHz	256	256	256	
		384fs = 18.432MHz	384	384/768	384	
		512fs = 24.576MHz	256	512	256	Default
Double Speed	88.2kHz	256fs = 22.5792MHz	256	256	256	
		384fs = 33.8688MHz	384	384/768	384	
	96kHz	256fs = 24.576MHz	256	256	256	
		384fs = 36.864MHz	384	384/768	384	
Quad Speed	176.4kHz	128fs = 22.5792MHz	384	256	384	
	192kHz	128fs = 24.576MHz	384	256	384	

Table 1. Clock Setting

■ DIP Switch set up

[SW2] (MODE): Setting the evaluation mode for AK5385B and AK4103A
ON is "H", OFF is "L".

No.	Name	OFF ("L")	ON ("H")	Default
1	CKS0	See Table 3		OFF ("L")
2	CKS1			ON ("H")
3	DIF	MSB justified	I^2S Compatible	OFF ("L")
4	M/S	Slave mode	Master mode	OFF ("L")
5	DFS0	See Table 4		OFF ("L")
6	DFS1			OFF ("L")
7	HPFE	HPF Disable	HPF Enable	ON ("H")
8	DIT1	See Table 5		ON ("H")
9	DIT0			OFF ("L")
10	-	N/A	N/A	OFF ("L")

Table 2. Mode Setting

CKS1	CKS0	MCLK Frequency	
L	L	256fs	
L	H	128fs	
H	L	512fs	Default
H	H	384fs	

Table 3. MCLK Frequency

DFS1	DFS0	LRCK Frequency	
L	L	8kHz ≤ fs ≤ 54kHz	Default
L	H	54kHz < fs ≤ 108kHz	
H	L	108kHz < fs ≤ 216kHz	
H	H	N/A	

Table 4. Sampling Speed

Mode	DIT1	DIT0	MCLK	fs	
0	L	L	256fs	~ 108kHz	
1	L	H	128fs	~ 216kHz	
2	H	L	512fs	~ 54kHz	Default
3	H	H	384fs	~ 54kHz	

Table 5. MCLK Frequency Setting of AK4103A

■ The function of the toggle SW

Upper-side is "H" and lower-side is "L".

[SW1] (PDN): Resets the AK5385B and AK4103A. Keep "H" during normal operation.

■ Input Circuit

Analog signal is input to LIN/RIN pins via J1, J2 connectors.

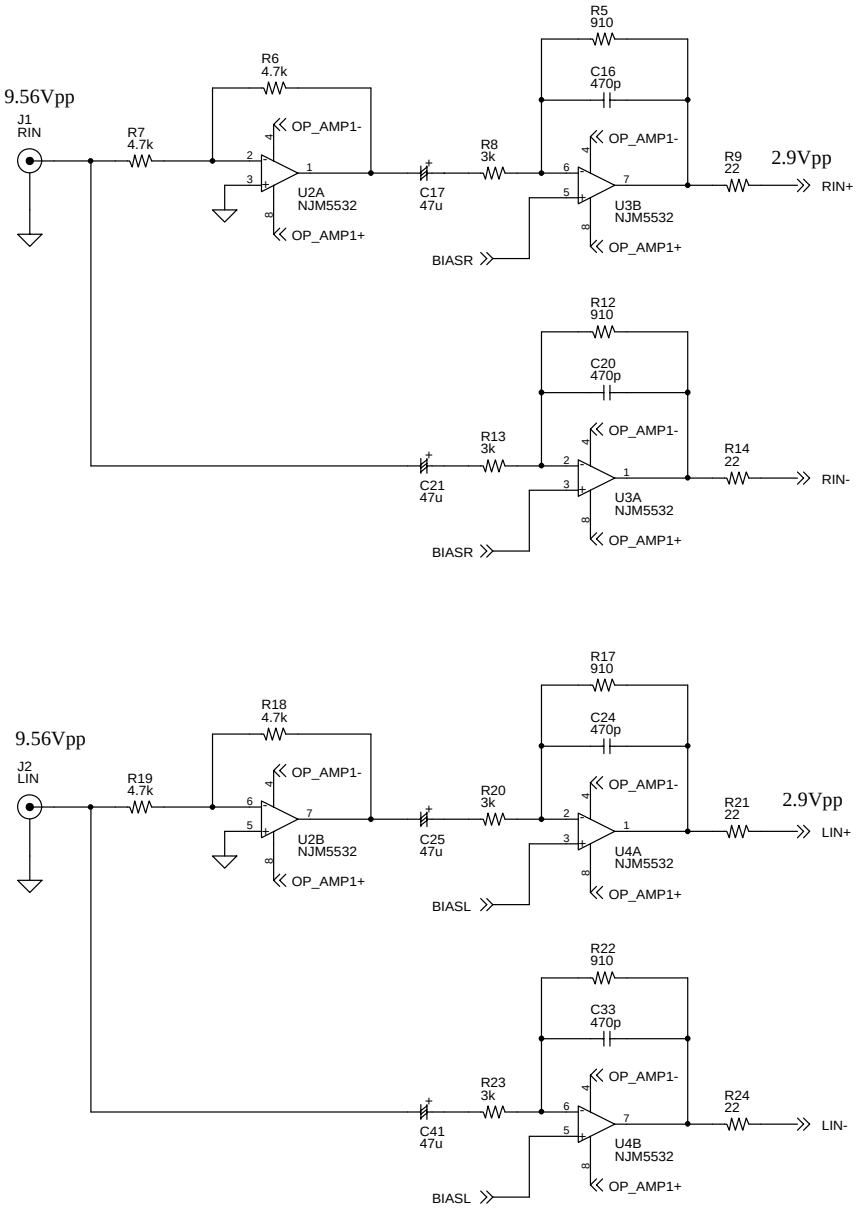


Figure 2. LIN/RIN Input circuits

* AKM assumes no responsibility for the trouble when using the circuit examples.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement Unit : Audio Precision, System Two Cascade
- MCLK : 512fs@fs=48kHz, 256fs@fs=96kHz, 128fs@fs=192kHz
- BICK : 64fs
- fs : 48kHz, 96kHz, 192kHz
- Band Width : 10Hz ~ 20kHz@fs=48kHz, 10Hz ~ 40kHz@fs=96kHz/192kHz
- Bit : 24bit
- Power Supply : AVDD = 5.0V, DVDD = 3.3V
- Interface : DIT@fs=48kHz/96kHz, Serial Port@fs=192kHz
- Temperature : Room

[Measurement Results]

Parameter	Result (Lch / Rch)	Unit
ADC Analog Input Characteristics:		
S/(N+D)		
(fs=48kHz, -1dBFS, BW=20kHz)	100.8 / 101.1	dB
(fs=48kHz, -1dBFS, BW=20kHz, VREFL,VREFR Cap=100uF) (Note1)	102.6 / 102.9	dB
(fs=96kHz, -1dBFS, BW=40kHz)	99.6 / 100.0	dB
(fs=192kHz, -1dBFS, BW=40kHz)	99.7 / 99.9	dB
D-Range		
(fs=48kHz, -60dBFS, A-weighted)	113.4 / 113.6	dB
(fs=96kHz, -60dBFS, BW=40kHz)	106.6 / 107.1	dB
(fs=192kHz, -60dBFS, BW=40kHz)	105.8 / 106.9	dB
S/N		
(fs=48kHz, A-weighted)	113.8 / 113.6	dB
(fs=96kHz, BW=40kHz)	106.4 / 107.1	dB
(fs=192kHz, BW=40kHz)	106.3 / 107.0	dB
Interchannel Isolation		
(fs=48kHz)	127.6 / 123.2	dB
(fs=96kHz)	116.5 / 127.6	dB
(fs=192kHz)	114.5 / 126.4	dB

(Note1) 10uF is mounted on the VREFL and VREFR pins on the evaluation board.

[ADC Plot : fs=48kHz]

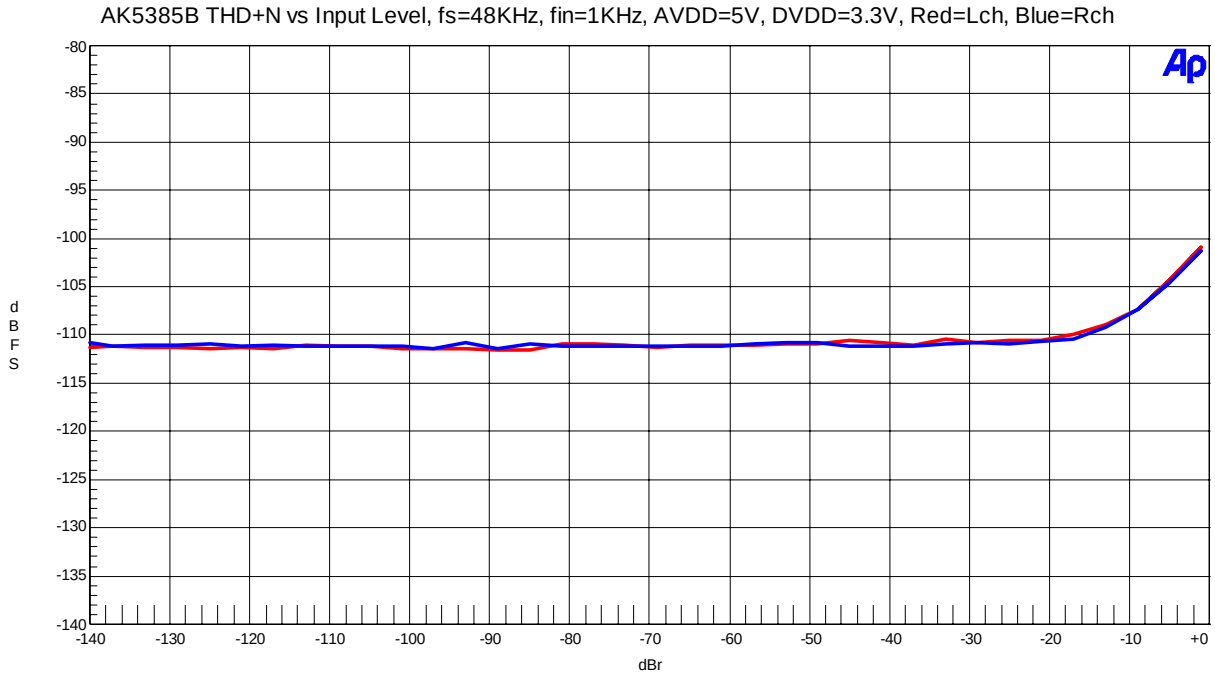


Figure 1. THD+N vs. Input Level

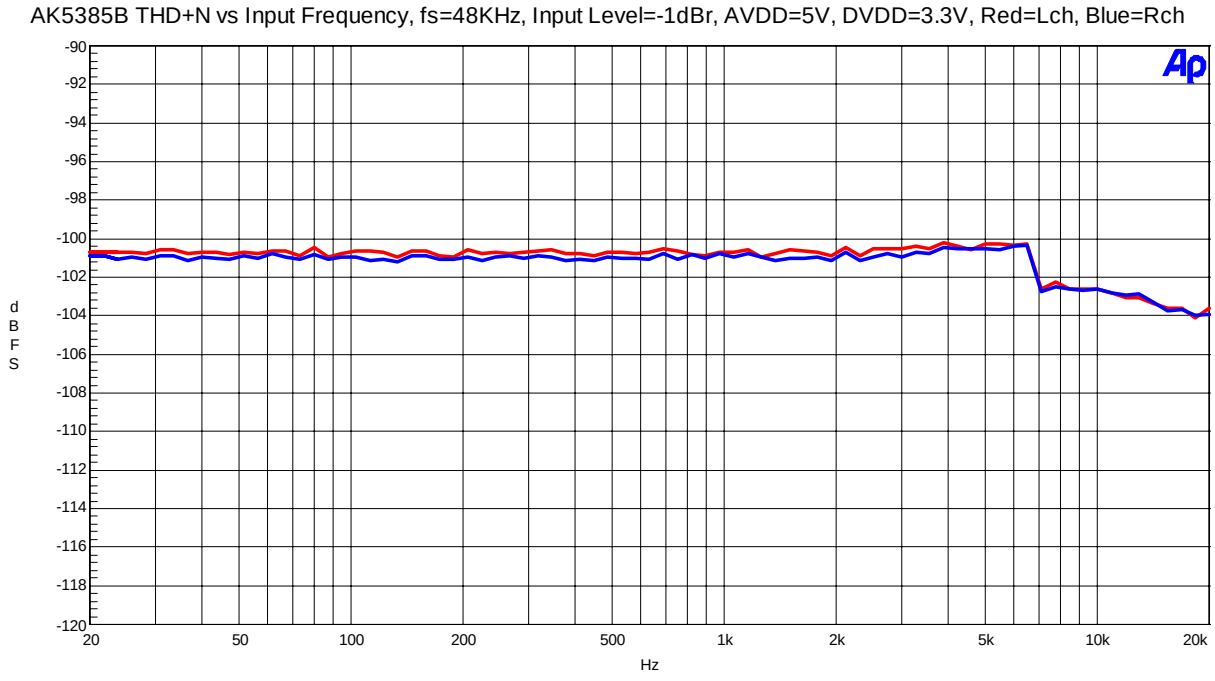


Figure 2. THD+N vs. Input Frequency

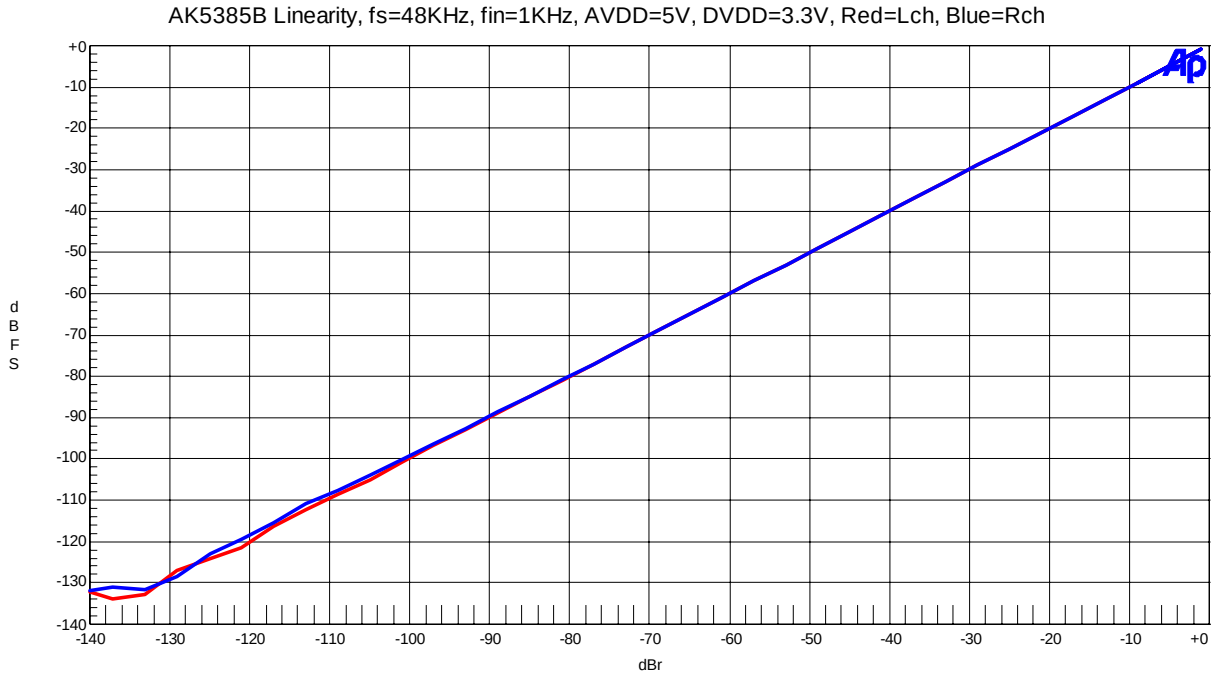


Figure 3. Linearity

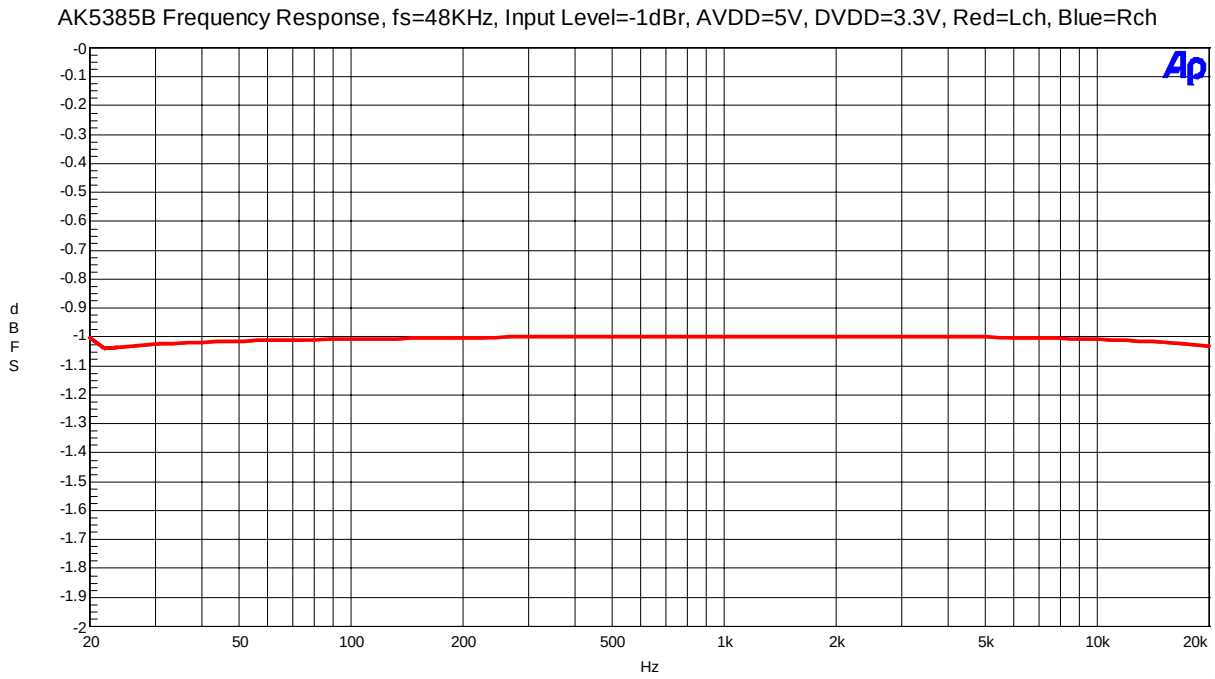


Figure 4. Frequency Response

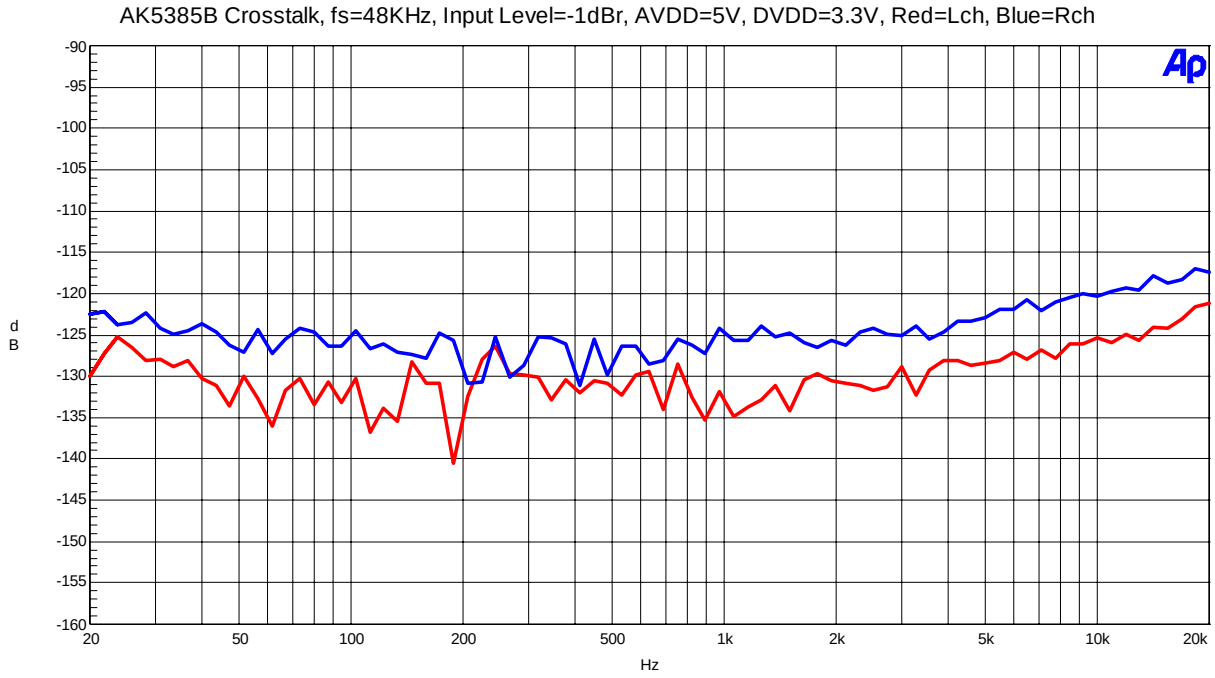


Figure 5. Crosstalk

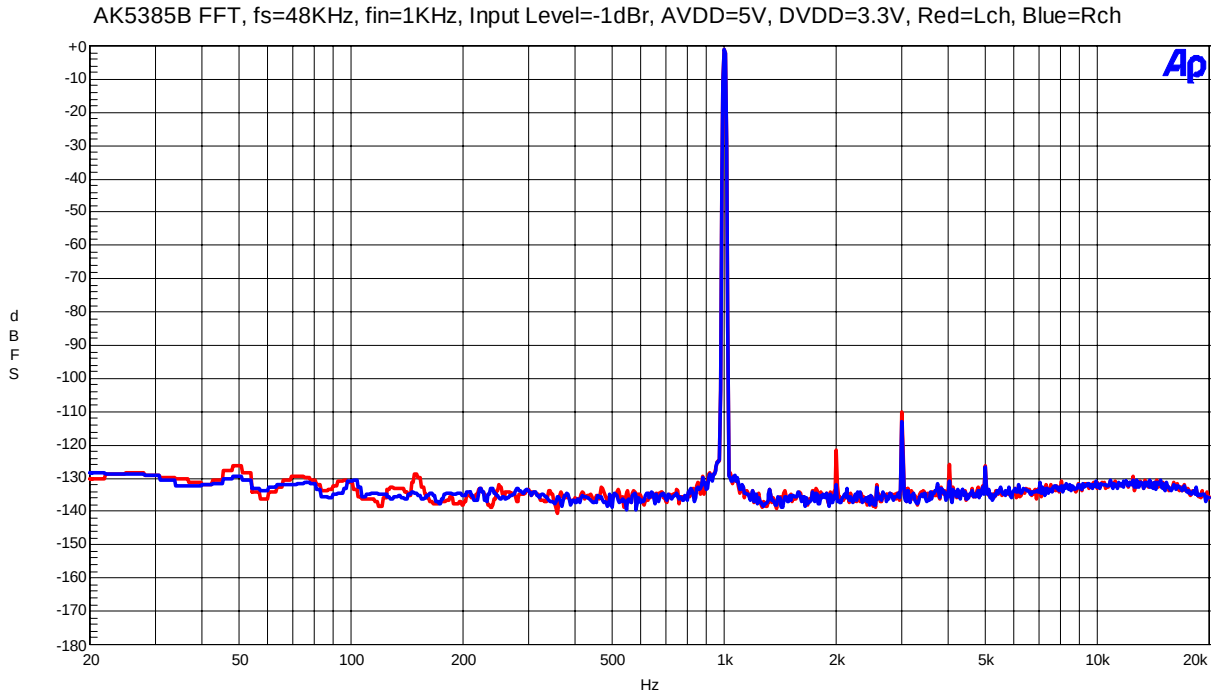


Figure 6. FFT Plot (Input=-1dBr)

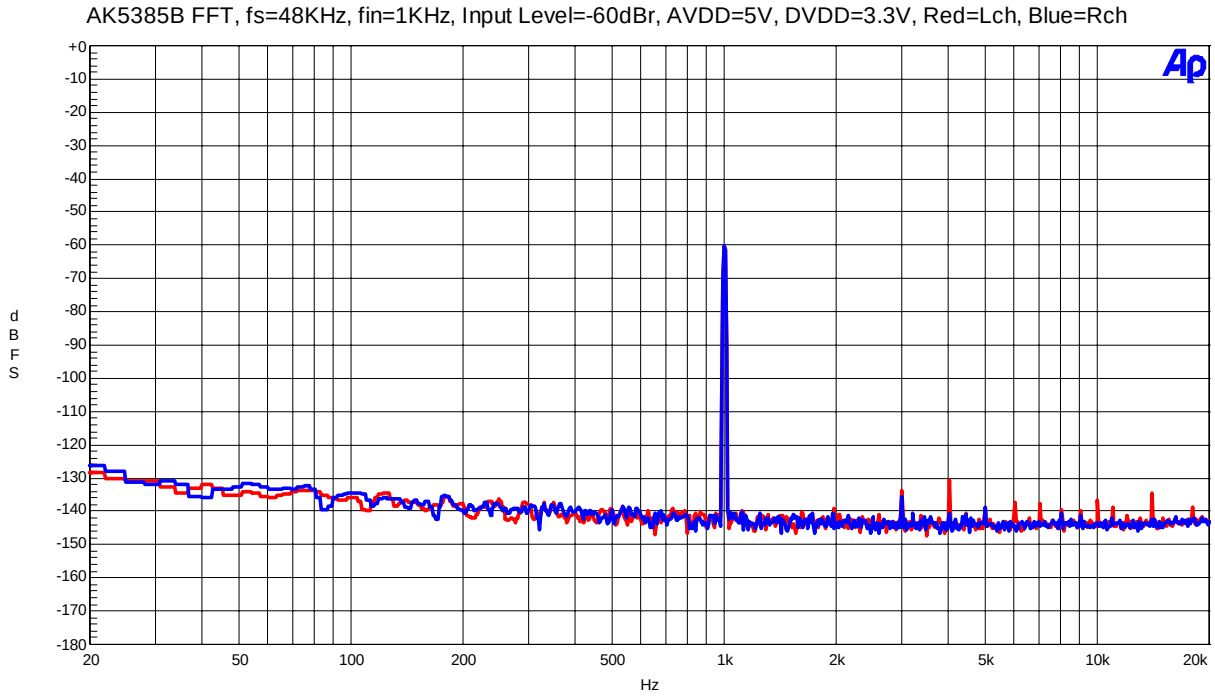


Figure 7. FFT Plot(Input=-60dBr)

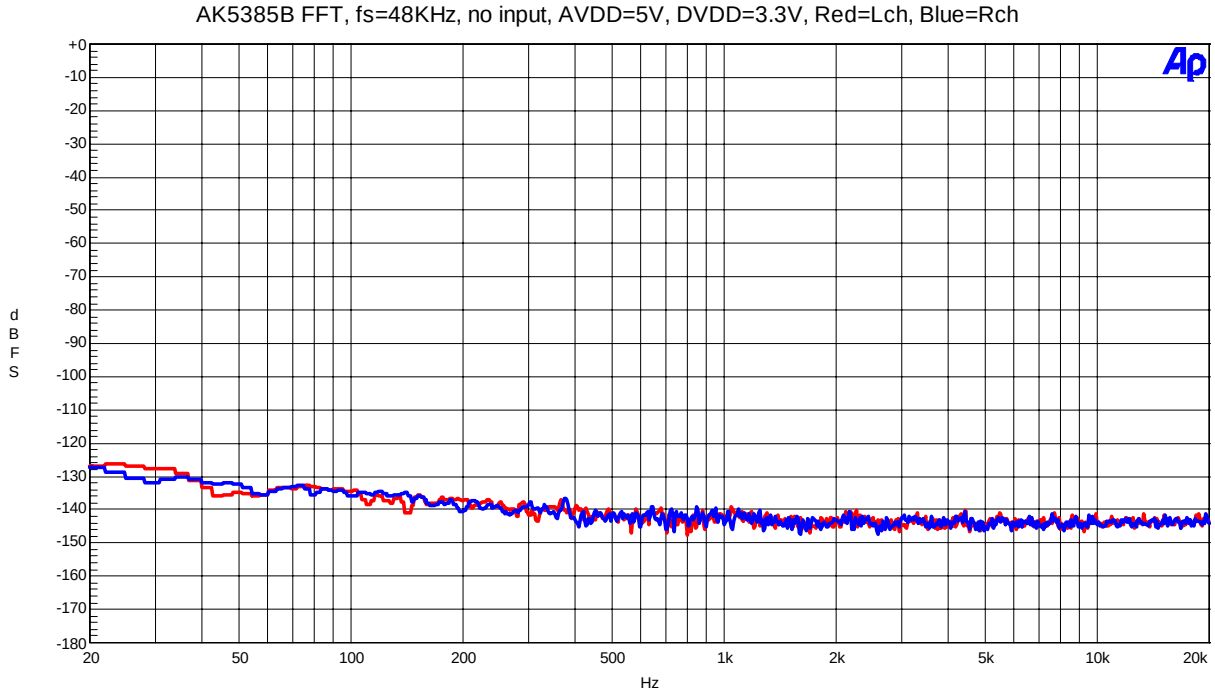


Figure 8. FFT Plot (no input)

[ADC Plot : fs=96kHz]

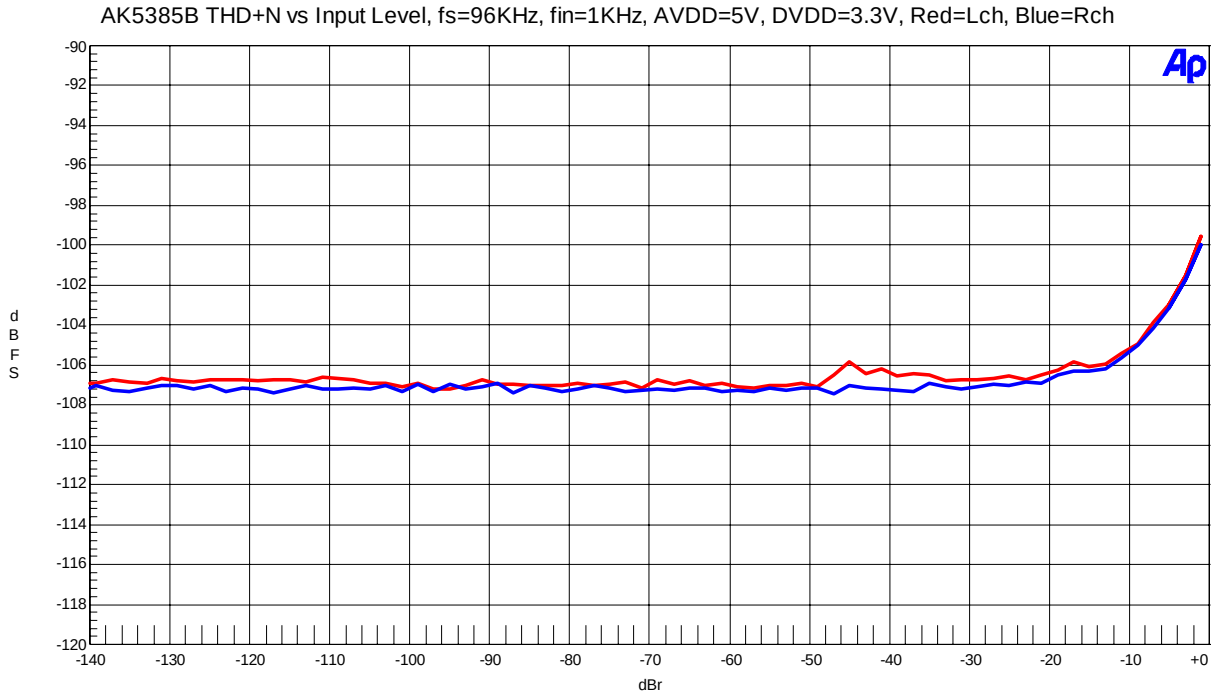


Figure 9. THD+N vs. Input Level

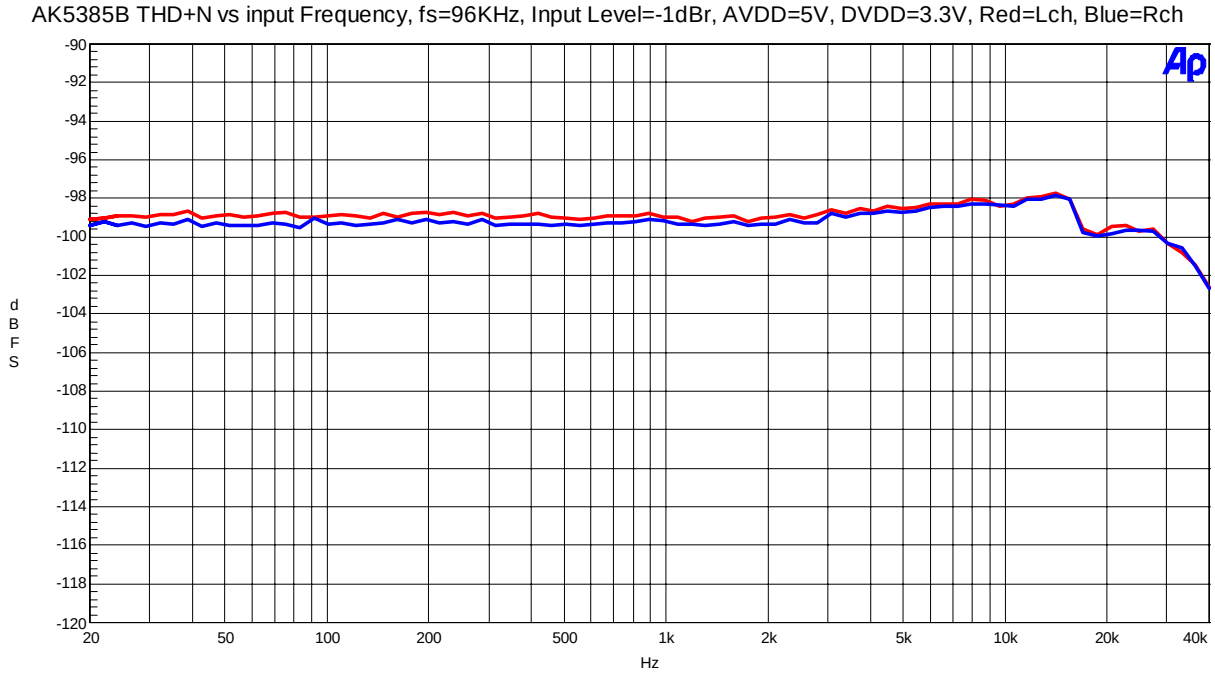


Figure 10. THD+N vs. Input Frequency

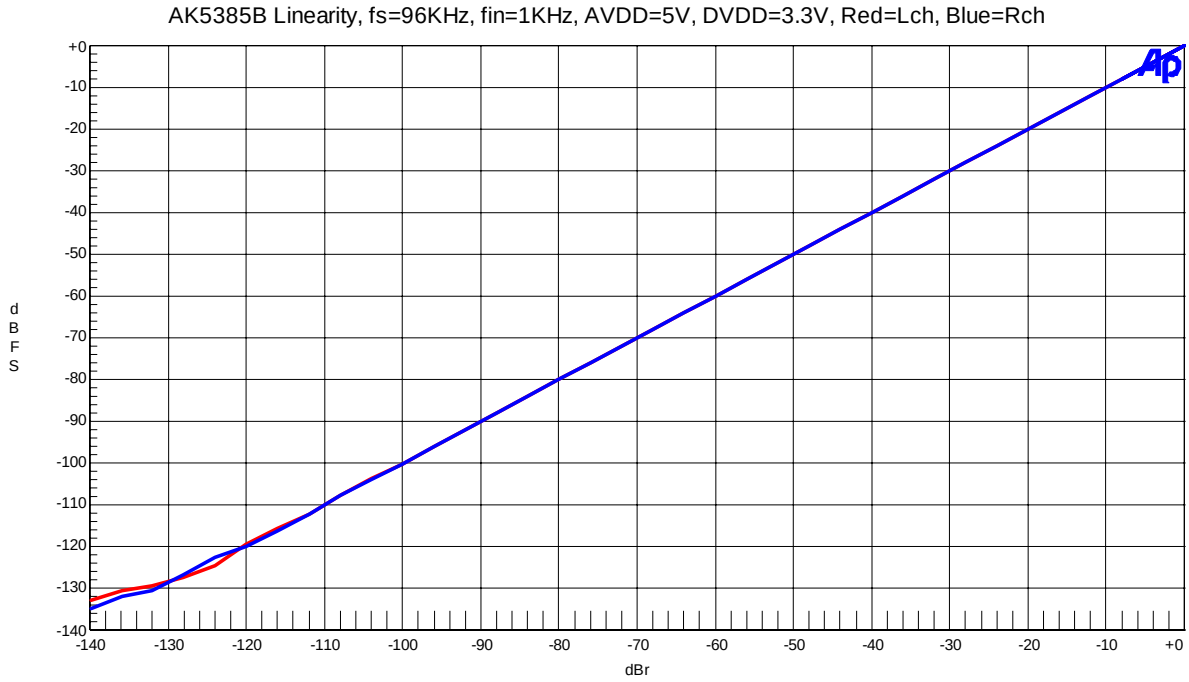


Figure 11. Linearity

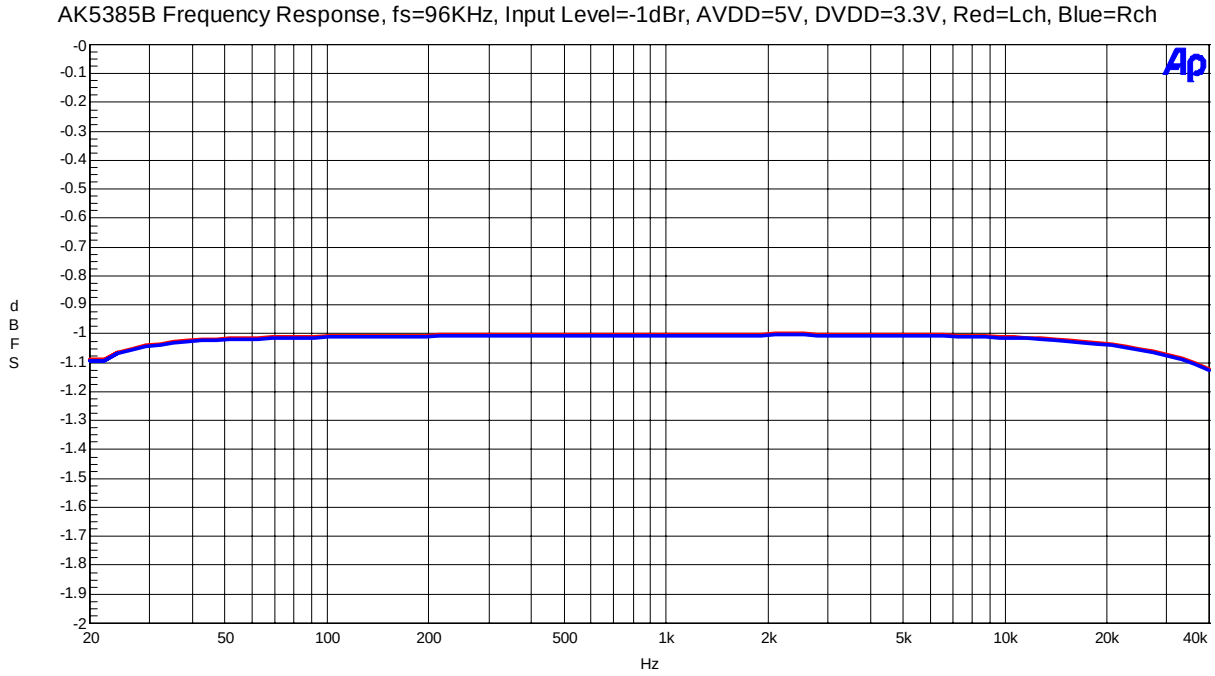


Figure 12. Frequency Response

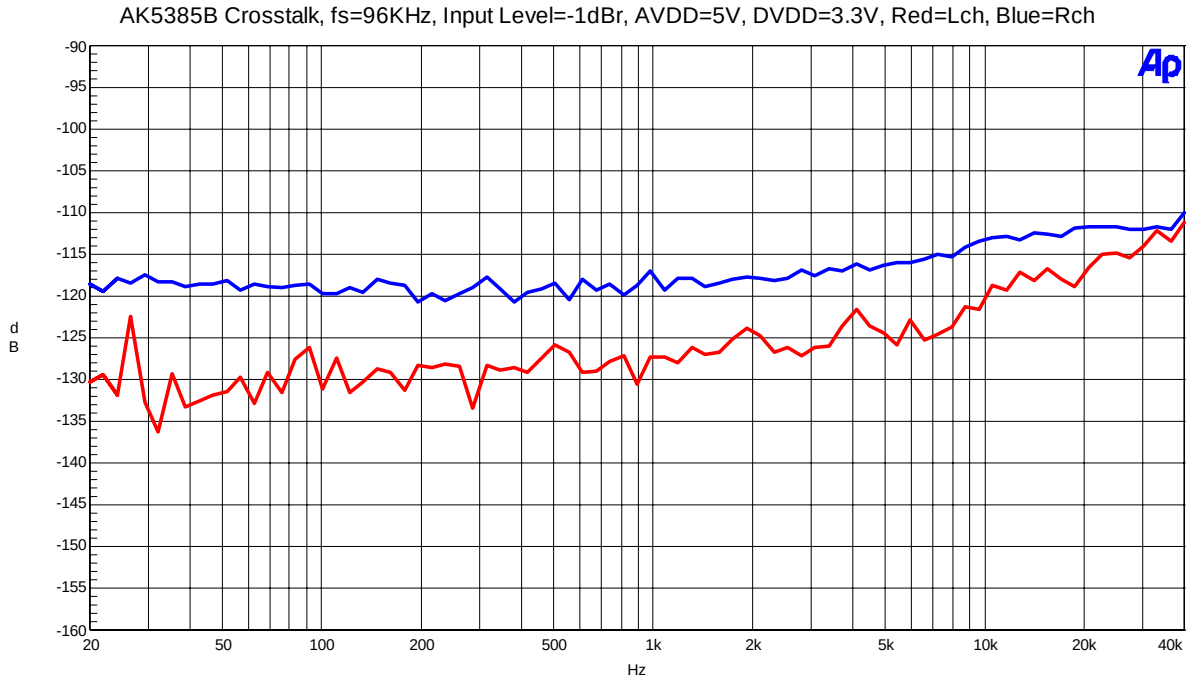


Figure 13. Crosstalk

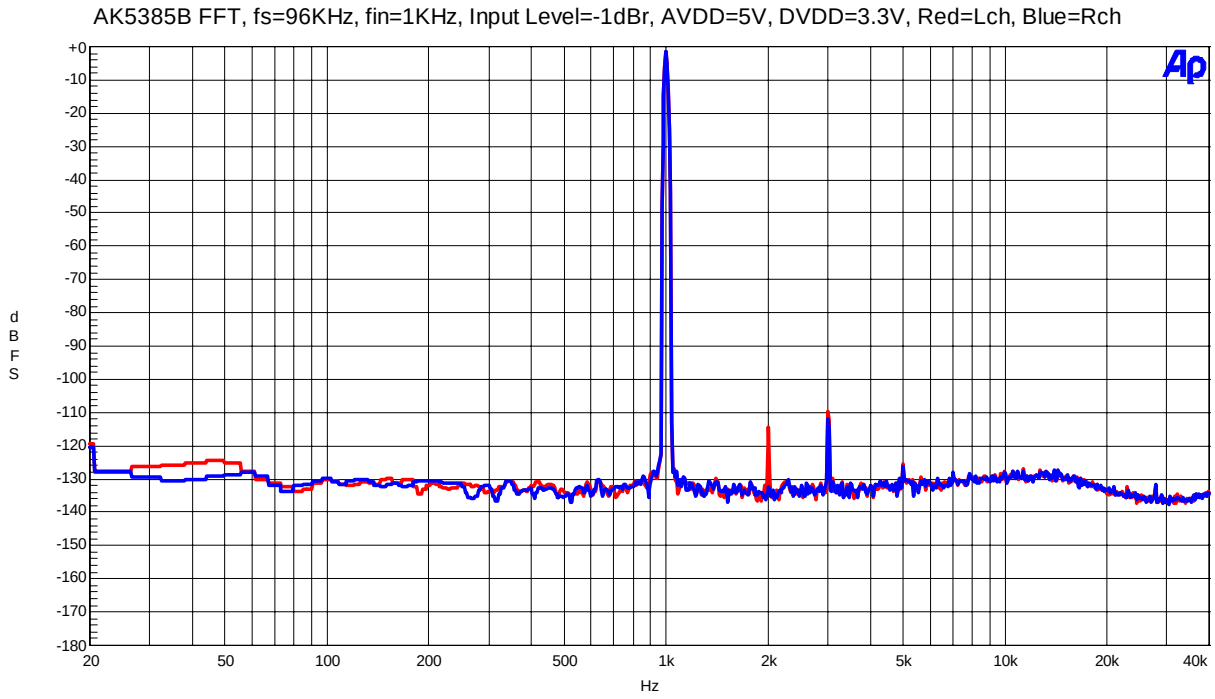


Figure 14. FFT Plot (Input=-1dBr)

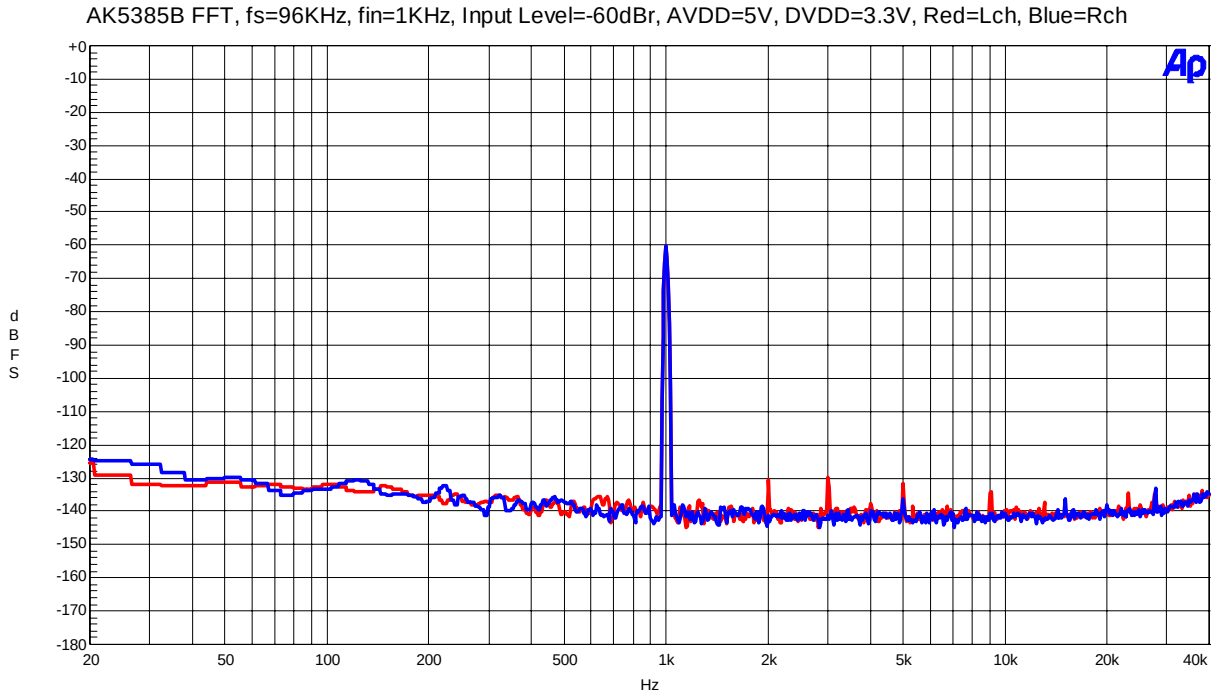


Figure 15. FFT Plot (Input=-60dBr)

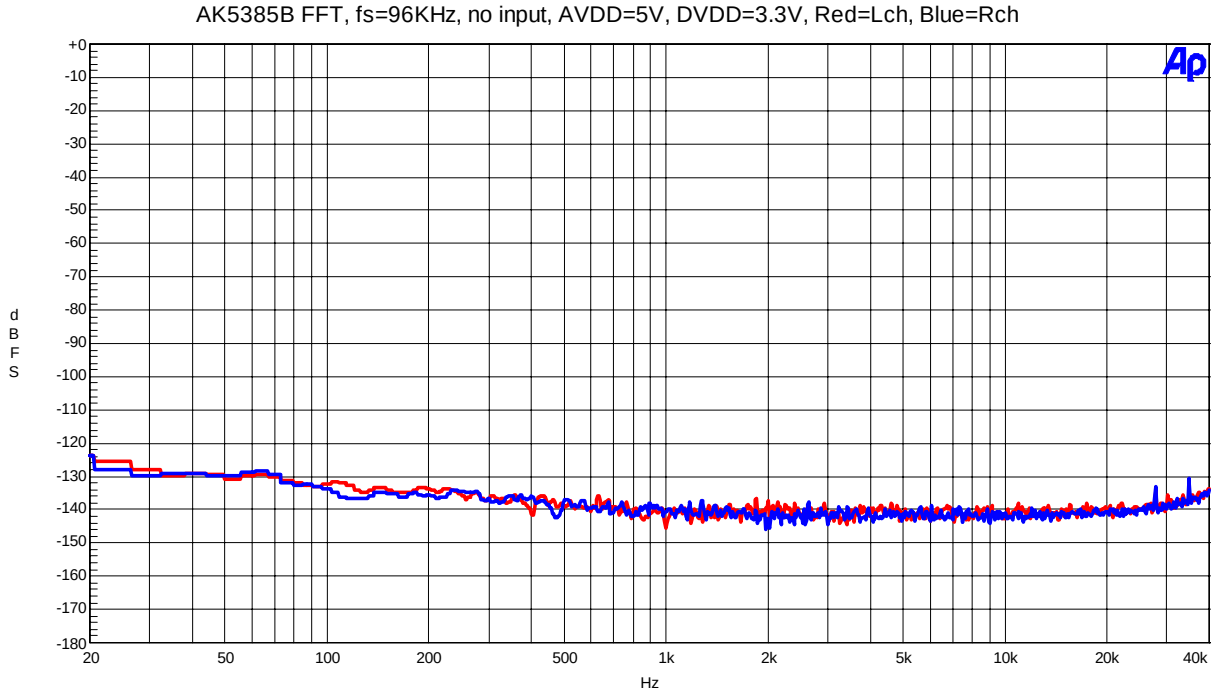


Figure 16. FFT Plot (no input)

[ADC Plot : fs=192kHz]

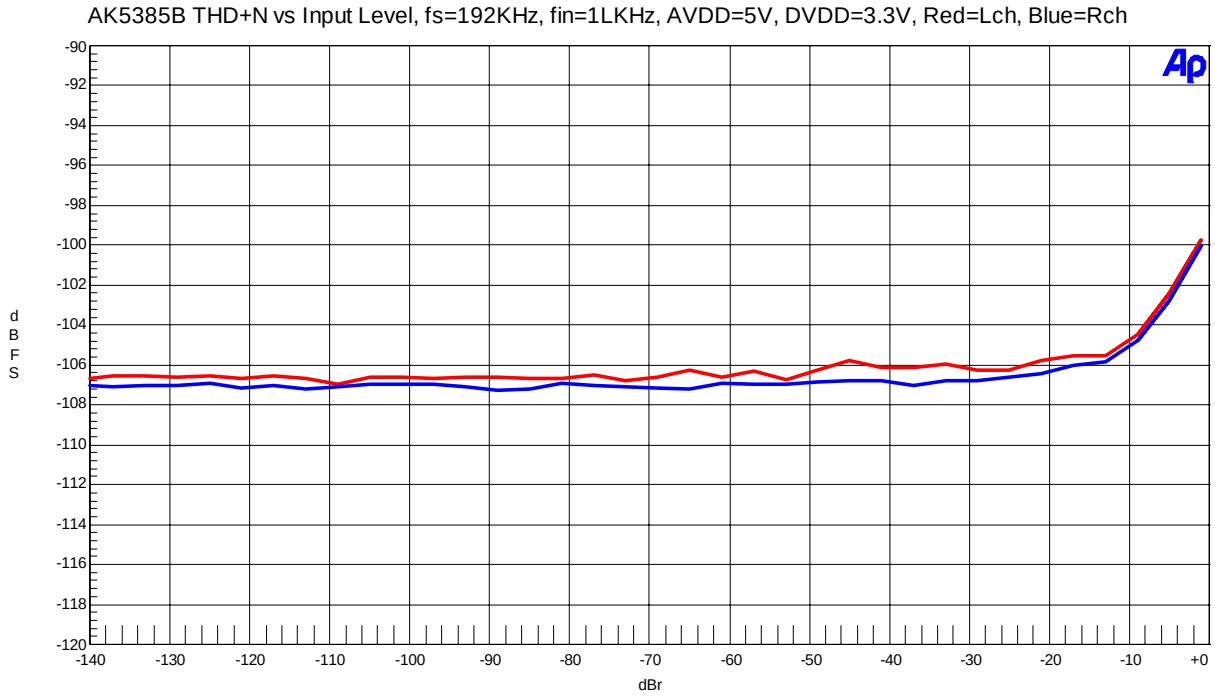


Figure 17. THD+N vs. Input Level

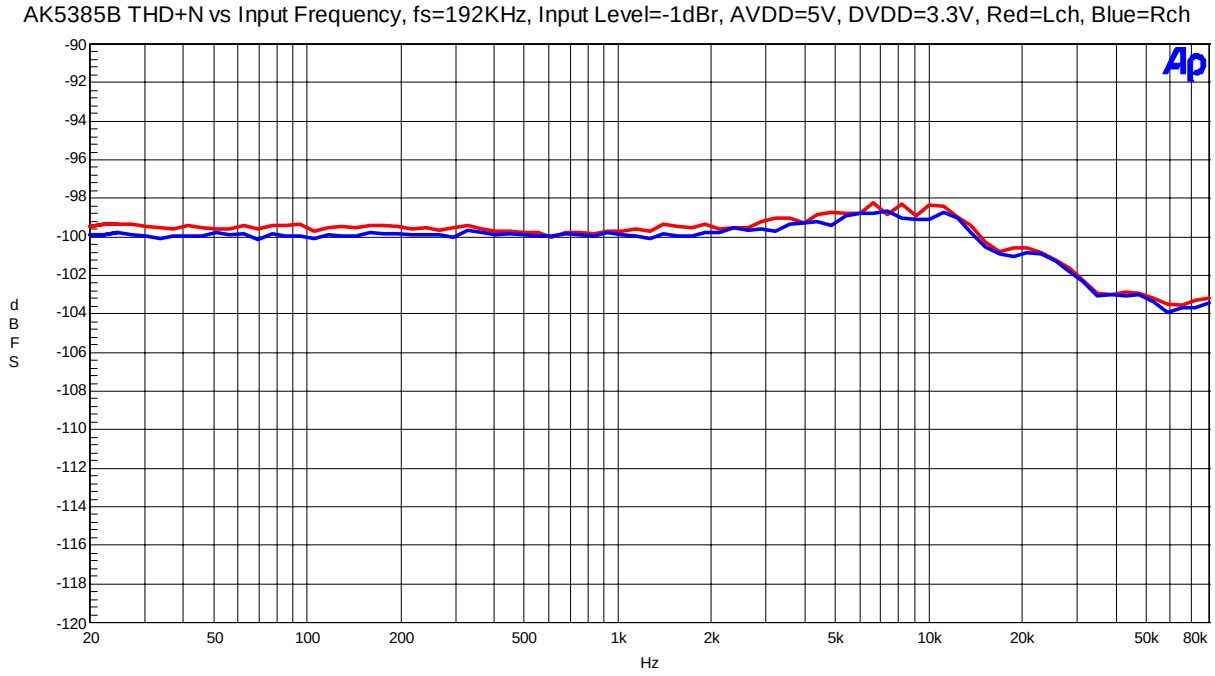


Figure 18. THD+N vs. Input Frequency (BW=40kHz)

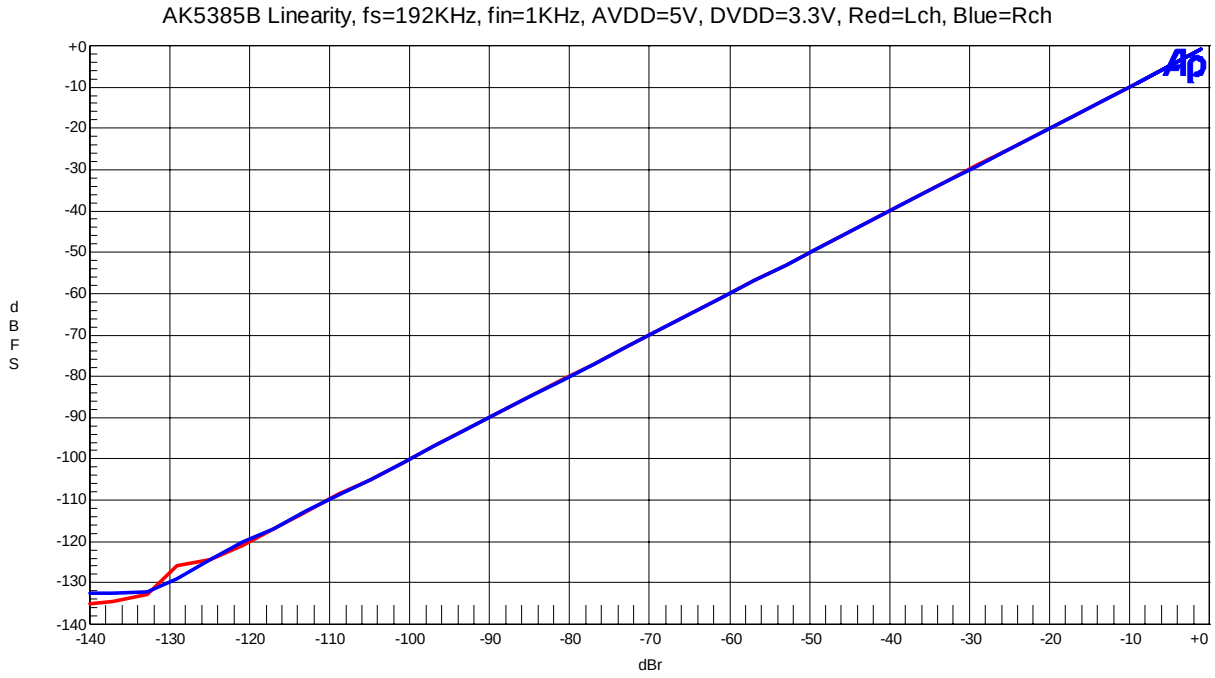


Figure 19. Linearity

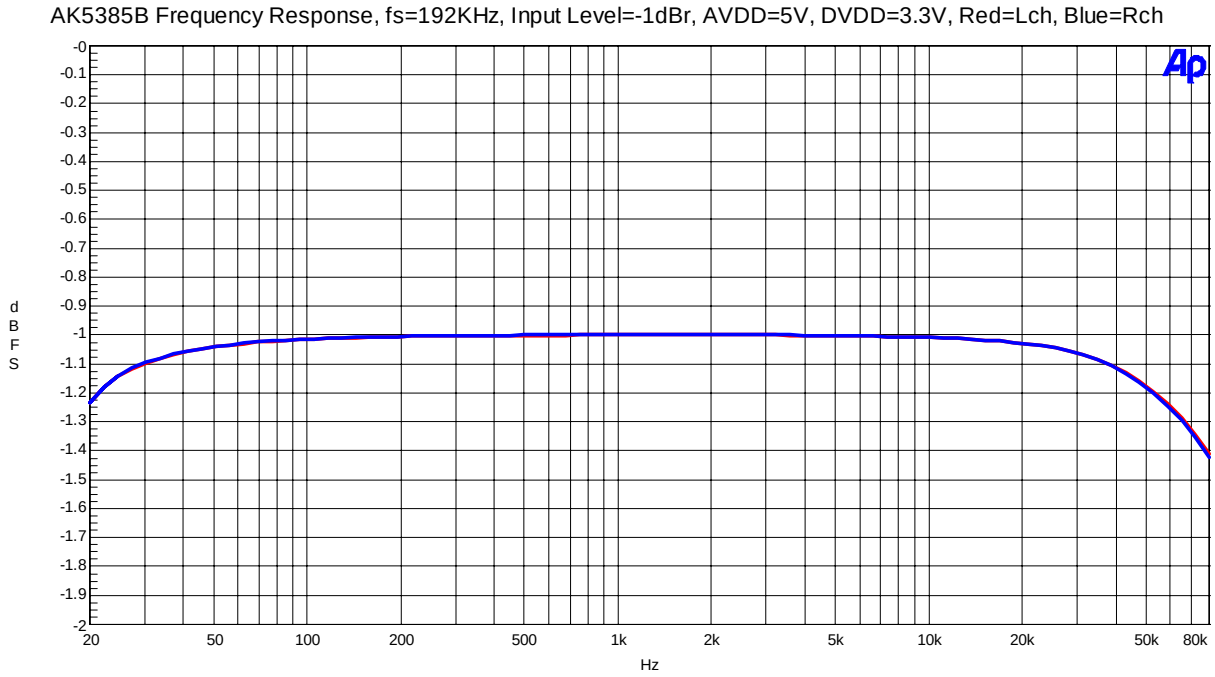


Figure 20. Frequency Response

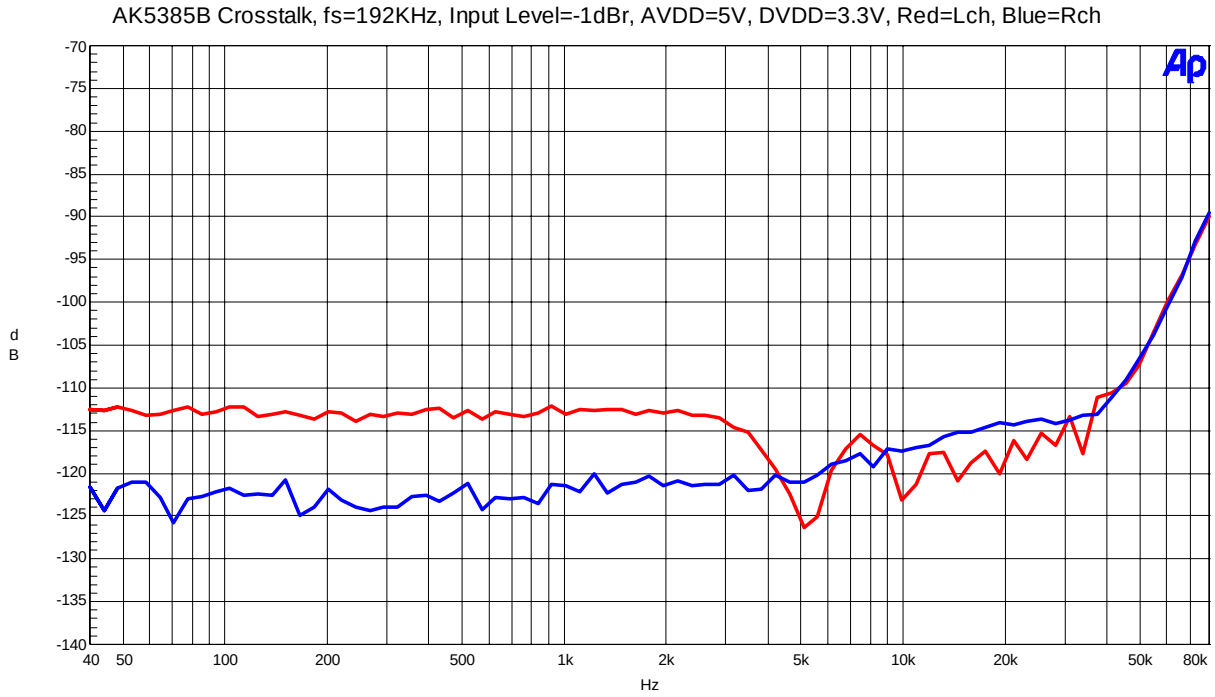


Figure 21. Crosstalk

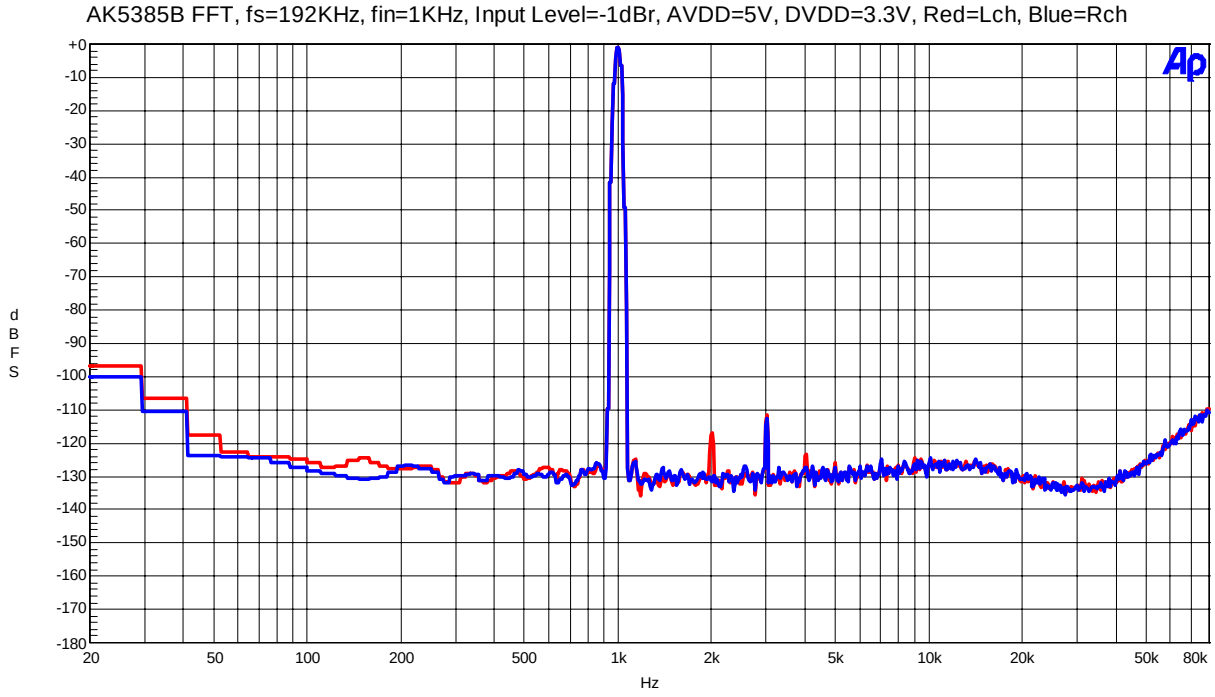


Figure 22. FFT Plot (Input=-1dBr)

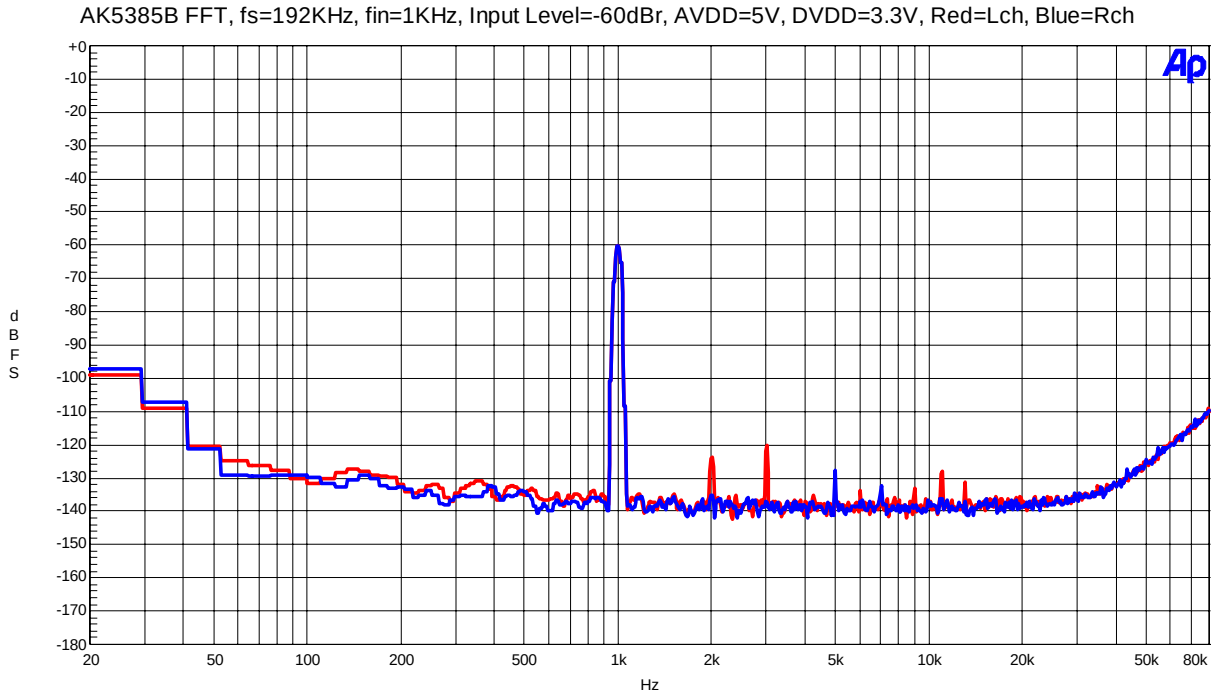


Figure 23. FFT Plot (Input=-60dBr)

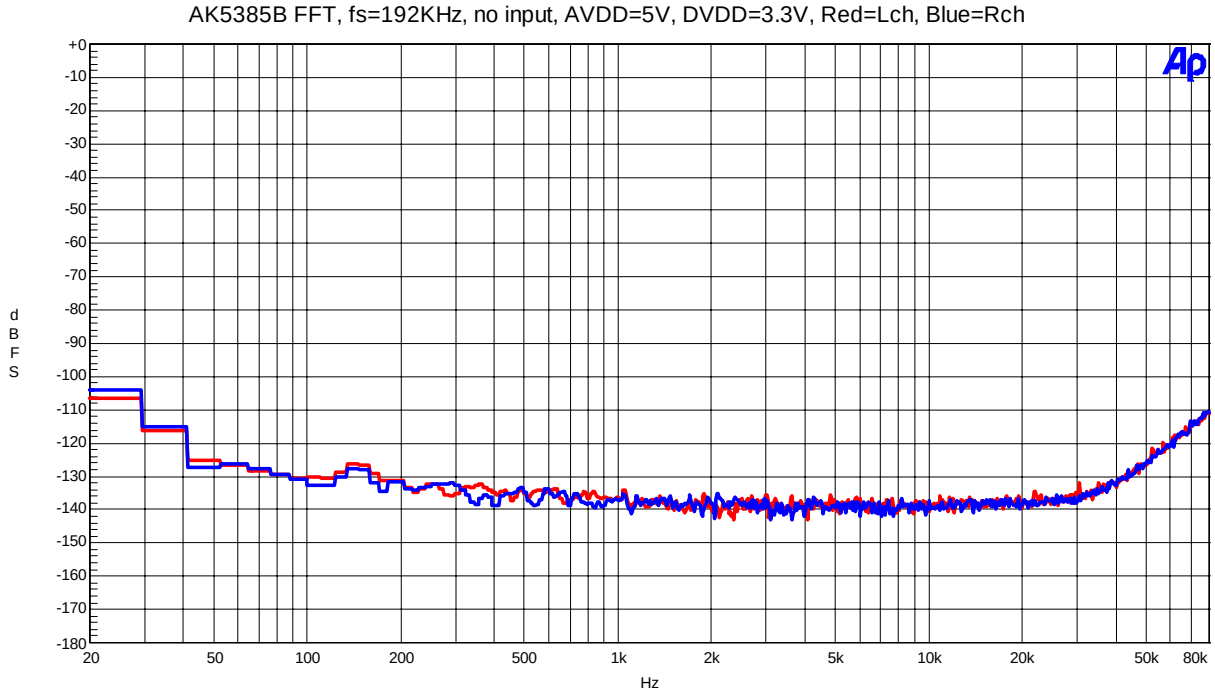
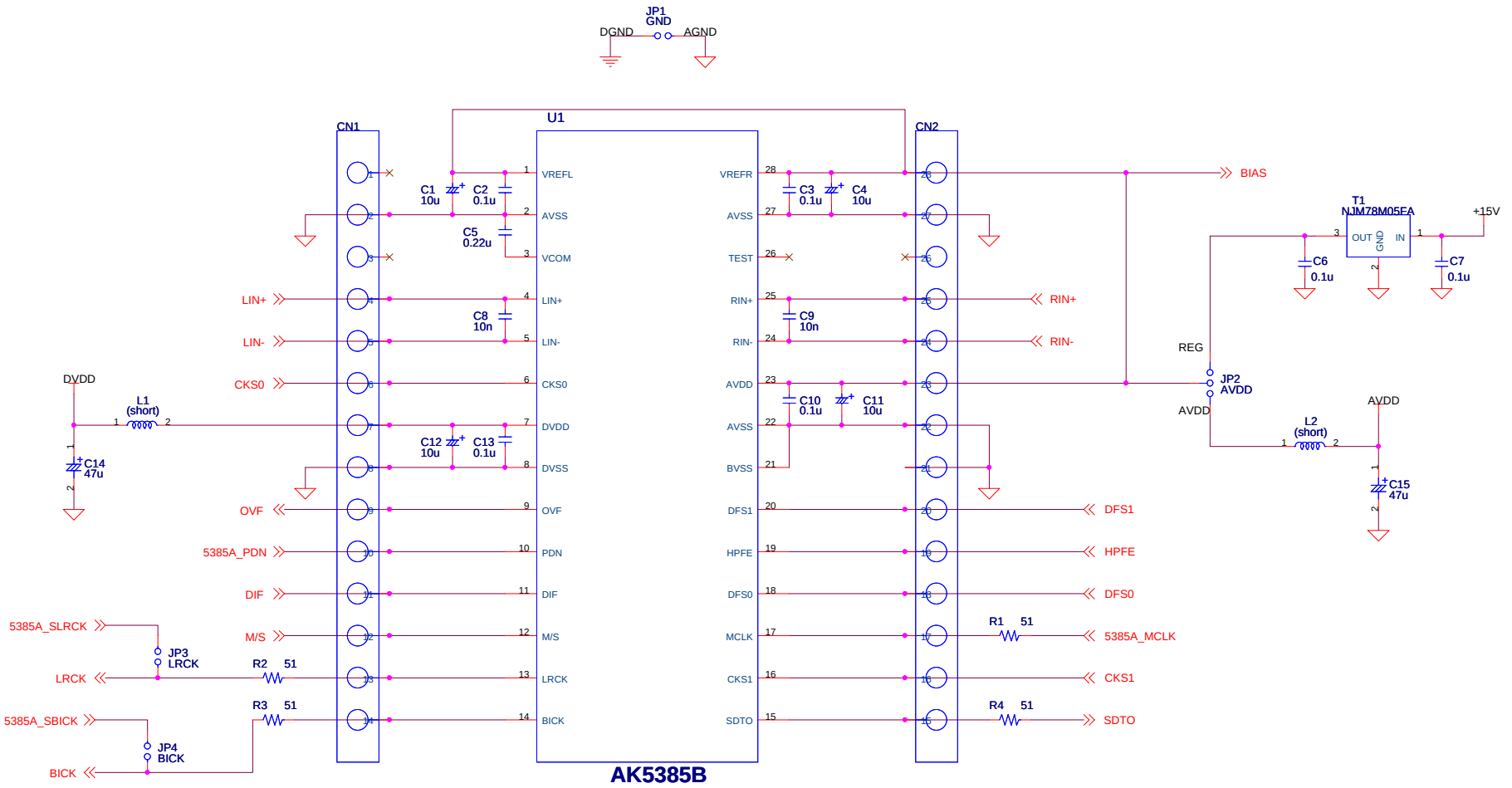


Figure 24. FFT Plot (no input)

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
05/09/02	KM080500	0	First Edition	



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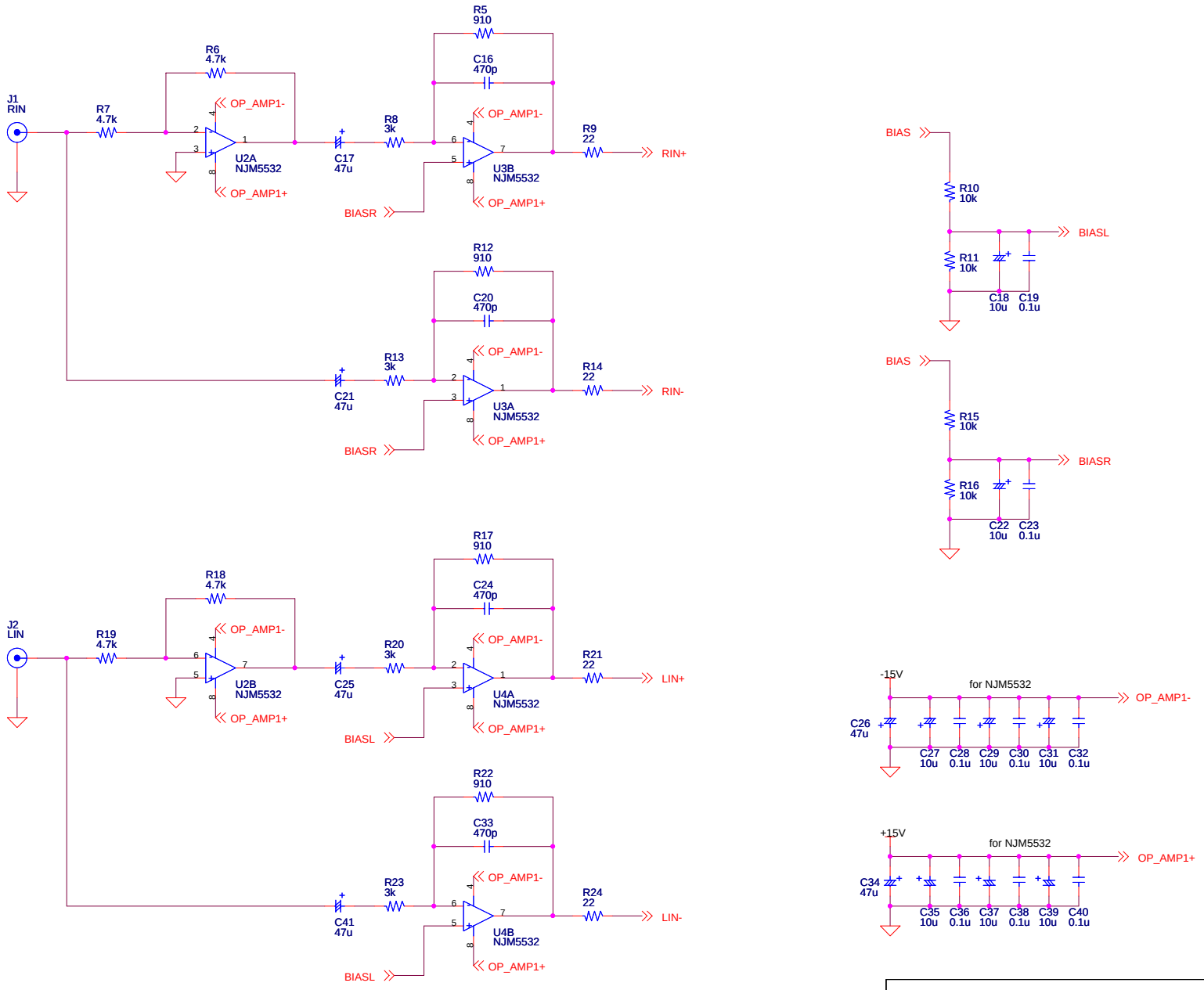
Date: Monday, September 12, 2005	Sheet 1 of 4	



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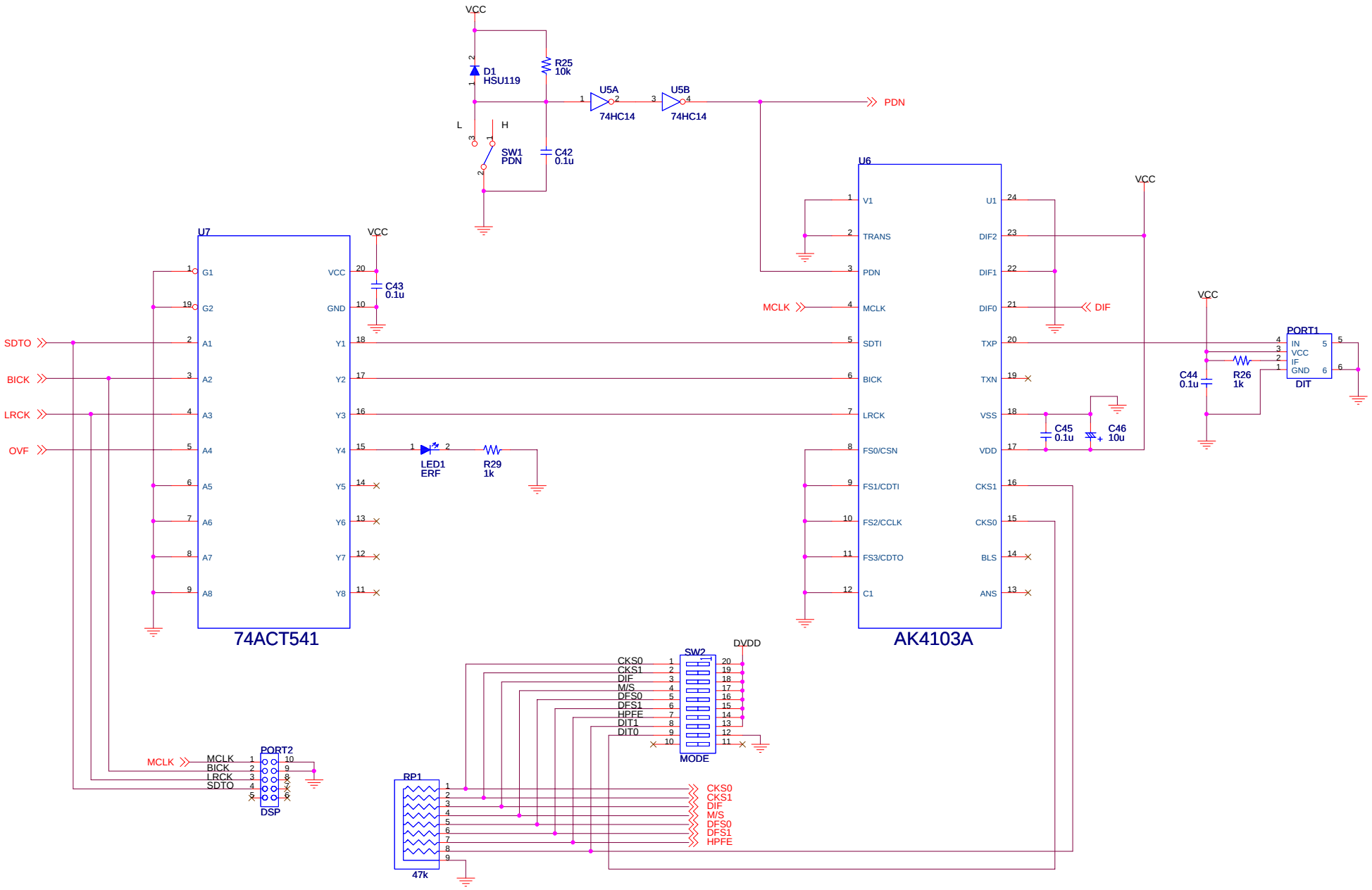

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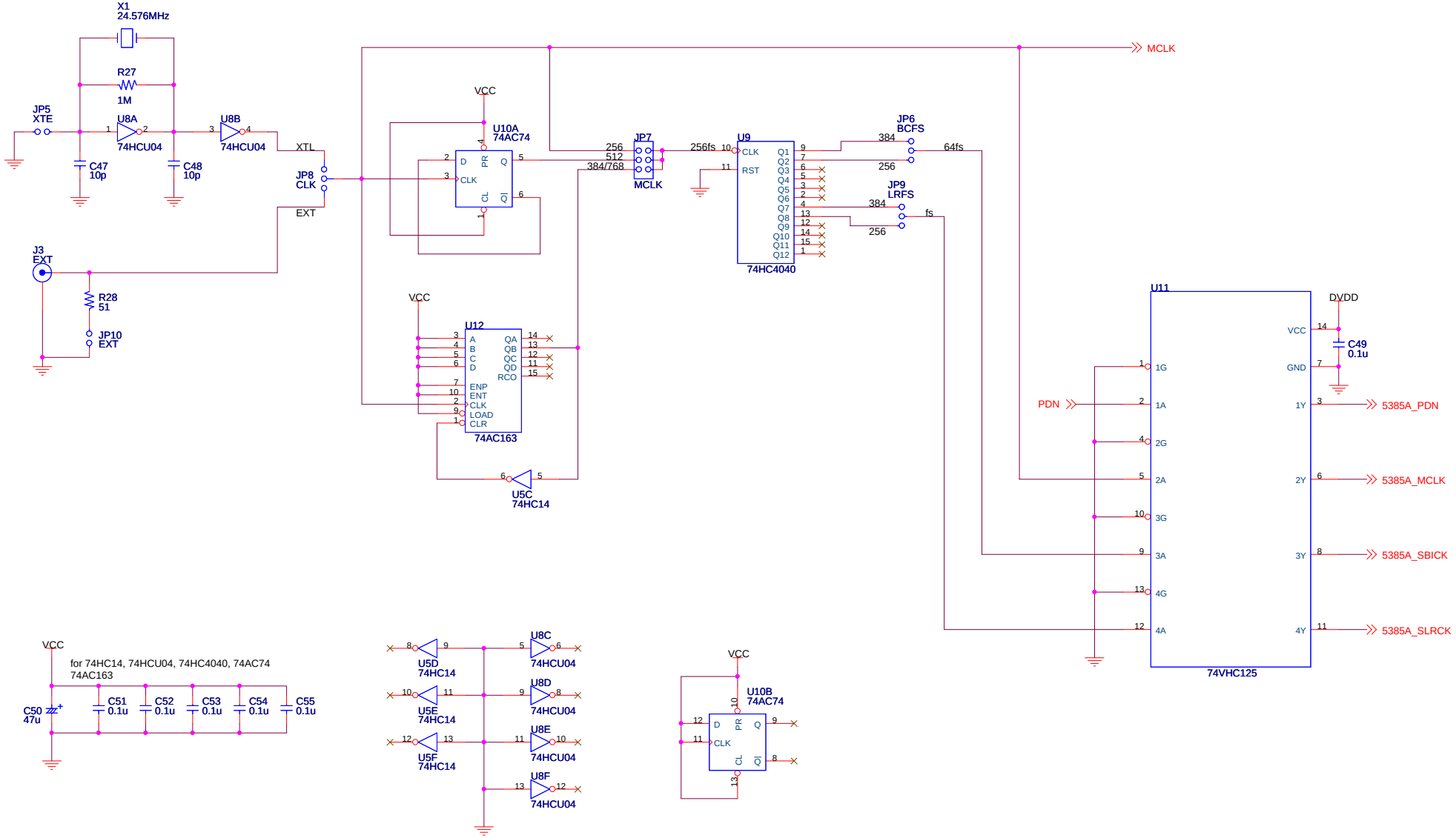
Size A3	Document Number DIT		Rev 0
Date: Monday, September 12, 2005	Sheet 3 of 4		



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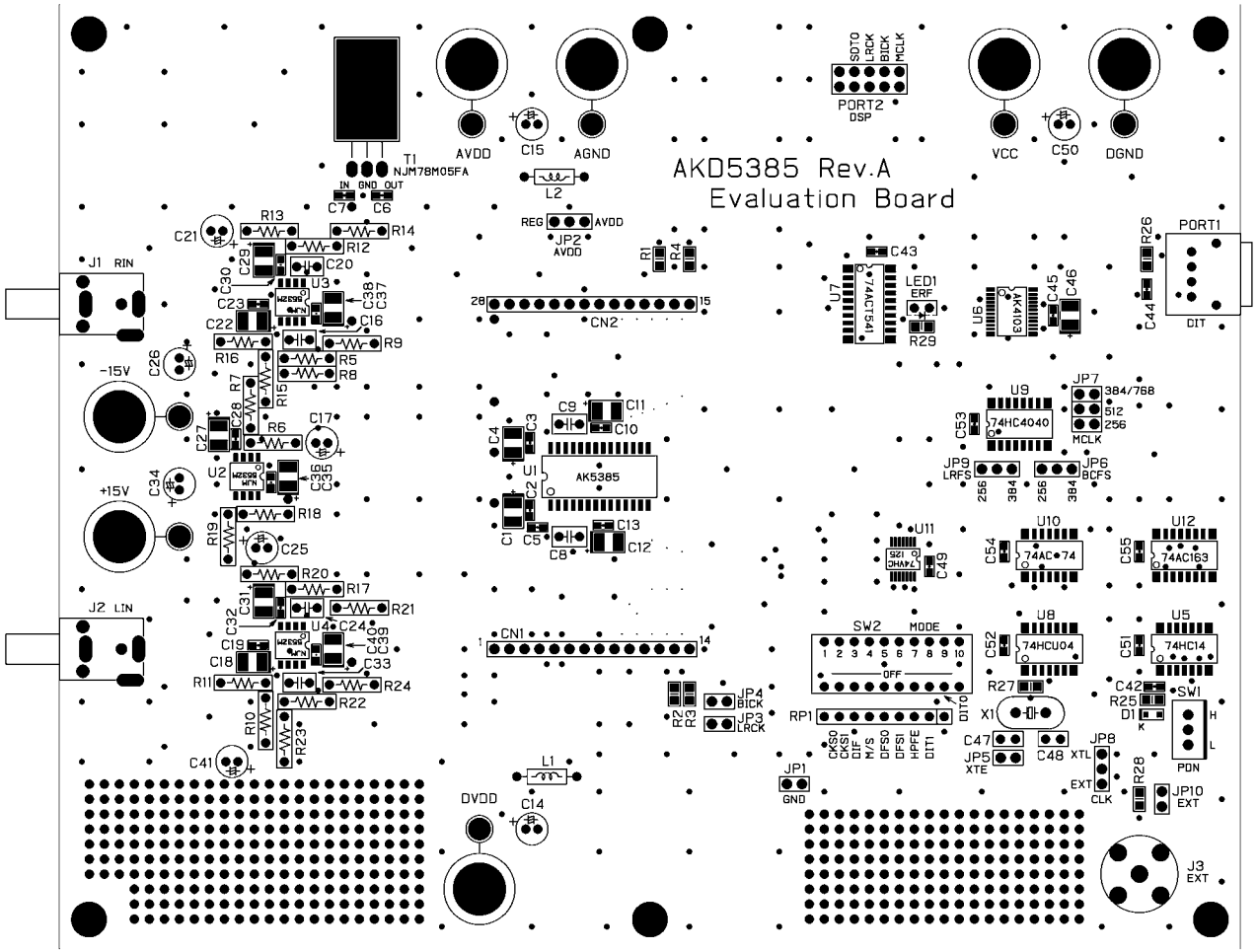
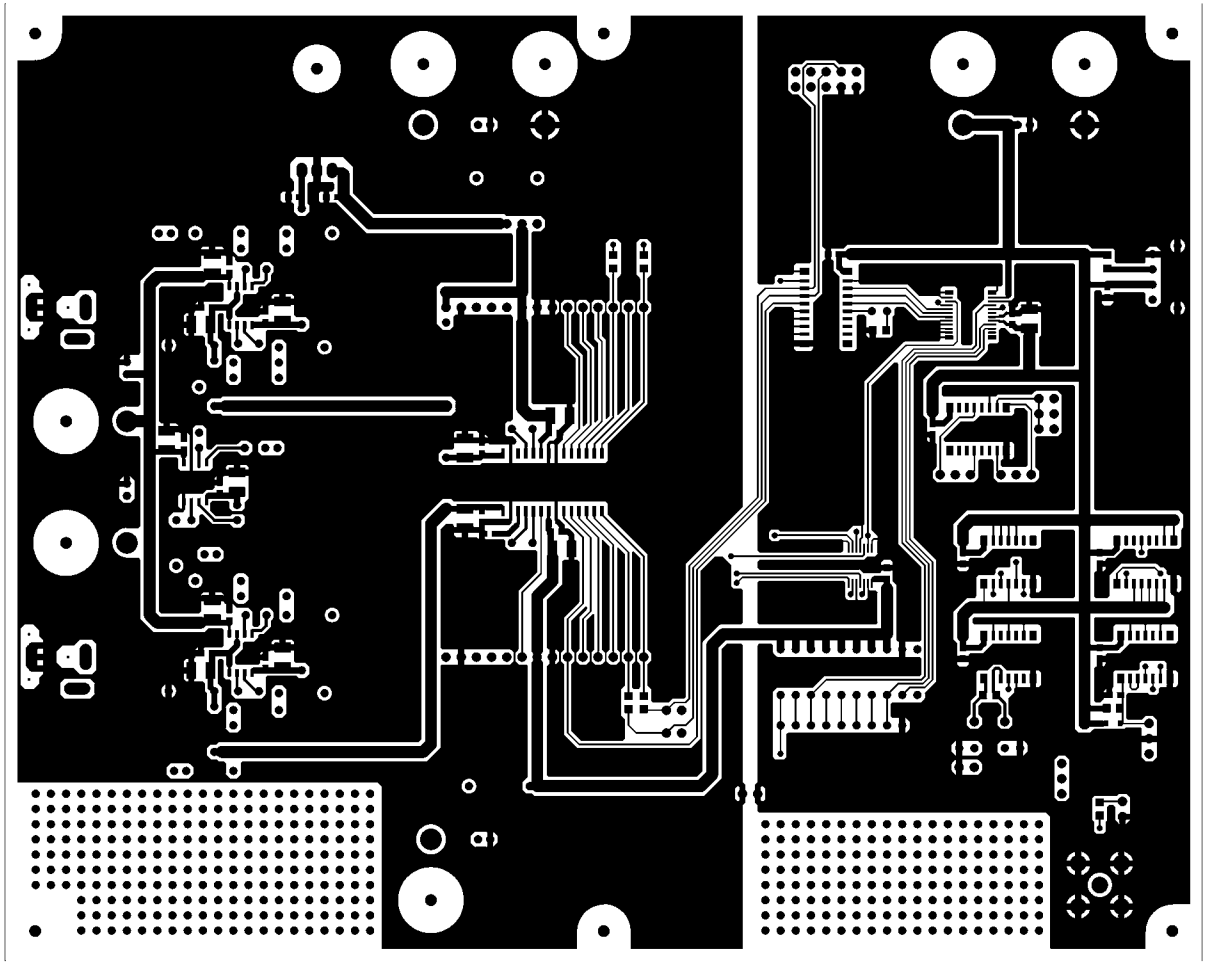


AKD5385 Rev.A L1 SR SILK



AKD5385 Rev.A L1

AKD5385 Rev.A L2