AUDIO CODEC WITH HEADPHONE DRIVER AND PROGRAMMABLE SAMPLE RATES

FEATURES

- Complete DAC and ADC Audio CODEC with headphone driver.
- Up to 96kHz input sampling frequencies for ADC/DAC
- Selectable DAC De-emphasis Filter.
- Selectable ADC High Pass Filter
- Programmable Audio Data Interface
  - I^2S, Normal, Left justified or DSP data for ADC/DAC
  - 16,18, 20 and 24-bit input data resolution
- System clock: 64fs, 96fs,128fs, 192fs, 256fs or 384fs
- 250fs and 272fs system clock for USB application
- Master or Slave Clocking mode
- Regular audio or USB mode audio
- 2 or 3-wire software control interface selectable by external pin.
- 2 channel microphone or line inputs
- Programmable power down features to conserve power

GENERAL

- 2.7-volt to 3.6-volt Power Supply range (TBD)
- 28-pin SSOP package

APPLICATIONS

- Low cost, CD-quality consumer audio equipment
- Portable MP3 Players and Recorders

ADVANCE PRODUCT INFORMATION.
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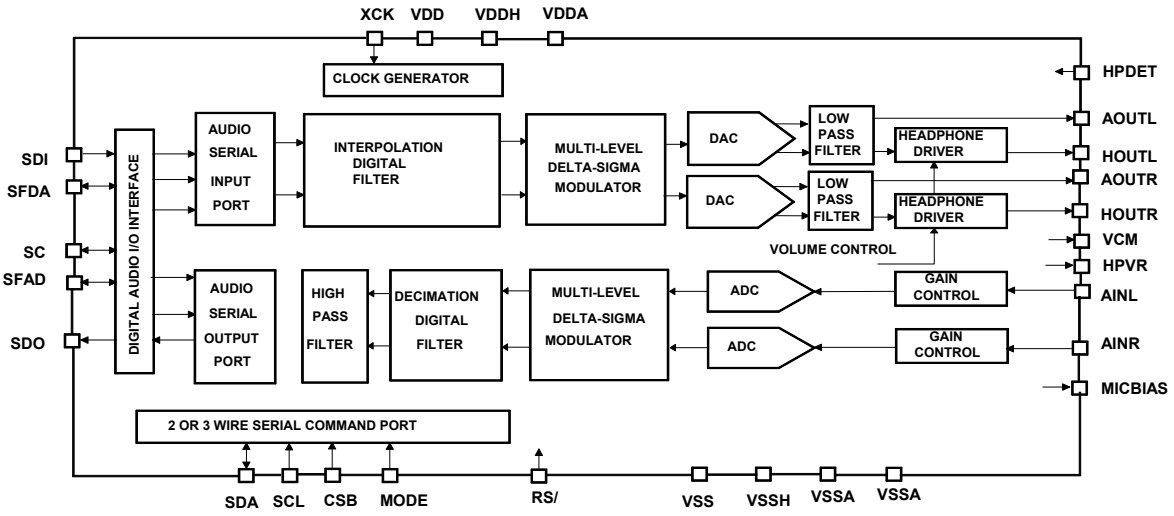
DESCRIPTION

The AV2722 is a mixed signal CMOS monolithic device which is a low cost audio CODEC designed with a built-in headphone driver. It supports regular audio or USB mode audio and is therefore ideal for portable MP3 audio and speech players and recorders. It can also be used for mini-disk, CD-RW machines.

Stereo line audio inputs with programmable gain are provided A microphone bias voltage output is also provided which makes the AV2722 ideal for an electret type microphone.

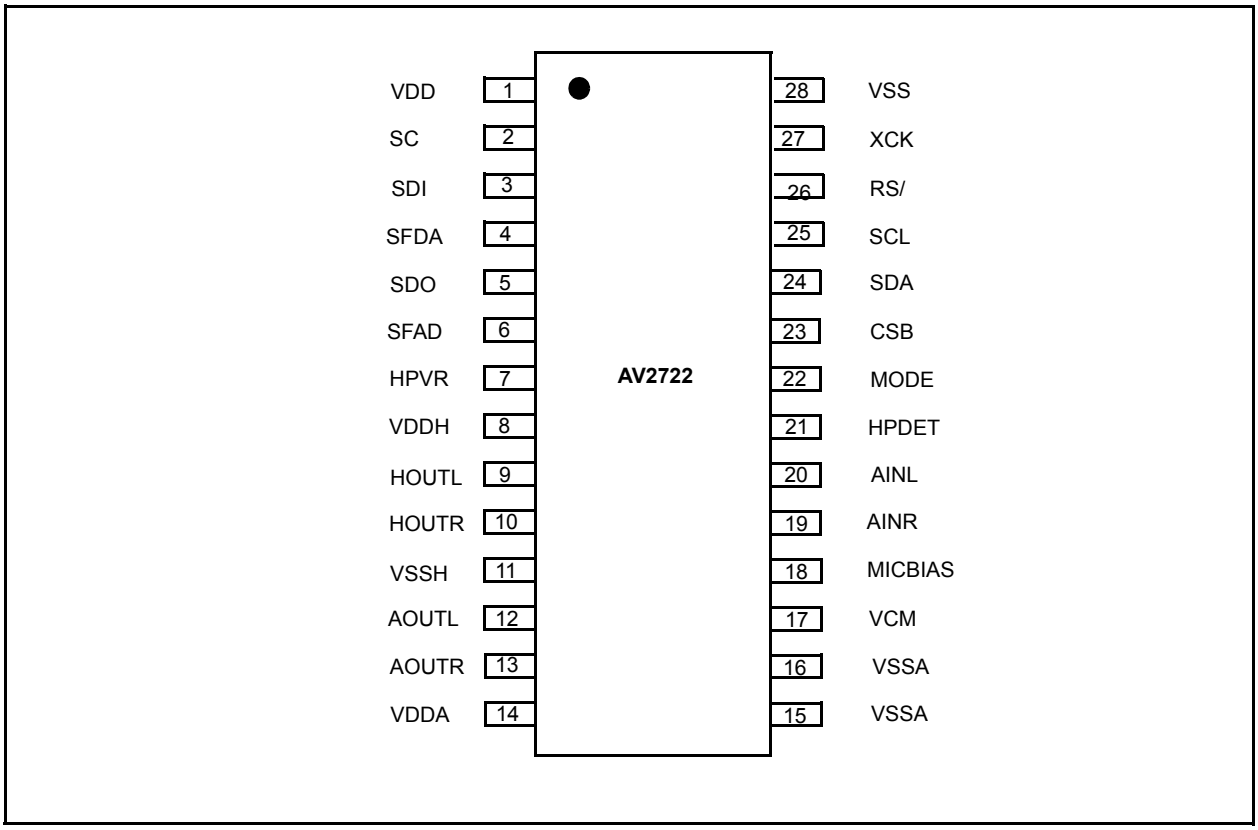
For the multi-bit signal delta DAC, 64X oversampling digital interpolation filter is used with programmable de-emphasis, volume control, and sampling rate selection features. The DAC supports I2S, Normal, Left justified or DSP data with 16, 18, 20 and 24-bit resolution. Sampling rates from 8KHz to 192 KHz are supported. At the DAC output, stereo headphone drivers are built in for driving headphones.

For the multi-bit delta-sigma ADC, programmable gain are provided at the input. State of the art decimation filter is used to down-sample the received signal and finally a selectable high pass filter is used to reduce un-wanted low frequency noise. The digital audio serial output can be programmed at various formats similar to the DAC input.



AV2722 BLOCK DIAGRAM

PIN CONFIGURATION



ORDERING INFORMATION

PRODUCT	PACKAGE	TEMPERATURE RANGE
AV2722	28-pin SSOP	-25 TO +85^{o}C

PIN ASSIGNMENTS

Pin No.	Pin Name	Type	Description
1	VDD	Supply	Power supply for digital circuits
2	SC	Digital Input/Output	DAC serial input data bit clock. It is input for slave mode and output for master mode.
3	SDI	Digital Input	DAC serial input data. It can be in normal, left justified, i2s, or DSP type
4	SFDA	Digital Input/Output	DAC sample rate clock. It is input for slave mode and output for master mode. For normal or left-justified type SDI data input, a high in SFDA indicates left channel data, a low in SFDA indicates right channel data. For I2S type, a low in SFDA indicates left channel data, a high in SFDA indicates right channel data.For DSP mode, a”sync” pulse in SFDA is followed by two data words, left channel data is followed by right channel data.
5	SDO	Digital Output	ADC serial output data. It can be in normal, left justified, i2s, or DSP type.
6	SFAD	Digital Input/Output	ADC sample rate clock. It is input for slave mode and output for master mode. For normal or left-justified type SDO data output, a high in SFAD indicates left channel data, a low in SFAD indicates right channel data. For I2S type, a low in SFAD indicates left channel data, a high in SFAD indicates right channel data. For DSP mode, a”sync” pulse in SFAD is followed by two data words, left channel data is followed by right channel data.
7	HPVR	Analog Output	Voltage reference for CAPLESS headphone connection..
8	VDDH	Supply	Power supply for headphone circuits.
9	HOUTL	Analog Output	Left channel headphone output.
10	HOUTR	Analog Output	Right channel headphone output.
11	VSSH	Ground	Ground for headphone circuits.
12	AOUTL	Analog Output	Left channel audio line output.
13	AOUTR	Analog Output	Right channel audio line output.
14	VDDA	Supply	Power supply for analog circuits.
15	VSSA	Ground	Ground for analog circuits.
16	VSSA	Ground	Ground for analog circuits
17	VCM	Analog output	Analog circuits common mode reference.
18	MICBIAS	Analog Output	Microphone bias.
19	AINR	Analog Input	Right channel line/microphone input.

Pin No.	Pin Name	Type	Description
20	AINL	Analog Input	Left channel line/microphone input
21	HPDET	Digital Input	Headphone is plugged in or not plugged in indicator. The polarity of this signal can be inverted or not inverted, which is controlled by programming bit HPDETMODE (creg4[2], address 04 hex), a logic “low” inverts the polarity of HPDET into the chip.
22	MODE	Digital Input	I2C or MPU control interface selection. If MODE is logic “high”, the chip is using MPU for chip programming. If MODE is logic “low”, the chip is using I2C for chip programming. MODE can be no-connect for MPU control due to the internal “pullup” resistor.
23	CSB	Digital Input	3-wire MPU chip select, active low.
24	SDA	Digital Input/Output	3-wire MPU data input /output or 2-wire I2C data input/output
25	SCL	Digital Input	3-wire MPU clock input /2-wire I2C clock input
26	RS/	Digital Input	Active low chip reset
27	XCK	Digital Input	Chip clock input. The clock rate of XCK depends on the audio sampling rate, regular audio or USB audio.
28	VSS	Ground	Ground for digital circuits

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuits is manufactured on a CMOS process. It can be damaged by ESD. AVS recommends that all integrated circuits be handled with appropriate ESD precautions. Improper handling and installation procedures can cause damage to the device.

XCK SYSTEN CLOCK REQUIREMENT

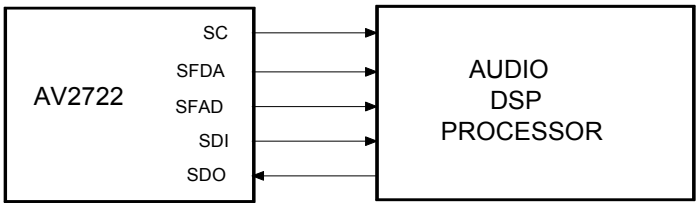
The system clock (XCK at pin 27) for the AV2722 supports audio sampling rates from 64fs to 384fs for regular type audio, where fs is the audio sampling frequency (SFDA /SFAD), typically 8KHz, 44.1KHz, 48KHz, 96KHz, or 192KHz. For USB type audio, SFDA /SFAD is either 250fs or 272fs. XCK is used to operate the digital interpolation filter and the delta-sigma modulator. By using the two-wire (I2S) or 3-wire (MPU type) serial command port, user can program the chip to accept different clock frequency under different sampling rate.

Sampling Rate		XCK Clock Frequency (MHz) For Regular Mode					
ADC	DAC	64fs	96fs	128fs	192fs	256fs	384fs
48KHz	48KHz	N/A	N/A	N/A	N/A	12.288	18.432
48KHz	8KHz	N/A	N/A	N/A	N/A	12.288	18.432
8KHz	48KHz	N/A	N/A	N/A	N/A	12.288	18.432
8KHz	8KHz	N/A	N/A	N/A	N/A	12.288	18.432
44.1KHz	44.1KHz	N/A	N/A	N/A	N/A	11.289	16.934
44.1KHz	8KHz	N/A	N/A	N/A	N/A	11.289	16.934
8KHz	44.1KHz	N/A	N/A	N/A	N/A	11.289	16.934
8KHz	8KHz	N/A	N/A	N/A	N/A	11.289	16.934
88.2KHz	88.2Khz	N/A	N/A	11.289	16.934	N/A	N/A
96KHz	96KHz	N/A	N/A	12.288	18.432	N/A	N/A
OFF	192KHz	12.288	18.432	24.576	36.864	49.152	73.728

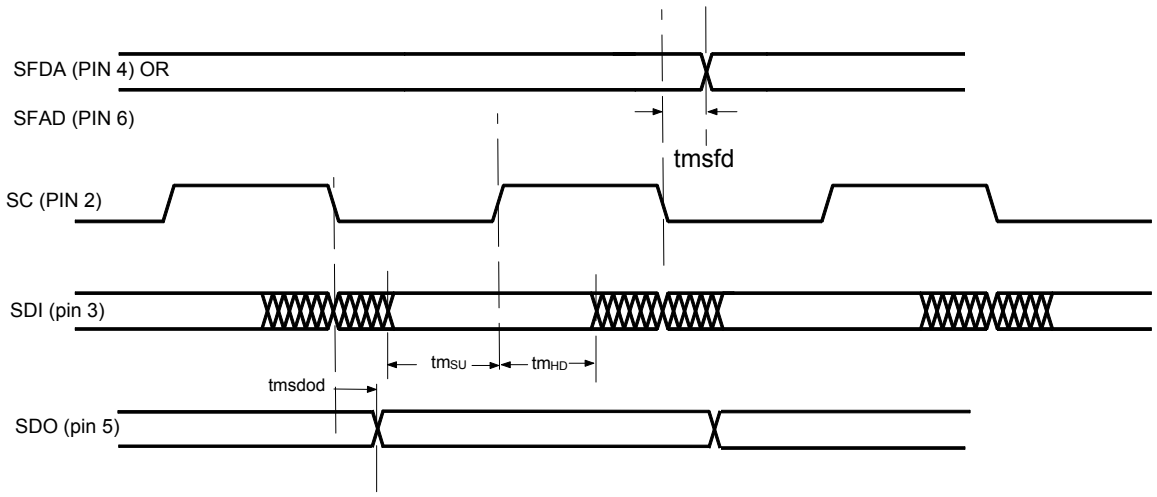
Sampling Rate		XCK Clock Frequency (MHz) For USB Mode	
ADC	DAC	250fs	272fs
48KHz	48KHz	12	N/A
48KHz	8KHz	12	N/A
8KHz	48KHz	12	N/A
8KHz	8KHz	12	N/A
96KHz	96KHz	12	N/A
44.1KHz	44.1KHz	N/A	12
44.1KHz	8KHz	N/A	12
44.1KHz	8KHz	N/A	12
8KHz	44.1KHz	N/A	12
8KHz	8KHz	N/A	12
88.2KHz	88.2KHz	N/A	12

MASTER AND SLAVE MODE OPERATION - DIGITAL AUDIO INTERFACE

The AV2722 can be operated in either master or slave mode. By default, the chip is set to operate in “Slave” mode. To configure the chip for “Master” mode operation, the programming bit MASTER (CREG6[7]) must be programmed to “1”. In master mode operation, AV2722 acts as a master which generates SC, SFAD, and SFDA. In slave mode operation, AV2722 receives these signals from an audio DSP encoder/decoder source.

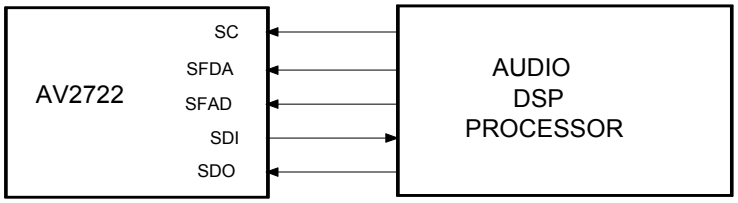


AV2722 in Master Mode

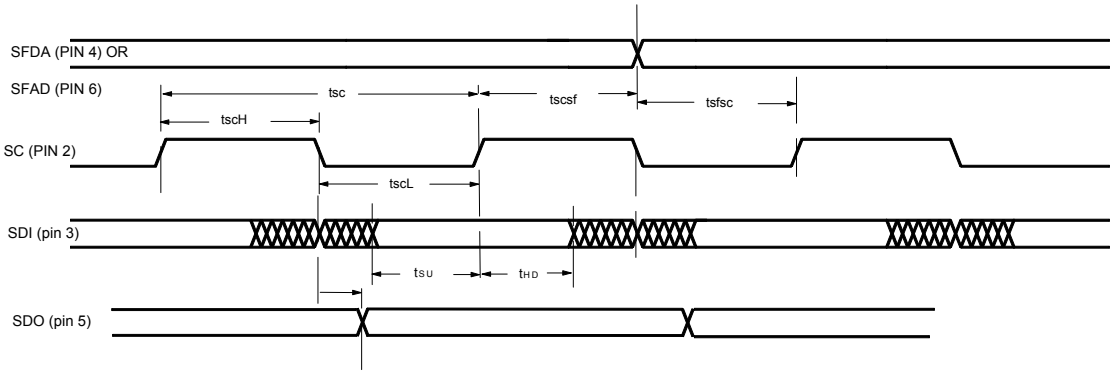


SDI audio data setup time	tm_{SU}	10 ns (min)
SDI audio data hold time	tm_{HD}	10 ns (min)
SFDA/SFAD propagation delay from SC ↓	tmsfd	10 ns (max)
SDO propagation delay from SC ↓	tmsdod	10 ns (max)

Audio Data Input Timing - MASTER MODE



AV2722 in Slave Mode

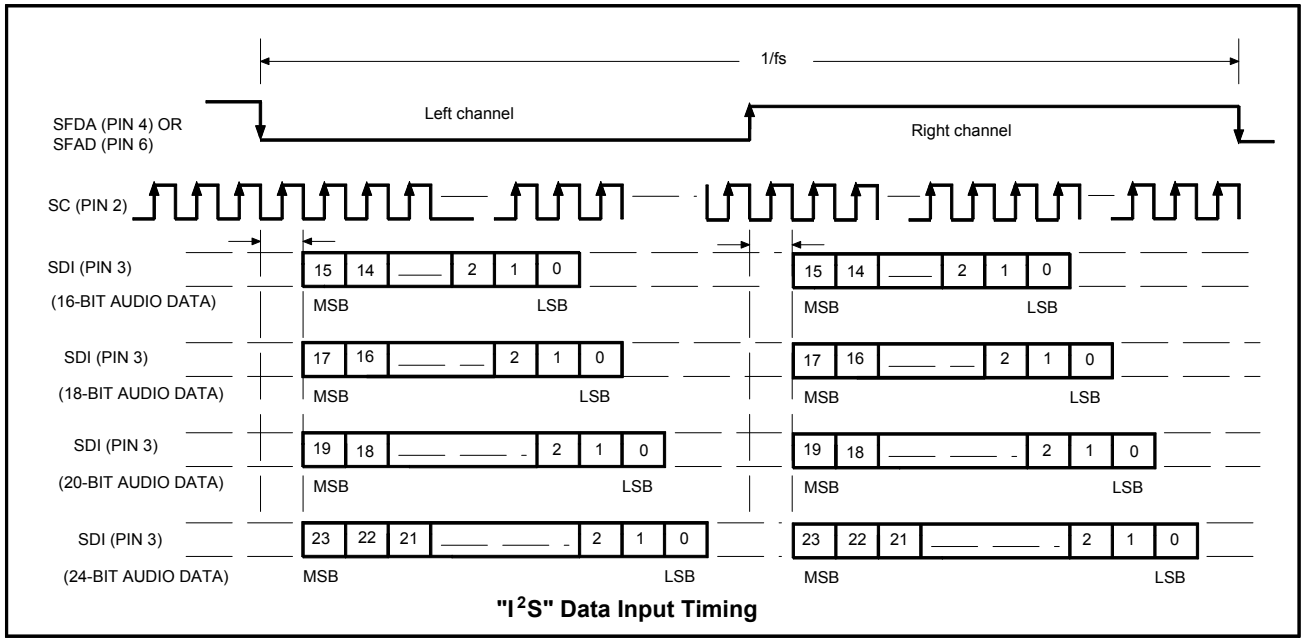


SC pulse cycle time	tsc	50 ns (min)
SC pulse width, High	tscH	20 ns (min)
SC pulse width, Low	tscL	20 ns (min)
SDI audio data setup time	t_{SU}	10 ns (min)
SDI audio data hold time	t_{HD}	10 ns (min)
SC ↓ to SFDA / SFAD edge	tscsf	10 ns (min)
SFDA / SFAD edge to SC ↓	tsfsc	10 ns (min)
SDO propagation delay from SC ↓	tsdod	10 ns (max)

Audio Data Input Timing - SLAVE MODE

I2S MODE

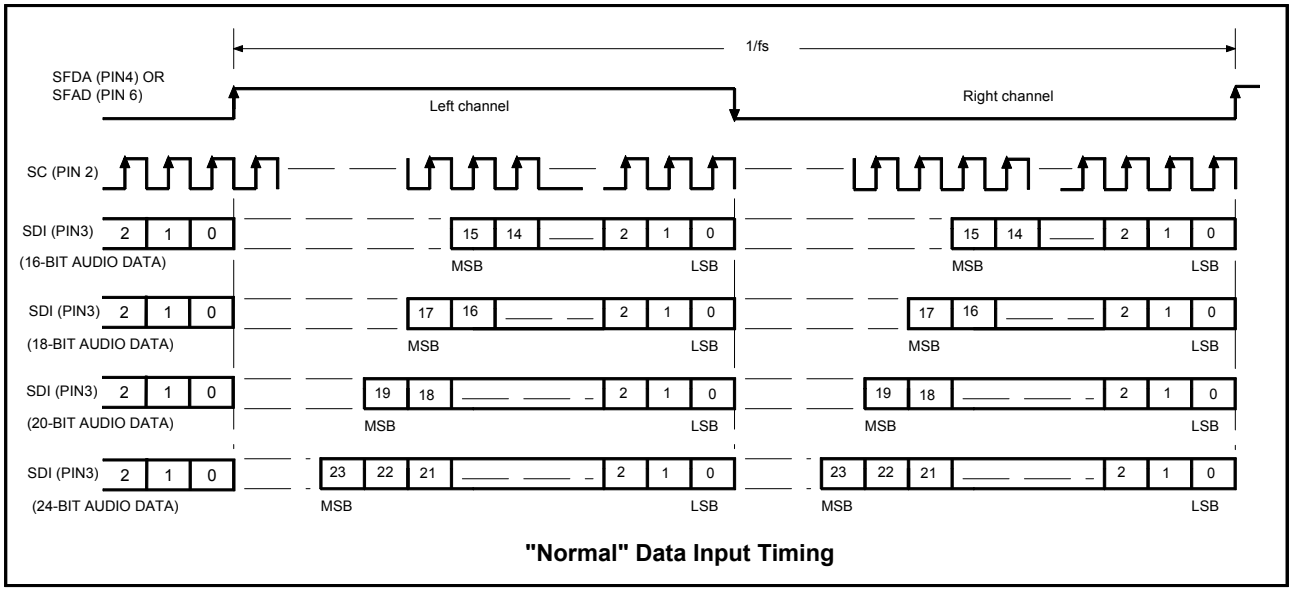
In I2S Mode, the MSB of the audio data SDI is sampled on the second rising edge of SC following SFDA/SFAD transition. SFDA/SFAD are low during the left channel samples and high during the right channel samples.



"I²S" Data Input Timing

Normal Mode

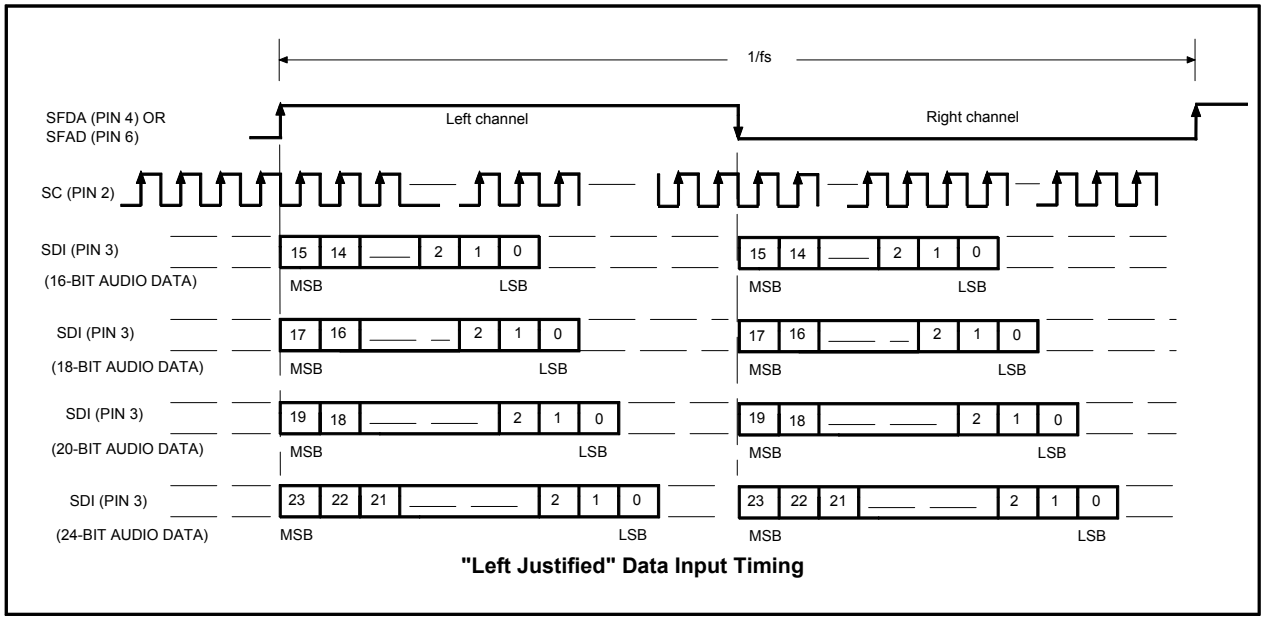
In Normal Mode, the audio data, SDI, is right-justified. The LSB are aligned with the rising/falling edge of SFDA/ SFAD. Data is latched into the chip on the rising edge of SC. SFDA/SFAD are high during the left channel samples and low during the right channel samples.



"Normal" Data Input Timing

LEFT JUSTIFIED MODE

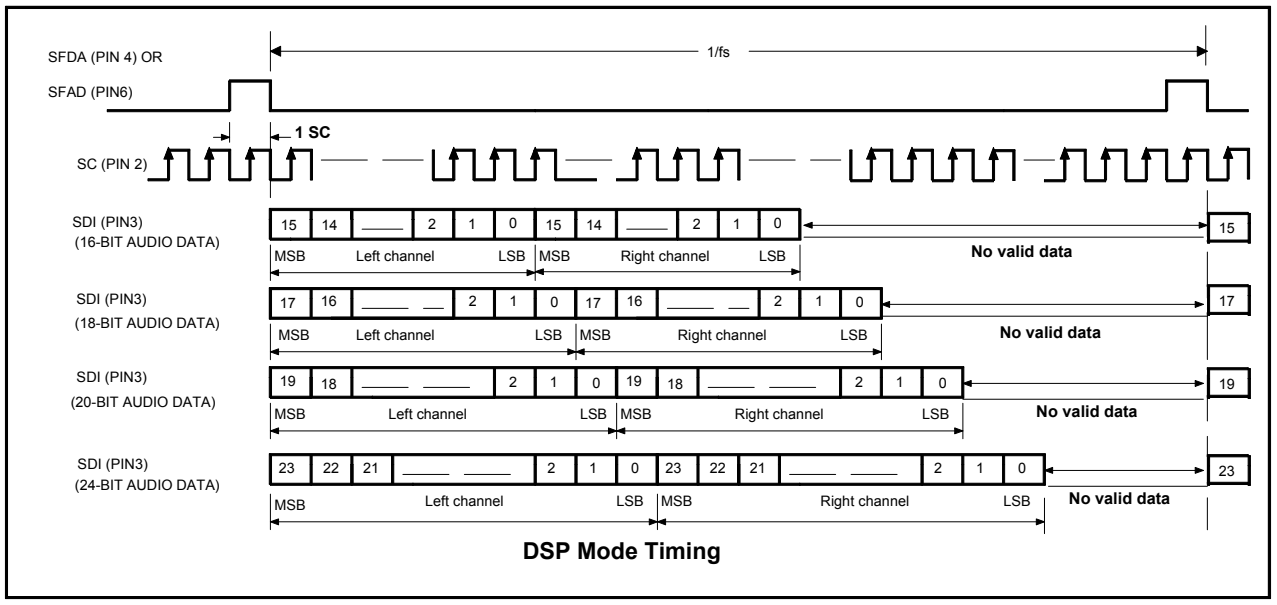
In Left Justified mode, the MSB of the audio data SDI is sampled on the first rising edge of SC following SFDA/ SFAD transition. SFDA/SFAD are high during the left channel samples and low during the right channel samples.



"Left Justified" Data Input Timing

DSP Mode

In DSP Mode, the audio data SD is in time division multiplexed format. The left and right channel data are shifted into the chip in sequence with the left channel data first followed by the right channel data. SFDA/SFAD is a “sync” pulse which appears every 1/fs time. The minimum SFDA/SFAD sync-pulse is one SC cycle.



DSP Mode Timing

SOFTWARE CONTROL INTERFACE

The AV2722 programmable registers can be programmed via the software control interface. Either 3-wire (MPU type) or 2-wire (I2S) interface are supported. The MODE pin sets the selection of the software control interface.

MODE (PIN No. 22)	SOFTWARE CONTROL INTERFACE
0	2-wire I2S
1	3-wire MPU type

3-WIRE SERIAL COMMAND PORT

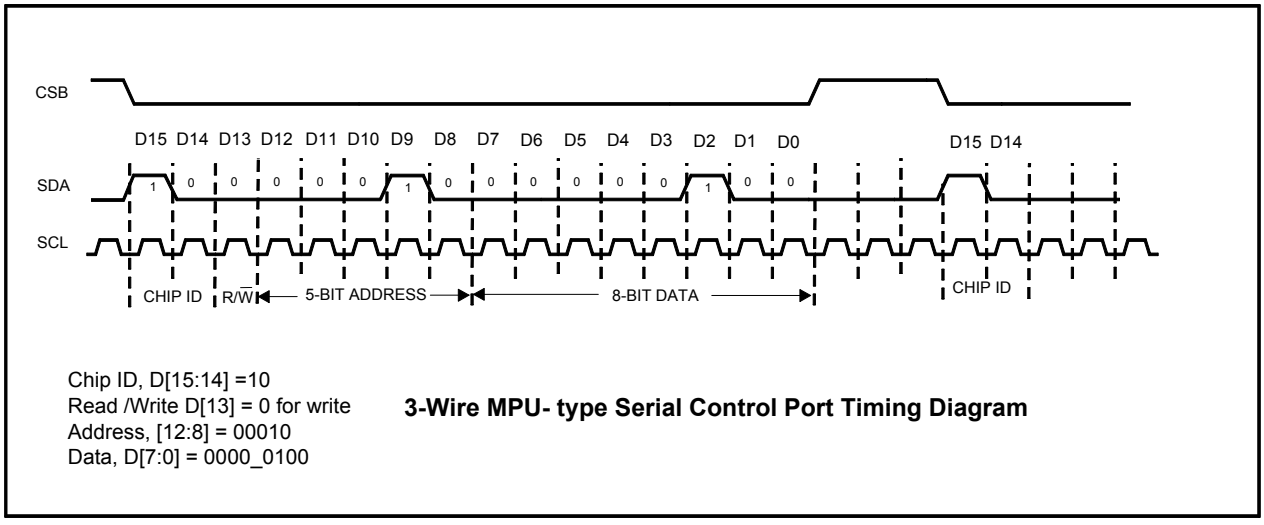
By default, the AV2722 is set to use the 3-wire, microprocessor-type interface (MPU). Because MODE pin is internally pulled up to default the chip in MPU programming mode. Therefore, the MODE pin can be “no-connect” if MPU interface is used. The 3-wire serial command port receives serial input data (SDA), serial input clock (SCL) and active low chip select (CSB). The serial data is clocked in by the rising edge of the serial input clock if CSB is low. The 16 bit serial input data contains 8 address control bits followed by 8 data bits.

The address control bits are:

D[15:14] - chip ID. (For the AV2722, chip ID is binary “10”)
D[13] - read/write control bit. (For the AV2722, D[13]=1 for read and 0 for write)
D[12:8] - 5-bit programmable register address.

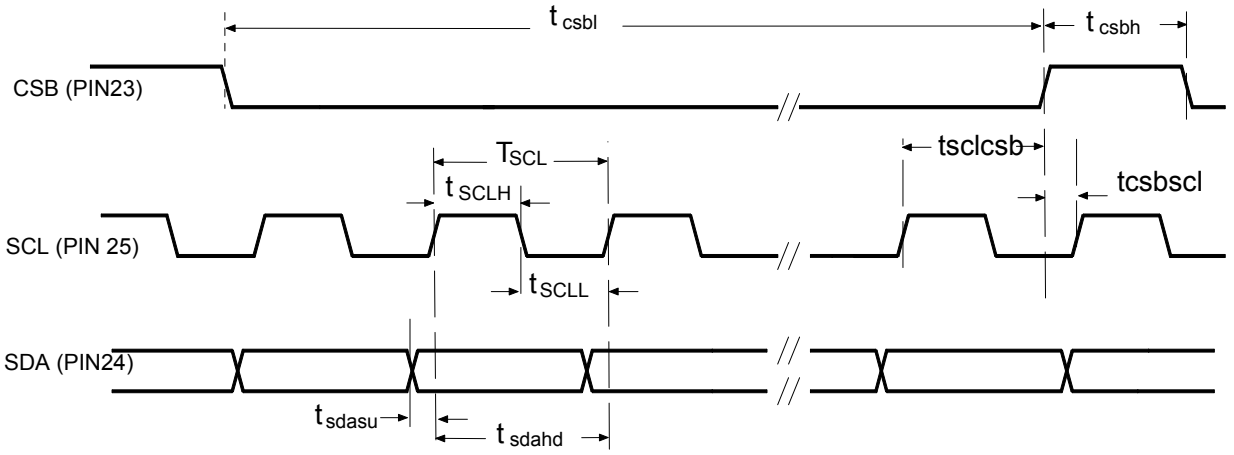
The data bits are:D[7:0] - 8 bit data.

An example is given to write into address ‘00010’ with data ‘0000_0100’.



Chip ID, D[15:14] =10
Read /Write D[13] = 0 for write
Address, [12:8] = 00010
Data, D[7:0] = 0000_0100

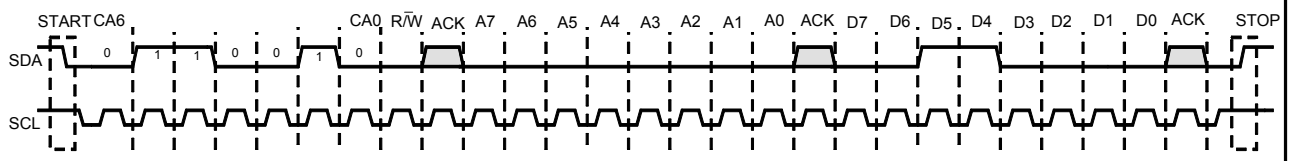
3-Wire MPU- type Serial Control Port Timing Diagram



3-Wire MPU-type Serial Control Port Timing Requirement

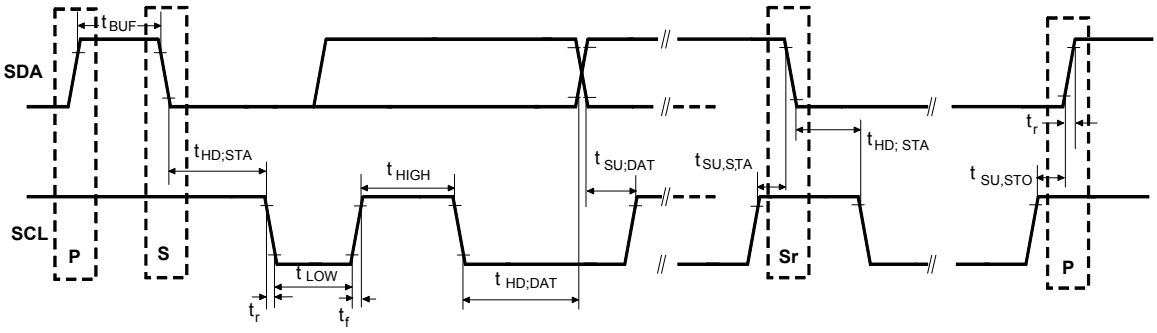
2-WIRE (I2C) SERIAL COMMAND PORT

The AV2722 also provides a 2-wire I2C Serial Command Port for chip programming. User can use this port to program the internal control registers. The Chip Address for the AV2722 is a 7-bit hexadecimal number “32hex”. The protocol for write operation consists of sending 3 bytes of data to the AV2722 at the SDA pin. Following each byte is the acknowledge generated by the AV2722. The first byte is the 7-bit Chip Address followed by the read/ write bit (read is logic “high” and write is logic “low”) The second byte is the AV2722 control register address. The third byte is the control register data. An example which illustrates “write” timing of register address 00H and data 30H is given below.



Chip Address: CA[6:0]=011_0010
Register Address: A[7:0]= 00H
Data: d[7:0] = 30H

I2S - Serial Command Port Timing Diagram



I2S - Serial Command Port Timing Requirement

To use the 2-wire I2C serial command port, the MODE pin must be connected to ground through a pulldown resistor.

Upon power up, all programming registers are set to default values. By default, or without using I2C or MPU-type port, the AV2722 is set ready to run 256fs clock frequency with 44.1K or 48K sampling rate, and to accept 24-bit, left justitied data, with de-emphasis filtering turns off.

REGULAR OR USB AUDIO DATA

The AV2722 can be operated in regular (non-USB) or USB (Universal Serial Bus) modes. The usage of regular or USB applications are programmed via the 3-wire or 2-wire serial command port. The selection of sampling rates for regular or USB modes are controlled by CREG3[7:0]. Please refer to the section “Programmable Control Register Assignment” below.

In regular audio application, the user selects an appropriate XCK clock which is generated by an off chip oscillator.The user then program the chip for desired ADC, DAC sampling frequencies. By default, the chip is set to operated at 48KHz sampling rate, 256fs for both the ADC and DAC, with XCK running at 12.288 MHz. The AV2722 supports sampling rates from 8KHz to 96 KHz for both ADC and DAC. For 192 KHz sampling rate, only the DAC path is operational. The ADC path is “turned off”.

In USB system, the common USB clock frequency is 12 MHz. To use the AV2722 for USB application, XCK should be running at 12 MHz.

PROGRAMMABLE CONTROL REGISTER ASSIGNMENT

The are 13 Programmable Registers in the AV2722. The function and address assignment of these registers are described in the following table. All these programmable registers can be read back via the Serial Command Port.

Address (7-bit hex)	Register	Default Value (hex)	Register Function
0	VOLREG[7:0]	7F	Volume value for both left and right channel
1	CREG1[7:0]	00	De-emphasis control
2	CREG2[7:0]	00	DAC path serial input port control
3	CREG3[7:0]	00	DAC, ADC sampling frequency selection control
4	CREG4[7:0]	00	DAC and miscellaneous power down control
5	CREG5[7:0]	40	DAC headphone control
6	CREG6[7:0]	00	ADC path serial output port control
7	CREG7[7:0]	03	ADC high-pass filter control
8	CREG8[7:0]	12	ADC path left channel gain and mute control
9	CREG9[7:0]	12	ADC path right channel gain and mute control
A	CREG10[7:0]	06	ADC power down control
B	CREG11[7:0]	00	ADC path left and right microphone gain control
C	CREG12[7:0]	00	Chip software reset

ADDRESS 00, VOLUME REGISTER (CREG0[7:0])

A[7:0]	CREG0[7:0]							
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Hex 00	VOLUME[7:0]							
Default Value	0	1	1	1	1	1	1	1

VOLUME[7:0]: control the volume of the left and right DAC channels concurrently. Default value is 8'h7F.

ADDRESS 01, DE-EMPHASIS CONTROL REGISTER (CREG1[7:0])

A[7:0]	CREG1[7:0]							
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Hex 01	Reserved							DEEMP
Default Value	0	0	0	0	0	0	0	0

DEEMP:De-emphasis Control
0: by-pass the de-emphasis filter in the DAC path (default).
1: enable the de-emphasis filter in the DAC path.

ADDRESS 02, DAC PATH SERIAL INPUT PORT CONTROL REGISTER (CREG2[7:0])

A[7:0]	CREG2[7:0]							
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Hex 02	bpf48	dahrsc	dasfdly	dainvsc	damode[1:0]		daformat[1:0]	
Default Value	0	0	0	0	0	0	0	0

BPF48: Bit per SFDA/SFAD frame control
0: bit per frame is 64 bit, i.e. 32-bit for the left channel and 32-bit for the right channel for the SD input and SDO output.
1:bit per frame is 48 bit, i.e. 24-bit for the left channel and 24-bit for the right channel for the SD input and SDO output.

DAHRSC: DACs use higher rate SC
0: DAC path uses whatever SC is provided, either master or slave mode (default).
1: DAC path uses higher rate SC. When the ADC path is at higher sampling than the DAC path, program this bit to "1" allows SD input to come in at the higher SC rate.

DASFDLY: Delay SFDA by 1 SC in the DAC path.
0: do not delay the SFDA by 1 SC cycle (default).
1: delay the SFDA by 1 SC cycle.

DAINVSC: Invert the SC bit clock.
0: do not invert the SC bit clock (default).
1: invert the SC bit clock.

DAMODE[1:0]: These two bits define the DAC path serial data input mode.
- 00: left justified mode (default).
- 01: I2S mode.
- 10: normal mode
- 11: DSP mode

DAFORMAT[1:0]: These two bits define the audio serial input data bit length.
- 00: 24 bits (default).
- 01: 20-bits.
- 10: 18 bits.
- 11: 16 bits.

ADDRESS 03, DAC, ADC SAMPLING FREQUENCY SELECTION CONTROL REGISTER (CREG3[7:0])

A[7:0]	CREG3[7:0]							
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Hex 03	Reserved		freqcon[5:0]					
Default Value	0	0	0	0	0	0	0	0

The freqcon[5:0] are used to set up the device to work under different XCK clock rate and various sampling rate combinations. The following table defines programming values under different XCK and sampling rate conditions.There are 26 various cases for regular (non-USB) mode and 10 various cases for USB mode.

Regular (non-USB) Mode Frequency Control Register Settings

SAMPLING RATE		XCK FREQUENCY	SFDA SFAD	FREQUENCY CONTROL REGISTER PROGRAMMING VALUES						
ADC	DAC			FREQCON[5:0]						
KHz	KHz	MHz	NO. OF XCK	No.	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
48	48	12.288	256	0	0	0	0	0	0	0
48	48	18.432	384	1	0	0	0	0	0	1
48	8	12.288	256	2	0	0	0	0	1	0
48	8	18.432	384	3	0	0	0	0	1	1
8	48	12.288	256	4	0	0	0	1	0	0
8	48	18.432	384	5	0	0	0	1	0	1
8	8	12.288	256	6	0	0	0	1	1	0
8	8	18.432	384	7	0	0	0	1	1	1
44.1	44.1	11.289	256	8	0	0	1	0	0	0
44.1	44.1	16.934	384	9	0	0	1	0	0	1
44.1	8	11.289	256	10	0	0	1	0	1	0
44.1	8	16.934	384	11	0	0	1	0	1	1
8	44.1	11.289	256	12	0	0	1	1	0	0
8	44.1	16.934	384	13	0	0	1	1	0	1
8	8	11.289	256	14	0	0	1	1	1	0
8	8	16.934	384	15	0	0	1	1	1	1
88.2	88.2	11.289	128	16	0	1	0	0	0	0
88.2	88.2	16.934	192	17	0	1	0	0	0	1
96	96	12.288	128	18	0	1	0	0	1	0
96	96	18.432	192	19	0	1	0	0	1	1
OFF	192	12.288	64	20	0	1	0	1	0	0
OFF	192	18.432	96	21	0	1	0	1	0	1
OFF	192	24.576	128	22	0	1	0	1	1	0
OFF	192	36.864	192	23	0	1	0	1	1	1
OFF	192	49.152	256	24	0	1	1	0	0	0
OFF	192	73.728	384	25	0	1	1	0	0	1

USB Mode Frequency Control Register Settings

SAMPLING RATE		XCK FREQUENCY	SFDA SFAD	FREQUENCY CONTROL REGISTER PROGRAMMING VALUES						
ADC	DAC			FREQCON[5:0]						
KHz	KHz	MHz	NO. OF XCK	No.	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
48	48	12	250	32	1	0	0	0	0	0
48	8	12	250	33	1	0	0	0	0	1
8	48	12	250	34	1	0	0	0	1	0
8	8	12	250	35	1	0	0	0	1	1
96	96	12	250	36	1	0	0	1	0	0
44.1	44.1	12	272	37	1	0	0	1	0	1
44.1	8	12	272	38	1	0	0	1	1	0
8	44.1	12	272	39	1	0	0	1	1	1
8	8	12	272	40	1	0	1	0	0	0
88.2	88.2	12	272	41	1	0	1	0	0	1

ADDRESS 04, DAC AND MISCELLANEOUS POWER DOWN CONTROL REGISTER (CREG4[7:0])

A[7:0]	CREG4[7:0]							
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Hex 04	Reserved	pwdnpullupr	pwdncapless	pwdnvcm	pwdnline	hpdetmode	capless	mute
Default Value	0	0	0	0	0	0	0	0

PWDNPULLUPR: Power down pullup resistor at the MODE pin.

0: turn on the pullup resistor at the MODE pin (default).
1:disable the pullup resistor at the MODE pin.

This bit is used to reduce power consumption in the pullup resistor at the MODE pin if user uses I2C for chip programming. For I2C, the chip needs an external pulldown resistor at the MODE pin. User can program this bit to “1” to disable the internal pullup resistor. For user using the 3-wire MPU interface, the external pullup resistor is not needed. By default, the chip is in MPU mode with the internal pullup resistor enabled.

PWDNCAPLESS: Power down the analog “capless” circuit block.

0: do not power down the analog “capless” circuit block (default).
1: power down the “analog “capless” circuit block.

This bit must be used together with “CAPLESS” (CREG4[1]) for headphone output application. If user is using external coupling capacitors at headphone output pins HPOUTL and HPOUTR, CAPLESS should be programmed to “1” (CAPLESS circuit block is not used), PWDNCAPLESS should be programmed to “1” to conserve power consumption.

PWDNVCM:Power down the resistor at the analog common mode voltage reference.

0: do not power down the resistor at the analog common mode voltage reference(default).
1: power down the resistor at the analog common mode voltage reference.

PWDNLINE:Power down the line outputs simultaneously.

0: do not power down the line outputs (default).
1: power down the line outputs simultaneously.

When headphone is used, this bit must be programmed to “1” to conserve power consumption.

HPDETMODE:Headphone detection mode.

0: invert the HPDET pin signal inside the chip (default).
1: do not invert the HPDET pin signal inside the chip.

This bit provides the flexibility to invert or not invert the HPDET pin signal inside the chip.

CAPLESS: External coupling capacitor of headphone is used or not used at HPOUTL and HPOUTR.

0: external coupling capacitor is not used, the chip internal “capless” circuit block is needed (default).
1: external coupling capacitor is used, the chip internal “capless” circuit block is not needed.

This bit must be programmed together with PWDNCAPLESS (CREG4[5]). By default, external coupling capacitor at headphone outputs are not used. If they are used, both CAPLESS and PWDNCAPLESS must be programmed to “1” to conserve power consumption

MUTE: Mute the DAC AOUTL and AOUTR outputs

0: do not mute the DAC AOUTL and AOUTR outputs (default).
1: mute the DAC AOUTL and AOUTR outputs, the headphone HPOUTL and HPOUTR are not “muted”.

.ADDRESS 05, DAC PATH HEADPHONE CONTROL REGISTER (CREG5[7:0])

A[7:0]	CREG5[7:0]							
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Hex 05	Reserved	hpagcd[6:0]						
Default Value	0	1	0	0	0	0	0	0

HPAGCD[6:0]: 7-bit headphone automatic gain control AGC data. Default value of HPAGCD[6:0] is hex40 which is 0 dB.

ADDRESS 06, ADC PATH SERIAL OUTPUT PORT CONTROL REGISTER (CREG6[7:0])

A[7:0]	CREG6[7:0]							
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Hex 06	master	adhrsc	adsfdly	adinvsc	admode[1:0]		adformat[1:0]	
Default Value	0	0	0	0	0	0	0	0

MASTER: master or slave mode control

0: the chip is operated as “slave”. In slave mode, AV2722 accepts SFDA, SFAD, and SC.
1:the chip is operated as “master”. In master mode, AV2722 generates SFDA, SFAD and SC.

In either mode, DAC and ADC can be operated at different sampling rate.

ADHRSC:ADCs use higher rate SC

0:ADC path uses whatever SC is provided, either master or slave mode (default).
1:ADC path uses higher rate SC. When the DAC path is at higher sampling than the ADC path, program this bit to “1” allows SDO output to shift out data at the higher SC rate.

ADSFDLY: Delay SFAD by 1 SC in the ADC path.

0: do not delay the SF by 1 SC cycle (default).
1: delay the SFAD by 1 SC cycle.

ADINVSC: Invert the SC bit clock.

0: do not invert the SC bit clock (default).
1: invert the SC bit clock.

ADMODE[1:0]: These two bits define the ADC path serial output data mode.

00: left justified mode(defalut).
01: I2S mode.
10: normal mode
11: DSP mode

ADFORMAT[1:0]: These two bits define the audio serial output data bit length.

00: 24 bits (default).
01: 20-bits.
10: 18 bits.
11: 16 bits.

ADDRESS 07, ADC PATH HIGH PASS FILTER CONTROL REGISTER (CREG7[7:0])

A[7:0]	CREG7[7:0]							
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Hex 07	Reserved						HPFOSEN	HPFEN
Default Value	0	0	0	0	0	0	1	1

HPFOSEN: high-pass filter (HPF) offset enable in the ADC path.
0: allow HPF to use previous stored data.
1: allow HPF to use new coming data. (default)

HPFEN: high-pass filter (HPF) enable in the ADC path.
0: bypass the high-pass filter.
1: enable the high-pass filter (default).

ADDRESS 08, ADC PATH LEFT CHANNEL GAIN AND MUTE CONTROL REGISTER (CREG8[7:0])

A[7:0]	CREG8[7:0]							
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Hex 08	ADCMUTEL	reserved		ADCGAINL[4:0]				
Default Value	0	0	0	1	0	0	1	0

ADCMUTEL: ADC left channel mute control.
0: do not mute the ADC left channel (default).
1: mute the ADC left channel, SDO will shift out all zero data in the left channel.

ADCGAINL[4:0]: 5-bit ADC left channel input gain (volume) control. The default value of ADCGAINL[4:0] is binary 10010 which is corresponding to 0 dB.

ADDRESS 09, ADC PATH RIGHT CHANNEL GAIN AND MUTE CONTROL REGISTER (CREG9[7:0])

A[7:0]	CREG9[7:0]							
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Hex 09	ADCMUTER	reserved		ADCGAINR[4:0]				
Default Value	0	0	0	1	0	0	1	0

ADCMUTER: ADC right channel mute control.
0: do not mute the ADC right-channel (default).
1: mute the ADC right channel, SDO will shift out all zero data in the right channel.

ADCGAINR[4:0]: 5-bit ADC rightchannel input gain (volume) control. The default value of ADCGAINR[4:0] is binary 10010 which is corresponding to 0 dB.

ADDRESS 0A, ADC POWER DOWN CONTROL REGISTER (CREG10[7:0])

A[7:0]	CREG10[7:0]							
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Hex 0A	Reserved					ADCLPWDN	ADCRPWDN	PWDNMICBIAS
Default Value	0	0	0	0	0	1	1	0

ADCLPWDN: ADC left channel power down.
0: do not shut down power of ADC left channel.
1: shut down power of ADC left channel (default)

ADCRPWDN: ADC right channel power down
0: do not shut down power of ADC right channel.
1: shut down power of ADC right channel (default).

PWDNMICBIAS: Microphone bias circuit power down.
0: do not shut down microphone bias circuit (default).
1: shut down power of microphone bias circuit.

ADDRESS 0B, ADC LEFT AND RIGHT MICROPHONE GAIN CONTROL REGISTER (CREG11[7:0])

A[7:0]	CREG11[7:0]							
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Hex 0B	Reserved	USEADCL	MICGAINL[1:0]		reserved	USEADCR	MICGAINR[1:0]	
Default Value	0	0	0	0	0	0	0	0

USEADCL: use ADC microphone left channel.
0: ADC left channel microphone is not used (default).
1: ADC left channel microphone is used.

By default, ADC microphone left channel is shut down (ADCLPWDN=1). If ADCLPWDN is programmed to “0”, this bit must be programmed to “1” to use the left channel microphone

MICGAINL[1:0]:2-bit left channel microphone gain

00: no gain increase (default).
01: 6 dB gain increase for the left channel microphone input.
10: 12 dB gain increase for the left channel microphone input.
11: 18 dB gain increase for the left channel microphone input.

USEADCR: use ADC microphone right channel.

0: ADC left channel microphone is not used (default).
1: ADC right channel microphone is used.

By default, ADC microphone right channel is shut down (ADCRPWDN=1). If ADCRPWDN is programmed to “0”, this bit must be programmed to “1” to use the right channel microphone.

MICGAINL[1:0]:2-bit right channel microphone gain.

00: no gain increase (default).
01: 6 dB gain increase for the right channel microphone input.
10: 12 dB gain increase for the right channel microphone input.
11: 18 dB gain increase for the right channel microphone input.

ADDRESS 0C, SOFTWARE RESET CONTROL REGISTER (CREG12[7:0])

A[7:0]	CREG12[7:0]							
	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Hex0C	Reserved							SOFRST
Default Value	0	0	0	0	0	0	0	0

SOFRST: [1:0]: software reset.

0: no software reset.
1: software reset.

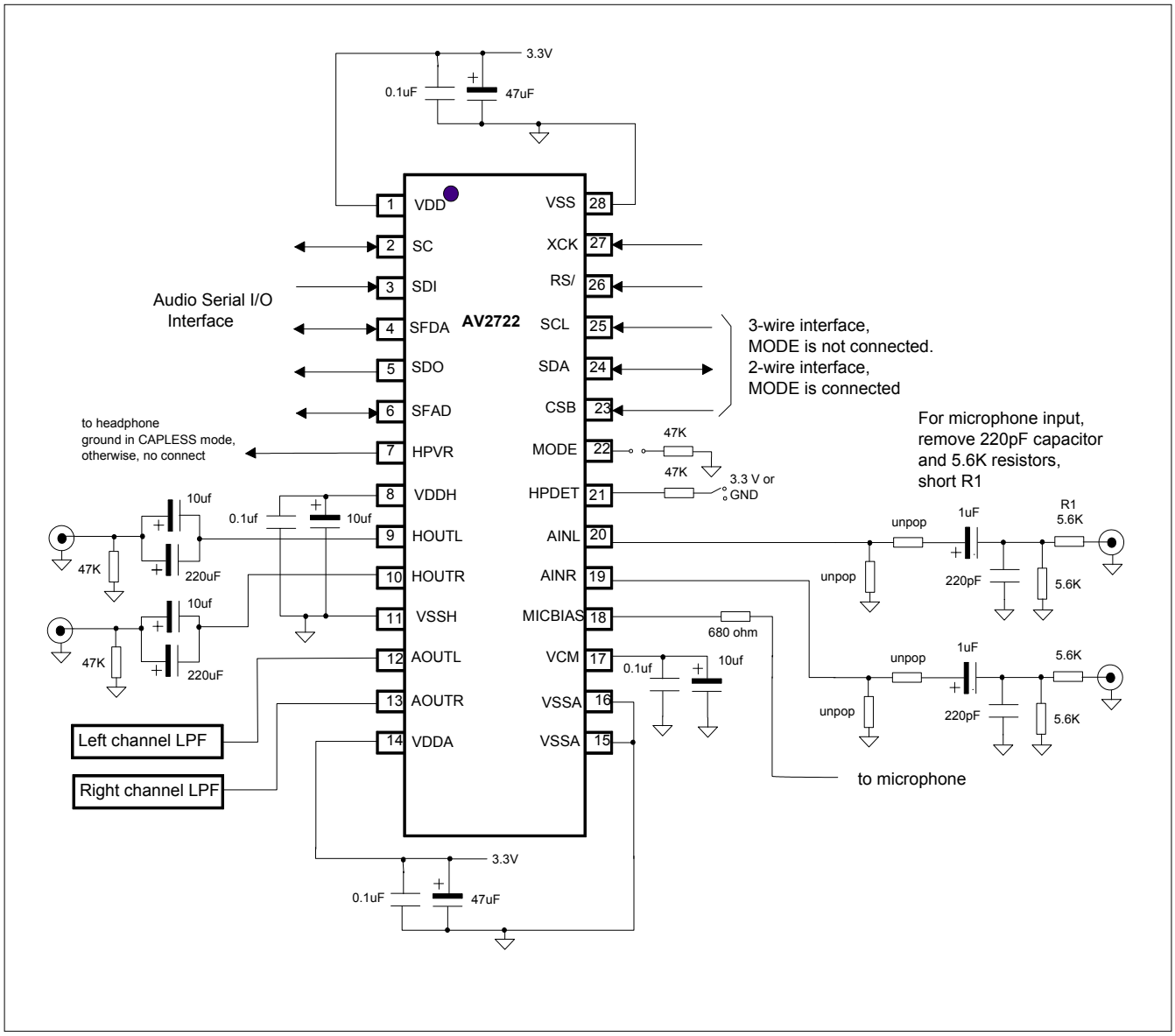
DIGITAL INTERPOLATION FILTER CHARACTERISTICS

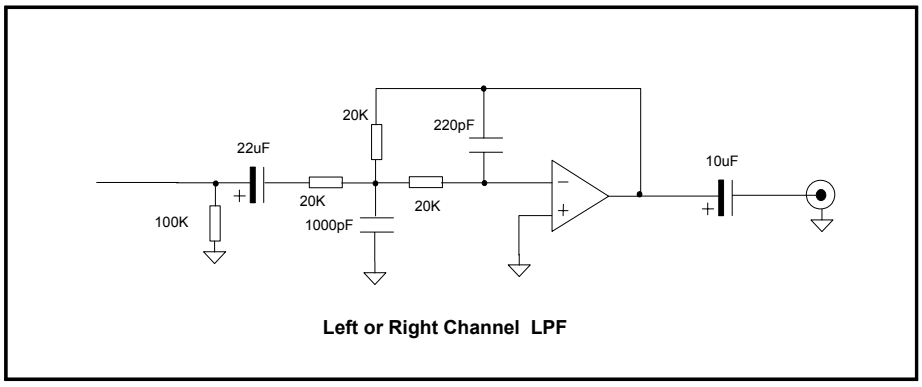
(TO BE INSERTED)

DIGITAL FILTER FREQUENCY RESPONSE

(TO BE INSERTED)

CONNECTION EXAMPLE





Left or Right Channel LPF

ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Min	Max	Units
V_{DD} **VDDA** **VDDH**	Power Supply Voltage (Measured to Vss)	-0.3	+3.6	V
V_{id}	Digital Input Applied Voltage[1]	GND-0.3	V_{DD}+0.3	V
V_{ia}	Analog Input Applied Voltage[1]	GND-0.3	V_{DDA}+0.3	V
V_o	Digital Output Voltage	GND-0.3	V_{DD}+0.3	V
T_A	Operating Temperature Range	-25	+85	°C
Tstg	Storage Temperature before soldering		30	°C
T_{stor}	Storage Temperature after soldering	-65	+150	°C
T_j	Junction Temperature (Plastic Package)	-65	+150	°C
Tsol	Lead Soldering Temperature (10 sec., 1/4” from pin)		240	°C
Tvsol	Vapor Phase Soldering (1 minute)		180	°C

Notes:

Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Typical	Max	Units
V_{DD} V_{DDA} V_{DDH}	Power supply voltage			3.6	V
Vss V_{SSA} V_{SSH}	Ground		0		V
T_a	Ambient operating temperature range	0		70	°C

ELECTRICAL CHRACTERISTICS

Parameter	Characteristics / Test Conditions	Min	Typ	Max	Units
Digital Input					
V_{IH}	Digital Input Voltage, Logic HIGH, TTL Compatible Inputs.	2.0		V_{DD}	V
V_{IL}	Digital Input Voltage, Logic LOW, TTL Compatible Inputs	V_{SS}		0.8	V
I_{IH}	Digital Input Current, Logic HIGH, (V_{IN}=4.0V)			TBD	μA
I_{IL}	Digital Input Current, Logic LOW, (V_{IN}=0.4V)			TBD	μA
Serial Audio Port Timing (Slave Mode)					
tsc	SC Pulse Cycle Time	100			ns
tsc_H	SC Pulse Width, HIGH	50			ns
tsc_L	SC Pulse Width, LOW	50			ns
t_{SU}	Audio Data Setup Time With Respect To Rising Edge of SC	30			ns
t_{HD}	Audio Data Hold Time With Respect to Rising Edge of SC	30			ns
tsfsc	Audio SFSetup Time With Respect To Rising Edge of SC	30			ns
tscsf	Audio SF Hold Time With Respect To Rising Edge of SC	30			ns
Serial Audio Port Timing (Master Mode)					
tm_{SU}	SDI audio data setup time	10			ns
tm_{HD}	SDI audio data hold time	10			ns

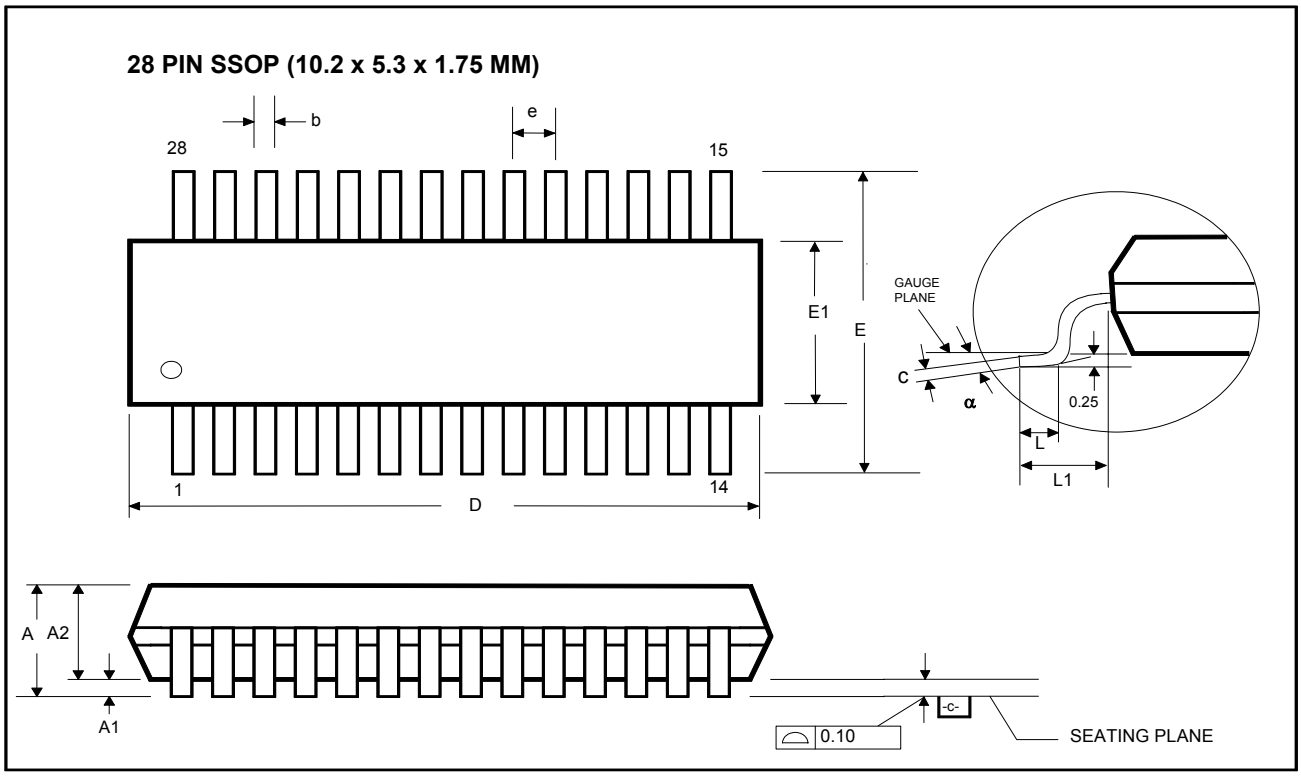
Parameter	Characteristics / Test Conditions	Min	Typ	Max	Units
tmsfd	SFDA/SFAD propagation delay from SC falling edge			10	ns
tmsdod	SDO propagation delay from SC falling edge			10	ns
Serial Command Port Timing (MPU type Mode)					
T_{SCL}	SCL cycle time	100			ns
t_{SCLH}	SCL high time	80			ns
t_{SCLL}	SCL low time	40			ns
t_{sdasu}	SDA to SCL setup time	20			ns
t_{sdahd}	SCL to SDA hold time	20			ns
t_{csbl}	CSB pulse low time	20			ns
t_{csbh}	CSB pulse high time	20			ns
tsclcsb	SCL rising edge to CSB rising edge	20			ns
tcsbscl	CSB rising edge to SCL rising edge	20			ns
Serial Command Port Timing (I2S Mode)					
fsc	SCL clock frequency			100	KHz
tsu;sta	START condition setup time	4.7			μs
thd;sta	START condition hold time	4.0			μs
tsu;sto	STOP condition setup time	4.0			μs
tLOW	SCL low time	4.7			μs
tHIGH	SCL high time	4.0			μs
tr	SCL and SDA rise time			1.0	μs
tf	SCL and SDA fall time			0.3	μs
tsu;DAT	Data setup time	250			ns
thd;DAT	Data hold time	0			ns
Tvd;DAT	SCL low to data output valid			3.4	μs
tBUF	Bus free time	4.7			μs
ADC Line Input					
Vin(line)	Input signal level for line input (0dB)		TBD		Vrms
SNR	A-weighted, 0 dB gain @fs=48KHz		TBD		dB
	A-weighted, 0 dB gain @fs=96KHz		TBD		dB
	A-weighted, 0 dB gain @fs=48KHz, VDDA=2.7V		TBD		dB

Parameter	Characteristics / Test Conditions	Min	Typ	Max	Units
THD	Total Harmonic Distortion		TBD		dB
DR	Dynamic Range, A weighted -60 db full scale input		TBD		dB
PSRR	Power Supply Rejection Ratio, 1KHz 100 mVpp		TBD		dB
	Power Supply Rejection Ratio, 20 Hz to 20KHz 100 mVpp		TBD		dB
	ADC Channel Separation (@ 1KHz input)		TBD		dB
	Mute Attenuation (0 dB @ 1KHz input)		TBD		dB
R_{INLINE}	Input resistance, 0 dB gain		TBD		Ω
	Input resistance, 12 dB gain		TBD		Ω
C_{INLINE}	Input Capacitance		TBD		pF
ADC Microphone Input @ 0dB gain, fs=48KHz					
Vin(mic)	Input signal level for microphone input (0dB)		TBD		Vrms
SNR	A weighted, 0 dB gain		TBD		dB
THD	0db input, 0 db gain		TBD		dB
PSRR	Power Supply Rejection Ratio, 1KHz 100 mVpp		TBD		dB
	Power Supply Rejection Ratio, 20 Hz to 20KHz 100 mVpp		TBD		dB
DR	Dynamic Range, A weighted, -60 dB full scale input		TBD		dB
	Mute Attenuation (@0dB, 1KHz input)		TBD		dB
R_{INMIC}	Input Resistance		TBD		Ω
C_{INMIC}	Input Capacitance		TBD		pF
MICROPHONE BIAS					
$V_{MICBIAS}$	Microphone bias voltage		TBD		V
$I_{MICBIAS}$	Microphone bias current		TBD		pF
Vn	Output Noise Voltage (1K to 20 KHz)		TBD		$nV/Hz^{1/2}$
Line Output for DAC Playback (Load =10KΩ, 50pF)					
Vout	0 db full scale output voltage		TBD		Vrms
SNR	A-weighted, 0 dB gain @fs=48KHz		TBD		dB
	A-weighted, 0 dB gain @fs=96KHz		TBD		dB
	A-weighted, 0 dB gain @fs=48KHz, VDDA=2.7V		TBD		dB
DR	Dynamic Range, -60 dB full scale input		TBD		dB

Parameter	Characteristics / Test Conditions	Min	Typ	Max	Units
THD	Total Harmonic Distortion, 1KHz, 0dBfs		TBD		dB
	Total Harmonic Distortion, 1KHz, -3dBfs		TBD		dB
PSRR	Power Supply Rejection Ratio, 1KHz 100 mVpp		TBD		dB
	Power Supply Rejection Ratio, 20 Hz to 20KHz 100 mVpp		TBD		dB
	Mute Attenuation (1KHz, 0 dB)		TBD		dB
Stereo Headphone Output					
Vout	0 dB Full scale output voltage		TBD		Vrms
Pout	Output power with R_L= 32 Ω,		TBD		mW
	Output power with R_L= 16 Ω,		TBD		mW
SNR	Signal To Noise Ratio, A-weighted		TBD		dB
THD	1KHz, with R_L= 32 Ω, Pout =10mW rms (-5dB)		TBD		% dB
	1KHz, with R_L= 32Ω Pout = 20 mW rms (-2dB)		TBD		% dB
PSRR	Power Supply Rejection Ratio, 1KHz 100 mVpp		TBD		dB
	Power Supply Rejection Ratio, 20 Hz to 20KHz 100 mVpp		TBD		dB
	Mute Attenuation 1KHz, 0 dB		TBD		dB

Test Conditions: VDD, VDDH, VDDA= 3.3 V, VSS=0 V, T_A25 ^oC, slave mode, 48 KHz sampling rate, 256 fs.

PACKAGING INFORMATION



SYMBOLS	DIMENSIONS (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A1	0.05	0.13	0.25
A2	1.65	1.75	1.85
b	0.22	-----	0.38
c	0.09	-----	0.25
D	9.90	10.20	10.50
E	7.40	7.80	8.20
e	0.65 BSC		
E1	5.00	5.30	5.60
L	0.55	0.75	0.95
L1	1.25 REF		
α	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		