SUMITOMO ELECTRIC

*01.08.28*

# F0522501Q

**2.7 Gb/s NRZ Data Rate**

## *Laser Diode Driver*


## ♦ *Features*

- Up to 2.7 Gb/s (FEC available) high speed operation
- Clocked (MS-D/FF) or Non-clocked operation can be selected
- Disable function of modulation current and bias current
- Bias current monitoring
- Mark density monitoring
- +5 V or -5 V single power supply
- Up to 60 mA p-p modulation current
- Up to 50 mA bias current
- Differential ECL compatible interface
- On-chip 50 Ω terminations
- Internal voltage reference for AC coupling

## ♦ *Applications*

- Laser diode driver of an optical transmitter circuit up to 2.7 Gb/s (FEC available)

## ♦ *Functional Description*

The F0522501Q is a high performance GaAs laser diode driver IC applicable in an optical transmitter circuit up to 2.7 Gb/s NRZ data rate (especially suitable for SDH [STM-16] / SONET [OC-48]) , featuring the capable operation for the FEC signal.

The F0522501Q specifies the rise time and the fall time of 70 ps (20 %-80 %) typically. It features the single +5 V or -5 V supply operation, the modulation current between 1 mA and 60 mA, and the bias current between 1 mA and 50 mA while the dissipating power is around the typical value of 1 W.

## ♦ *Absolute Maximum Ratings*

$T_a$=25 °C, unless specified

| Parameter | Symbol | Value | Units |
|---|---|---|---|
| Supply Voltage | $V_{DD}$-$V_{SS}$ | - 0.5 to +7.0 | V |
| Supply Current | Icon | 250 | mA |
| Input Voltage ($D_{IN}$ ,$D_{INB}$ ,$CK_{IN}$ ,$CK_{INB}$) | $V_{IN}$ | $V_{SS}$ to $V_{DD}$+0.5 | V |
| Input Voltage ($DIS_{IN}$ ,$SEL_{IN}$) | $V_{INC1}$ | $V_{SS}$ to $V_{DD}$+0.5 | V |
| Input Voltage ($V_{MIN}$ ,$V_{BIN}$) | $V_{INC2}$ | $V_{SS}$ to $V_{SS}$+1.5 | V |
| Output Voltage (OUT,$OUT_B$,$OUT_{BIAS}$) | $V_{OUT}$ | $V_{DD}$-2.0 to $V_{DD}$+0.5 | V |
| Output Voltage (MRK,$MRK_B$,BM,$BM_B$) | $V_{OUTM}$ | $V_{SS}$ to $V_{DD}$+0.5 | V |
| Termination Voltage ($V_{TTD}$ ,$V_{TTCK}$) | $V_{TT}$ | $V_{DD}$-2.5 to $V_{DD}$+0.5 | V |
| Storage Temperature | Tstg | -55 to +125 | ° C |
| Ambient Operating Temperature | $T_a$ | 0 to +70 | ° C |

## ♦ *Recommended Operating Conditions*

| Parameter | Symbol | Value | | | Units |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Supply Voltage | $V_{DD}$-$V_{SS}$ | 4.75 | 5.00 | 5.46 | V |
| Output Voltage | $V_{OUT}$ | $V_{DD}$-1.6 | $V_{DD}$-1.0 | $V_{DD}$ | V |
| Ambient Operating Temperature | $T_a$ | 0 | 25 | 70 | °C |

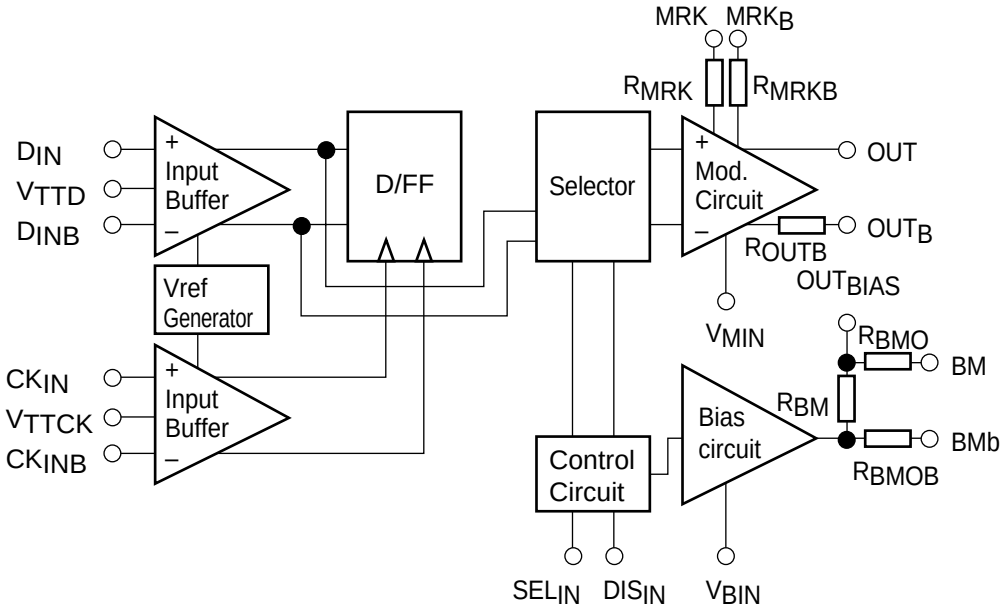
## ♦ *Electrical Characteristics*

$T_a$=25 °C, $V_{DD}$- $V_{SS}$=4.75 to 5.46 V

| Parameter | Symbol | Test Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Circuit Current (1) | $I_{CKT}$ | $V_{MIN}=V_{BIN}=V_{SS}$ | - | 100 | 130 | mA |
| Input Voltage (ECL) | $V_{IH}$ | Differential Input | $V_{DD}$-1.0 | $V_{DD}$-0.9 | $V_{DD}$-0.7 | V |
| | $V_{IL}$ | | $V_{DD}$-1.9 | $V_{DD}$-1.7 | $V_{DD}$-1.6 | V |
| Input Voltage (AC) | $V_{IN}$ | Differential Input | 0.6 | 0.8 | 1.2 | Vp-p |
| Input Resistor | $R_{IN}$ | - | - | 50 | - | Ω |
| Modulation Peak Current(2) | $I_{MMAX}$ | $V_{MIN}=V_{SS}$+1.5V | 60 | - | - | mA |
| | $I_{MMIN}$ | $V_{MIN}=V_{SS}$ | - | - | 1.0 | mA |
| | $I_{MDIS}$ | $V_{DISIN}=V_{DD}$-1.5V | - | - | 0.5 | mA |
| Bias Current | $I_{BMAX}$ | $V_{BIN}=V_{SS}$+1.5V | 50 | - | - | mA |
| | $I_{BMIN}$ | $V_{BIN}=V_{SS}$ | - | - | 1.0 | mA |
| | $I_{BDIS}$ | $V_{DISIN}=V_{DD}$-1.5V | - | - | 0.5 | mA |
| Input Voltage (SEL) | $V_{SELIH}$ | Non-Clocked op. | $V_{DD}$-1.5 | - | $V_{DD}$ | V |
| | $V_{SELIL}$ | Clocked opelation | $V_{SS}$ | OPEN | $V_{SS}$+1.5 | V |
| Input Voltage (DIS) | $V_{DISIH}$ | Disable opelation | $V_{DD}$-1.5 | - | $V_{DD}$ | V |
| | $V_{DISIL}$ | Enable opelation | $V_{SS}$ | OPEN | $V_{SS}$+1.5 | V |
| Bias Monitor Resistor | $R_{BM}$ | | - | 10 | - | Ω |
| Mark Density Monitor Voltage | $\Delta(V_{MRK}-V_{MRKB})$ | Differential Mode Date: All "H" | - | 1.2 | - | V |
| Rise Time(3) | tr | RL = 15Ω 20% - 80% | - | 70 | 150 | ps |
| Fall Time(3) | tf | RL = 15Ω 80% - 20% | - | 70 | 150 | ps |
| Setup Time | ts | | - | 100 | - | ps |
| Hold Time | th | | - | 50 | - | ps |
| Maximum Clock Frequency | fmax | $V_{SEL}$=OPEN or $V_{SS}$ to $V_{SS}$+1.5V | 2.7 | - | - | GHz |
| Maximum Data Rate | fopr | $V_{SEL}=V_{DD}$-1.5V to $V_{DD}$ | 2.7 | - | - | Gbps |

(1) Excluding the input current, the modulation current and the bias current.
(2) Modulation peak current is measured at "OUT" pin.
(3) Rise time and fall time are measured at "OUT" pin.

## ♦ *Block Diagram*




## ♦ *Pin Descriptions*

$D_{IN}$ : Positive data input
$D_{INB}$ : Negative data input
$V_{TTD}$ : Termination for data input
$CK_{IN}$ : Positive clock input
$CK_{INB}$ : Negative clock input
$V_{TTCK}$ : Termination for clock input
OUT : Positive modulation output (LD should be connected to this pin.)
$OUT_B$ : Negative modulation output ($R_{OUTB}$=15 Ω typ.)
$OUT_{BIAS}$ : Bias output ($R_{BM}$=10 Ω typ., $R_{BMO}$=$R_{BMOB}$=3 kΩ typ.)
$V_{MIN}$ : Voltage input that sets the LD modulation peak current
$V_{BIN}$ : Voltage input that sets the LD bias current
$DIS_{IN}$ : Voltage input that controls turning on/off the modulation current and the bias current
$SEL_{IN}$ : Voltage input that selects clocked or non-clocked operation
BM : Bias current monitor positive output
$BM_B$ : Bias current monitor negative output
MRK : Mark density monitor positive output ($R_{MRK}$=25 kΩ typ.)
$MRK_B$ : Mark density monitor negative output ($R_{MRKB}$=25 kΩ typ.)

## ♦ *Function Table*

(1) Clocked Operation ($V_{IN}$@$SEL_{IN}$=OPEN or $V_{SS}$ to $V_{SS}$+1.5V)

| Input | | Output | |
|---|---|---|---|
| $D_{IN}$ | $CK_{IN}$ | Current@OUT | Current@OUTB |
| H | ↑ | ON | OFF |
| L | ↑ | OFF | ON |
| Φ | L | $Q_O$ | $Q_{OB}$ |

↑ : Clock transition from low to high

Φ : Don't care

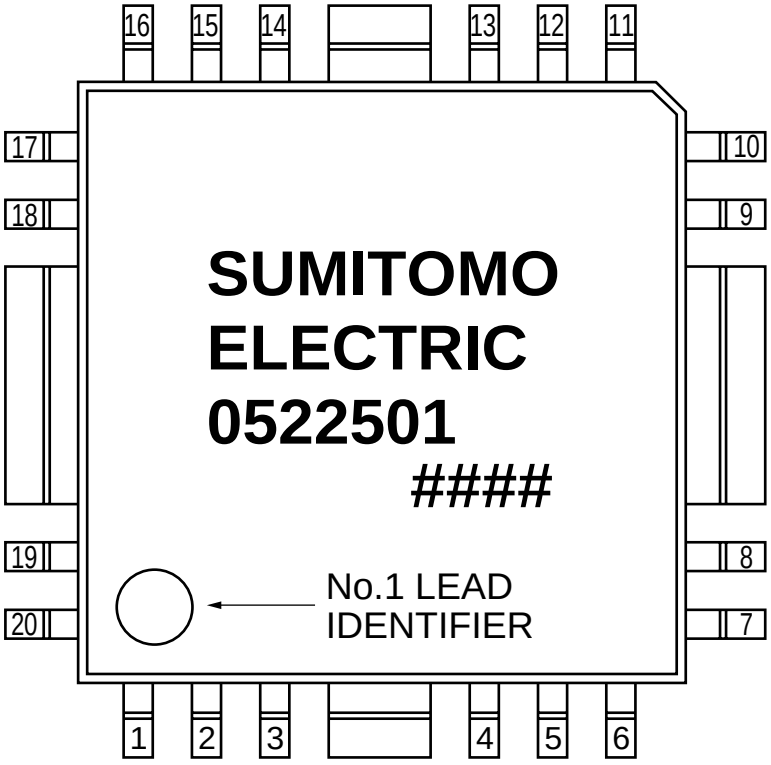
$Q_O$ : Previous current output status @OUT before clock pulse

$Q_{OB}$ : Previous current output status @OUTB before clock pulse

(2) Non-clocked Operation ($V_{IN}$@$SEL_{IN}$=$V_{DD}$-1.5V to $V_{DD}$)

| Input | | Output | |
|---|---|---|---|
| $D_{IN}$ | $CK_{IN}$ | Current@OUT | Current@OUTB |
| H | Φ | ON | OFF |
| L | Φ | OFF | ON |

## ♦ *Pin Assignments (Top View)*




1 :$D_{INB}$
2 :$V_{TTD}$
3 :$D_{IN}$
4 :$CK_{IN}$
5 :$V_{TTCK}$
6 :$CK_{INB}$
7 :$SEL_{IN}$
8 :$V_{DDC}$
9 :$V_{DDO}$
10 :$BM_{B}$
11 :BM
12 :$OUT_{BIAS}$
13 :OUT
14 :$OUT_{B}$
15 :DNC
16 :$VM_{IN}$
17 :$VB_{IN}$
18 :$MRK_{B}$
19 :MRK
20 :$DIS_{IN}$

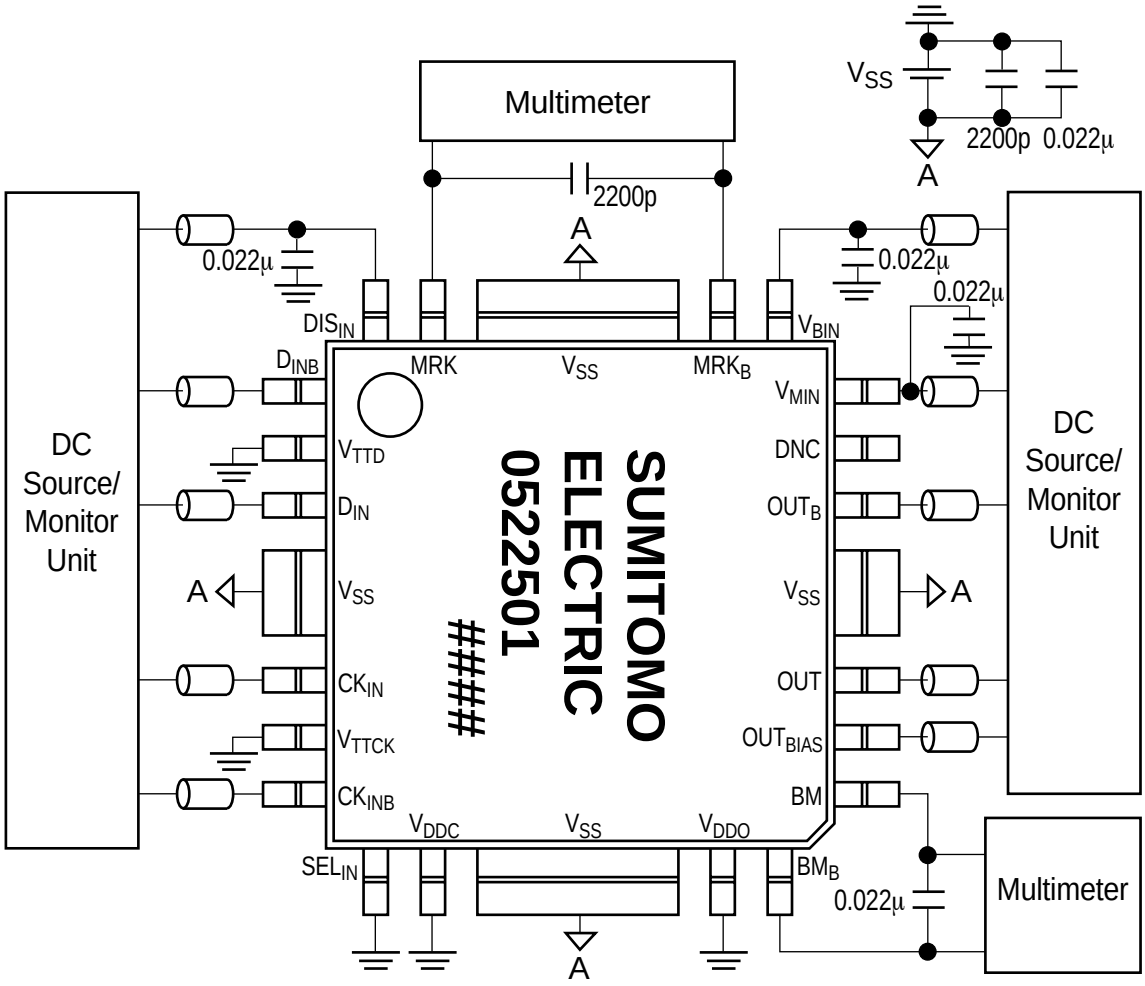
(*) The pins without numbering should be connected to $V_{SS}$.

(**) $V_{DDC}$ and $V_{DDO}$ are not connected internally.

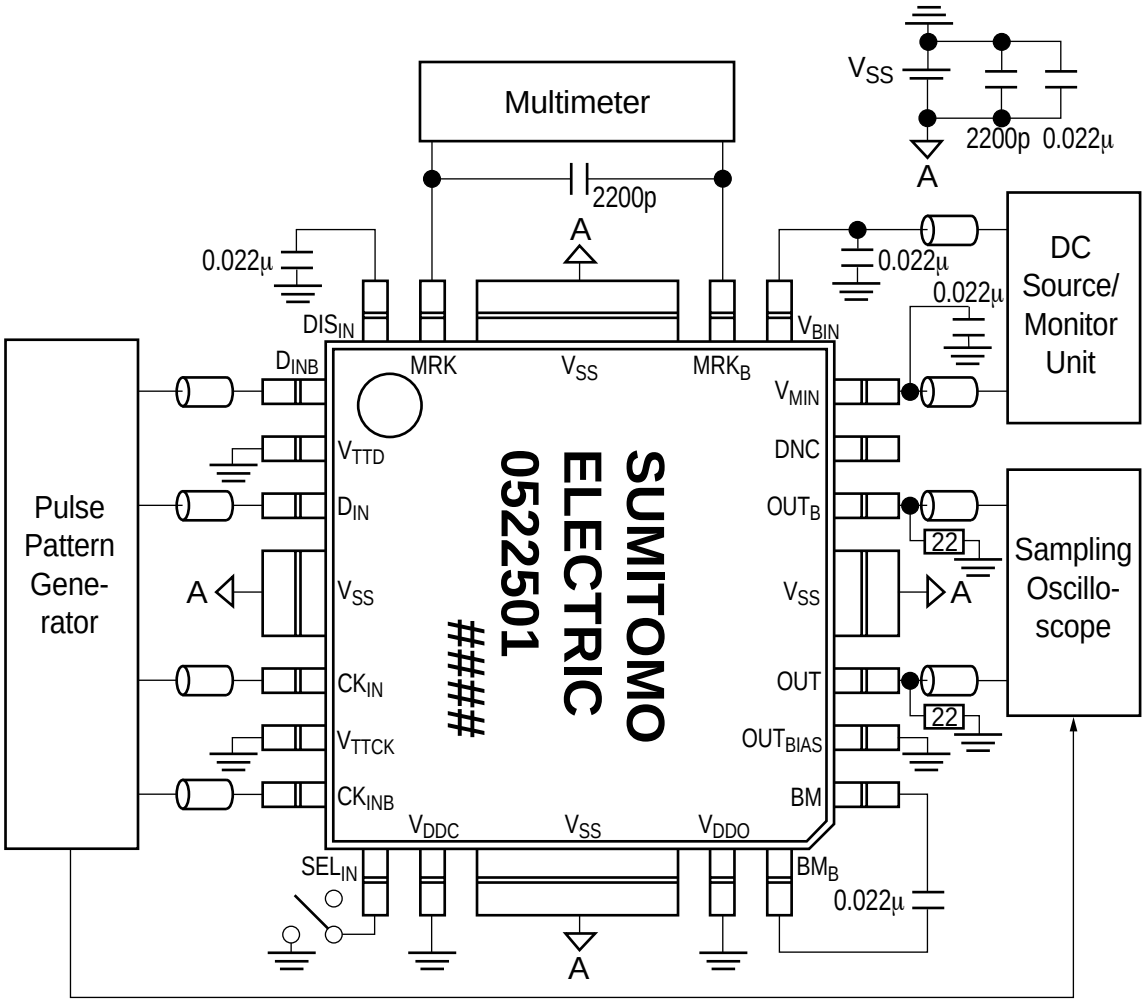
(***) DNC is a no user connection pin.

## ♦ *Test Circuits*

(1) DC Characteristics

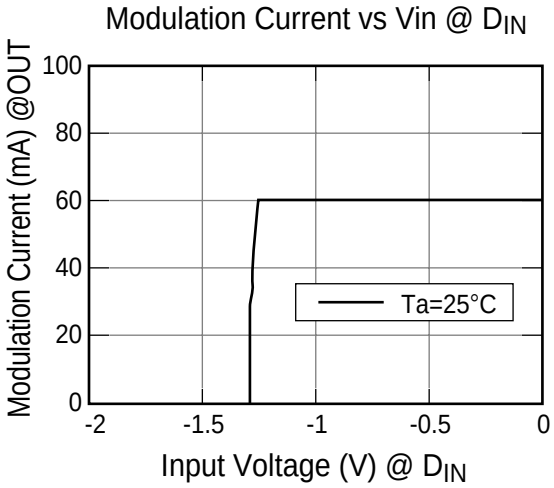


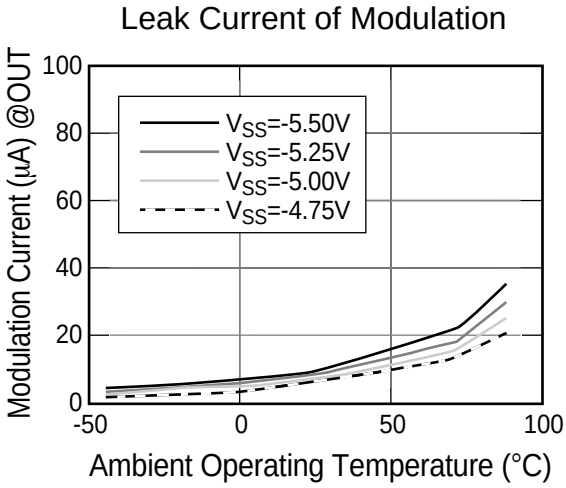
(2) AC Characteristics



## ♦ *Typical Characteristics*

(1) Modulation Current



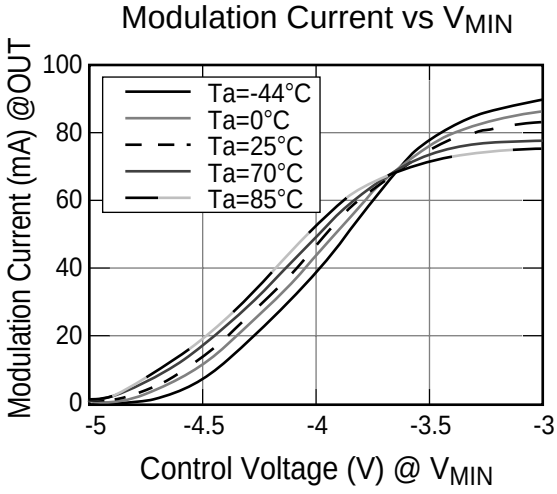



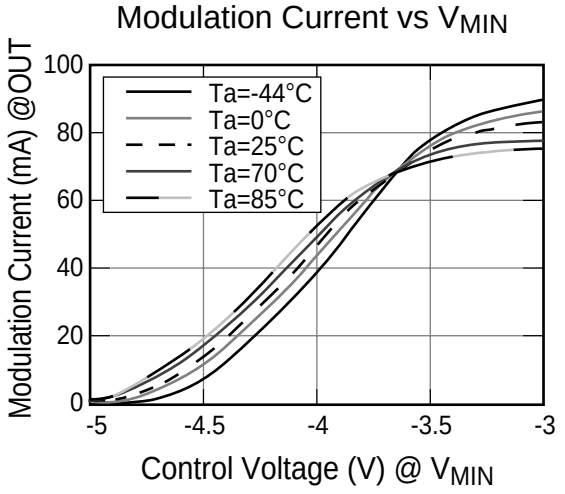

Conditions

$V_{DD}$=GND, $V_{SS}$=-5 V, $V_{IN}$@$D_{INB}$=-1.3 V
$V_{MIN}$@$I_{Mpeak}$=60 mA, $V_{BIN}$=$V_{SS}$
$V_{OUT}$@OUT, $OUT_B$ , $OUT_{BIAS}$=GND

Conditions

$V_{DD}$=GND, $V_{IN}$@$D_{IN}$=-1.6 V, $V_{IN}$@$D_{INB}$=-1.3 V
$V_{MIN}$@$I_{Mpeak}$=60 mA, $V_{BIN}$=$V_{SS}$
$V_{OUT}$@OUT, $OUT_B$ , $OUT_{BIAS}$=GND




Conditions

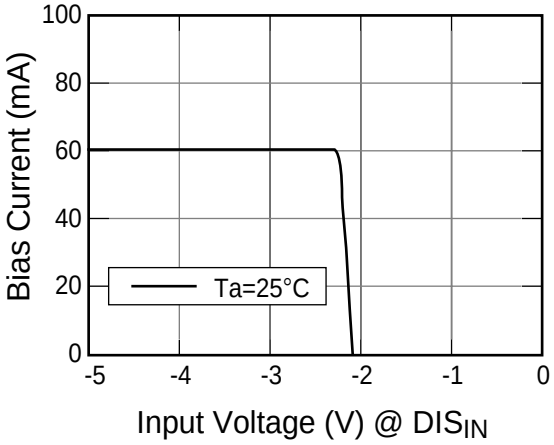
$V_{OUT}$@OUT=GND
$V_{DD}$= GND , $V_{SS}$= -5 V, $V_{IN}$@$D_{IN}$=-1.0 V
$V_{IN}$@$D_{INB}$=-1.3 V, $V_{BIN}$=$V_{SS}$
$V_{OUT}$@$OUT_B$ , $OUT_{BIAS}$=GND

Conditions

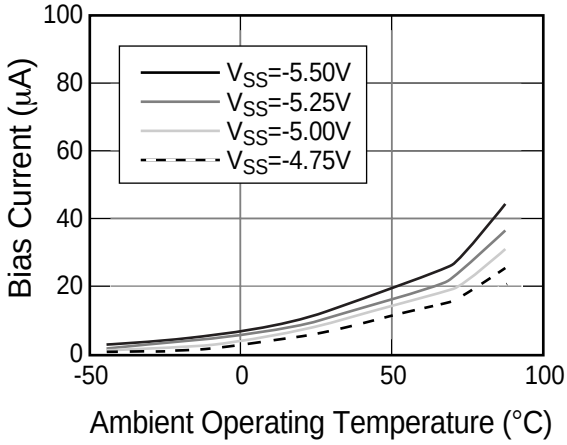
$V_{OUT}$@OUT=-1.6 V
$V_{DD}$= GND, $V_{SS}$= -5 V, $V_{IN}$@$D_{IN}$=-1.0 V
$V_{IN}$@$D_{INB}$=-1.3 V, $V_{BIN}$=$V_{SS}$
$V_{OUT}$@$OUT_B$ , $OUT_{BIAS}$=GND

(2) Bias Current

Bias Current vs Vin @ $DIS_{IN}$




Leak Current of Bias



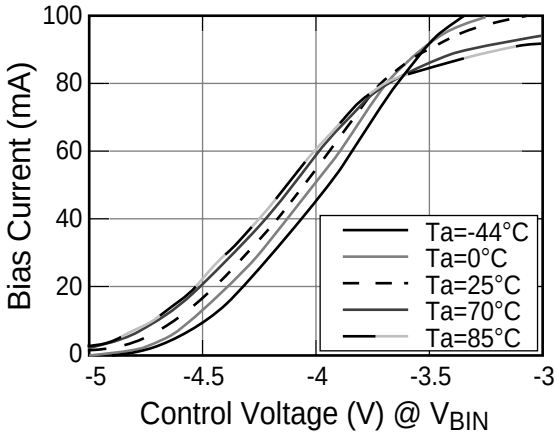

Conditions

$V_{DD}$=GND, $V_{SS}$=-5 V, $V_{IN}@D_{IN}$=-1.0 V
$V_{IN}@D_{INB}$=-1.3 V, $V_{MIN}=V_{SS}$
$V_{BIN}@I_B$=60mA
$V_{OUT}@OUT$, $OUT_B$ , $OUT_{BIAS}$=GND

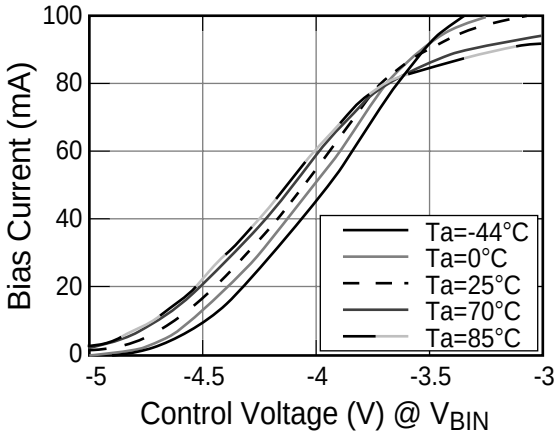
Conditions

$V_{DD}$=GND, $V_{IN}@D_{IN}$=-1.0 V, $V_{IN}@D_{INB}$=-1.3 V
$V_{IN}@DIS_{IN}$=-1.5 V, $V_{MIN}=V_{SS}$
$V_{BIN}@I_B$=60 mA
$V_{OUT}@OUT$, $OUT_B$ , $OUT_{BIAS}$=GND

Bias Current vs $V_{BIN}$




Bias Current vs $V_{BIN}$



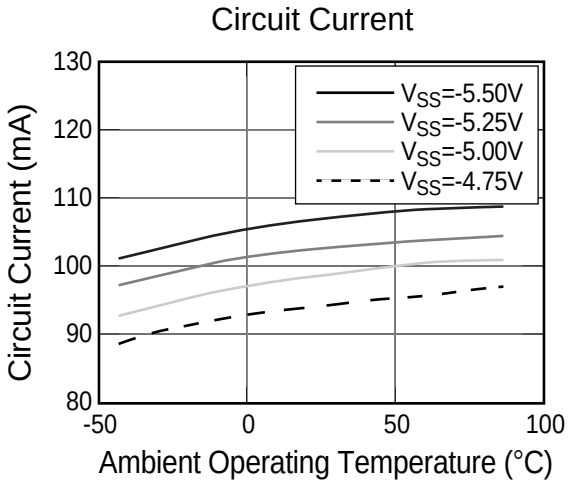

Conditions

$V_{OUT}@OUT_{BIAS}$=GND
$V_{DD}$= GND , $V_{SS}$= -5 V, $V_{IN}@D_{IN}$=-1.0 V
$V_{IN}@D_{INB}$=-1.3 V, $V_{MIN}=V_{SS}$
$V_{OUT}@OUT$, $OUT_B$ =GND

Conditions

$V_{OUT}@OUT_{BIAS}$ =-1.6 V
$V_{DD}$= GND, $V_{SS}$= -5 V, $V_{IN}@D_{IN}$=-1.0 V
$V_{IN}@D_{INB}$=-1.3 V, $V_{MIN}=V_{SS}$
$V_{OUT}@OUT$, $OUT_B$ =GND

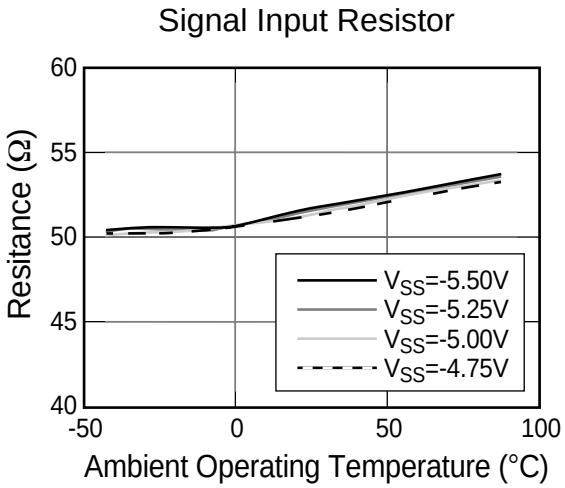
(3) Circuit Current




Conditions

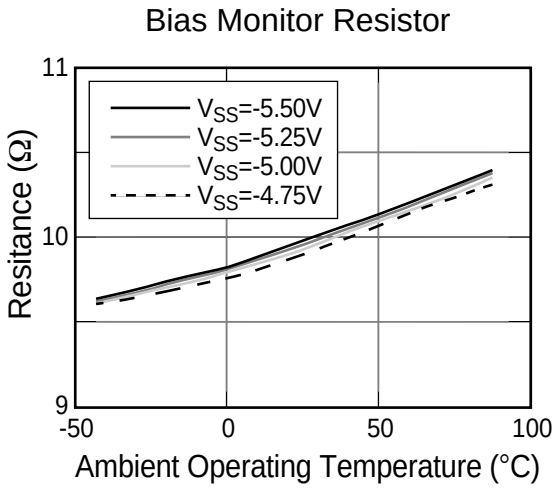
$V_{DD}$=GND, $V_{IN}$@$D_{IN}$=-1.0V
$V_{IN}$@$D_{INB}$=-1.3 V, $V_{MIN}$=$V_{SS}$ , $V_{BIN}$=$V_{SS}$
$V_{OUT}$@OUT, $OUT_B$ , $OUT_{BIAS}$ =GND

(4) Signal Input Resistor and Bias Monitor Resistor




Conditions

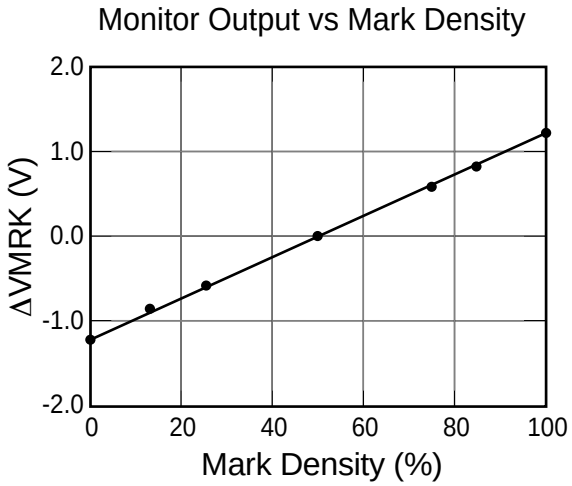
$V_{DD}$ =GND, $V_{SS}$= -5 V, $V_{IN}$@$D_{IN}$=-1.0 V
$V_{IN}$@$D_{INB}$=-1.3 V, $V_{MIN}$=$V_{SS}$ , $V_{BIN}$=$V_{SS}$
$V_{OUT}$@OUT, $OUT_B$ , $OUT_{BIAS}$ =GND




Conditions

$V_{DD}$ =GND, $V_{SS}$= -5 V, $V_{IN}$@$D_{IN}$=-1.0 V
$V_{IN}$@$D_{INB}$=-1.3V, $V_{MIN}$=$V_{SS}$ , $V_{BIN}$@$I_B$=60 mA
$V_{OUT}$@OUT, $OUT_B$ , $OUT_{BIAS}$ =GND

(5) Mark Density Monitor Voltage



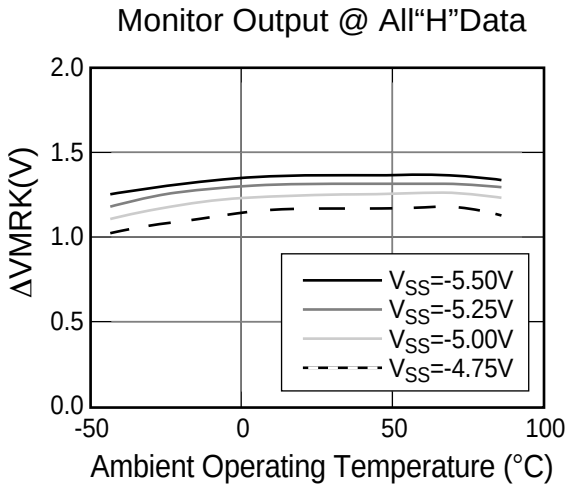

Conditions (See test circuits for AC characteristics)

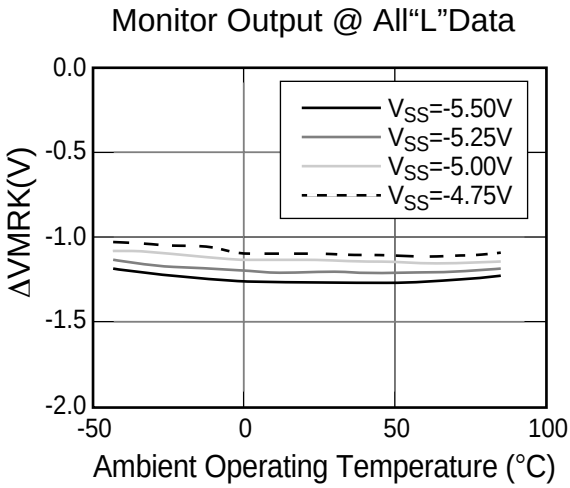
$V_{DD}$=GND, $V_{SS}$=-5 V, @2.48832 Gb/s, PRBS$2^{23}$-1

$V_{IN}$@$D_{IN}$ , $D_{INB}$ , $CK_{IN}$ , $CK_{INB}$=-0.9 V/-1.7 V

$V_{MIN}$@$I_{Mpeak}$=60 mA, $V_{BIN}$=$V_{SS}$

$V_{OUT}$@$OUT_{BIAS}$=GND, $T_a$=25 °C




Conditions

$V_{DD}$=GND, $V_{IN}$@$D_{IN}$=-1.0 V, $V_{IN}$@$D_{INB}$=-1.3 V

$V_{MIN}$@$I_{Mpeak}$=60 mA, $V_{BIN}$=$V_{SS}$

$V_{OUT}$@OUT, $OUT_B$ , $OUT_{BIAS}$=GND

Conditions

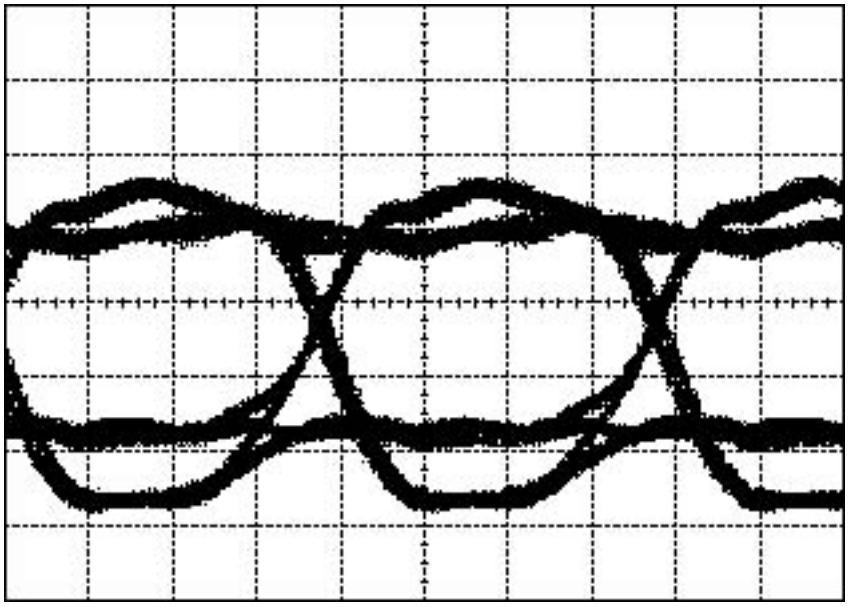
$V_{DD}$=GND, $V_{IN}$@$D_{IN}$=-1.6 V, $V_{IN}$@$D_{INB}$=-1.3 V

$V_{MIN}$@$I_{Mpeak}$=60 mA, $V_{BIN}$=$V_{SS}$

$V_{OUT}$@OUT, $OUT_B$ , $OUT_{BIAS}$=GND

(6)-(a) Erectrical Output Waveform @Clocked Operation

200 mV/div



100 ps/div

Conditions

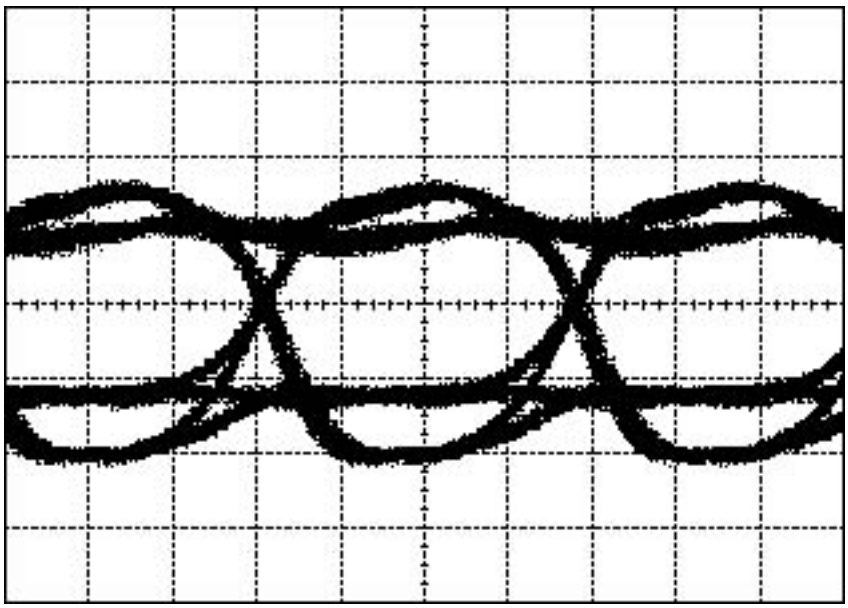
$T_a$=25 °C, $V_{DD}$=GND, $V_{SS}$=-5 V,

$D_{IN}$ :VIL=-1.7V,VIH=-0.9V,DINB=-1.3V,@2.5 Gb/s, PRBS$2^{23}$-1

CKIN:VIL=-1.7V,VIH=-0.9V.CKINB=-1.3V,f=2.5GHz

VM=-3.9V,VB=-5.0V,RL=15 ohms

200 mV/div



100 ps/div

Conditions

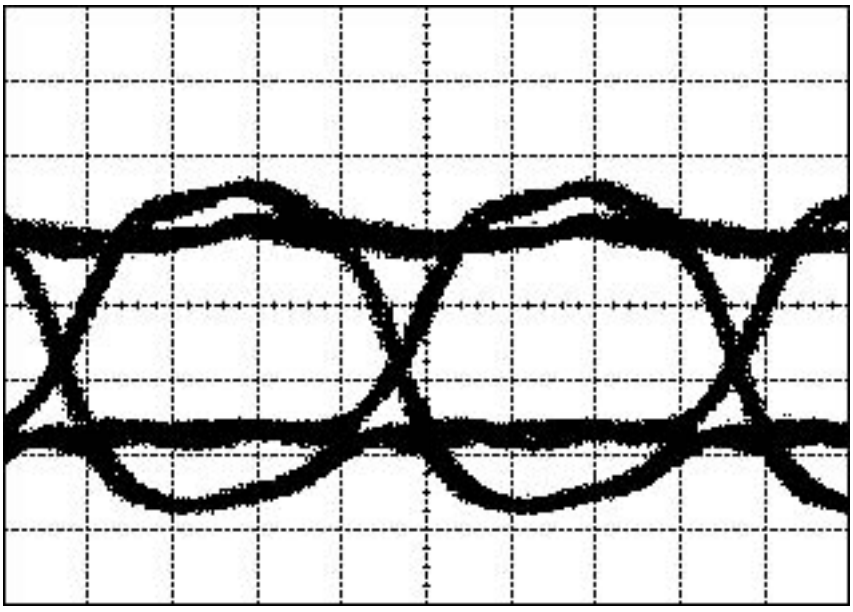
$T_a$=25 °C, $V_{DD}$=GND, $V_{SS}$=-5 V,

$D_{IN}$ :VIL=-1.7V,VIH=-0.9V,DINB=-1.3V,@2.5 Gb/s, PRBS$2^{23}$-1

CKIN:VIL=-1.7V,VIH=-0.9V.CKINB=-1.3V,f=2.7GHz

VM=-3.9V,VB=-5.0V,RL=15 ohms

(6)-(b) Erectrical Output Waveform @non-Clocked Operation

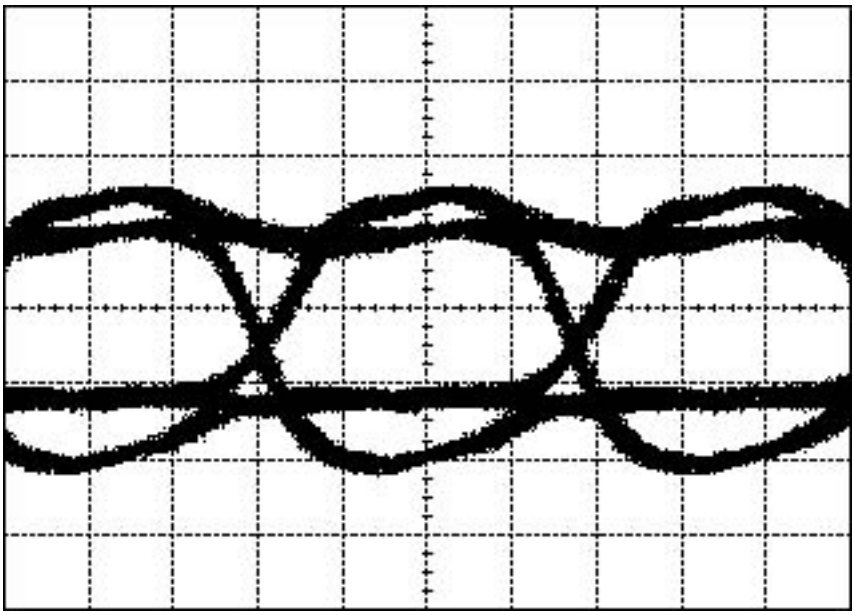


Conditions

$T_a$=25 °C, $V_{DD}$=GND, $V_{SS}$=-5 V,

$D_{IN}$ :VIL=-1.7V,VIH=-0.9V,DINB=-1.3V,@2.5 Gb/s, PRBS$2^{23}$-1

VM=-3.9V,VB=-5.0V,RL=15 ohms



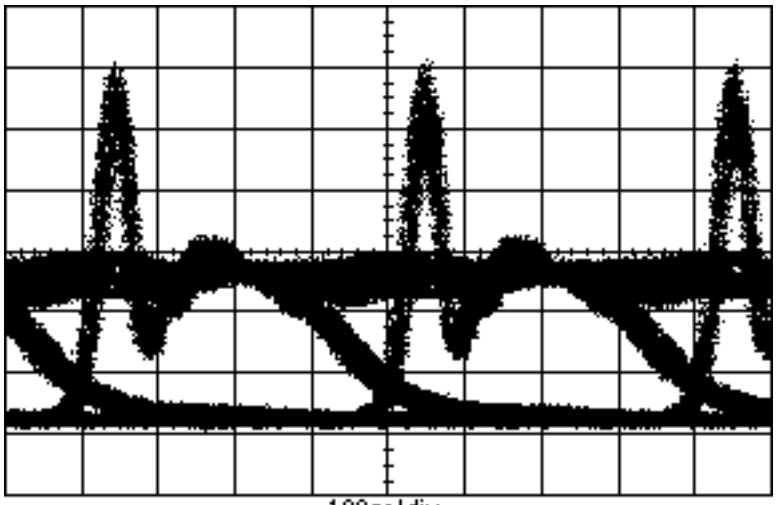
Conditions

$T_a$=25 °C, $V_{DD}$=GND, $V_{SS}$=-5 V,

$D_{IN}$ :VIL=-1.7V,VIH=-0.9V,DINB=-1.3V,@2.5 Gb/s, PRBS$2^{23}$-1

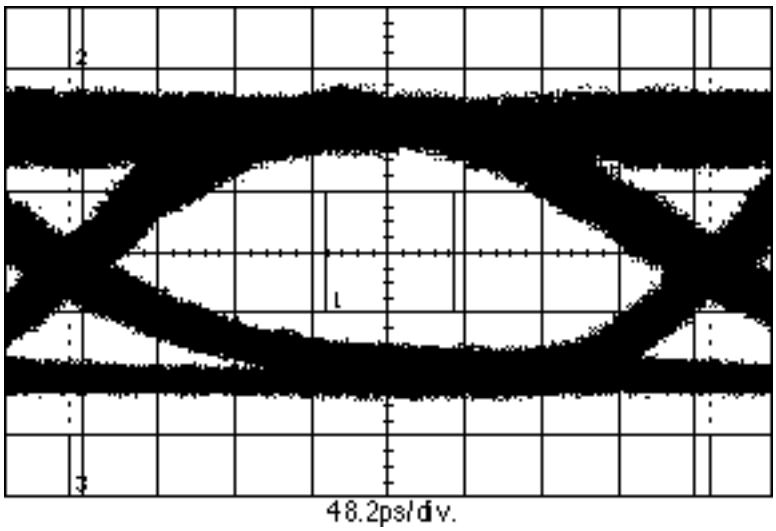
VM=-3.9V,VB=-5.0V,RL=15 ohms

(7)-(a) Optical Output Waveform @2.48832Gb/s (1310nm FP-LD)




Conditions

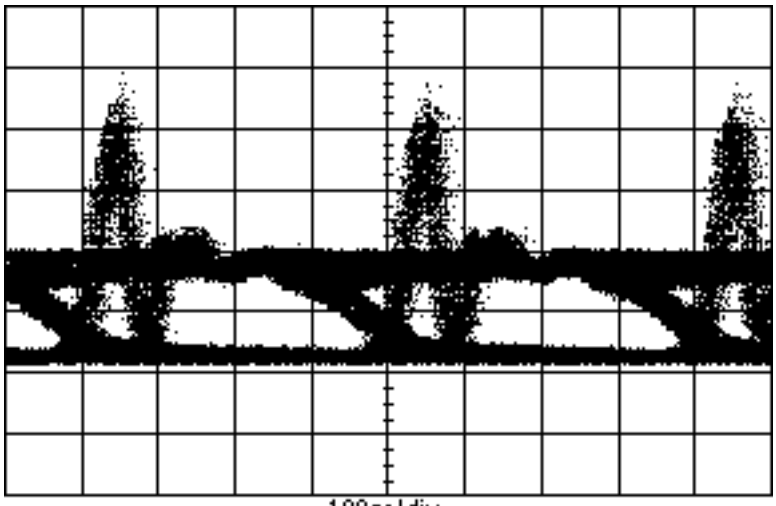
$T_a$=25 °C, $V_{DD}$=GND, $V_{SS}$=-5 V, @2.48832 Gb/s, PRBS$2^{23}$-1
$V_{IN}$@$D_{IN}$ , $D_{INB}$ , $CK_{IN}$ , $CK_{INB}$=0.8Vp-p (AC coupled)




Conditions

$T_a$=25 °C, $V_{DD}$=GND, $V_{SS}$=-5 V, @2.48832 Gb/s, PRBS$2^{23}$-1
$V_{IN}$@$D_{IN}$ , $D_{INB}$ , $CK_{IN}$ , $CK_{INB}$=0.8Vp-p (AC coupled)
with fourth order Bessel-Thompson filter

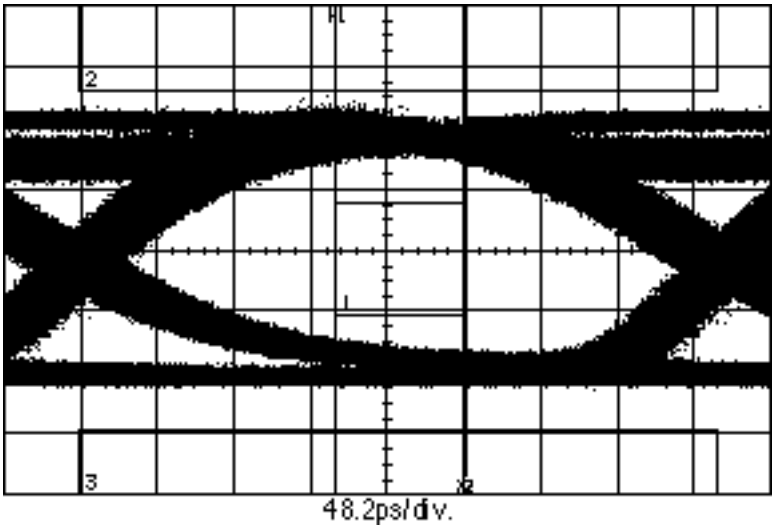
(7)-(b) Optical Output Waveform @2.48832Gb/s (1310nm DFB-LD)




Conditions

$T_a$=25 °C, $V_{DD}$=GND, $V_{SS}$=-5 V, @2.48832 Gb/s, PRBS$2^{23}$-1

$V_{IN}$@$D_{IN}$ , $D_{INB}$ , $CK_{IN}$ , $CK_{INB}$=0.8 Vp-p (AC coupled)



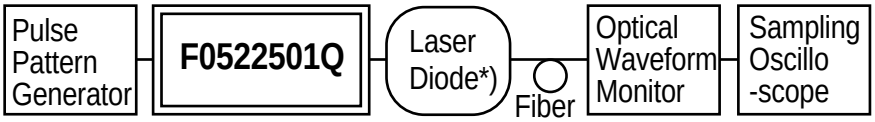

Conditions

$T_a$=25 °C, $V_{DD}$=GND, $V_{SS}$=-5 V, @2.48832 Gb/s, PRBS$2^{23}$-1

$V_{IN}$@$D_{IN}$ , $D_{INB}$ , $CK_{IN}$ , $CK_{INB}$=0.8 Vp-p (AC coupled)

with fourth order Bessel-Thompson filter

## ♦ *Test Circuit*

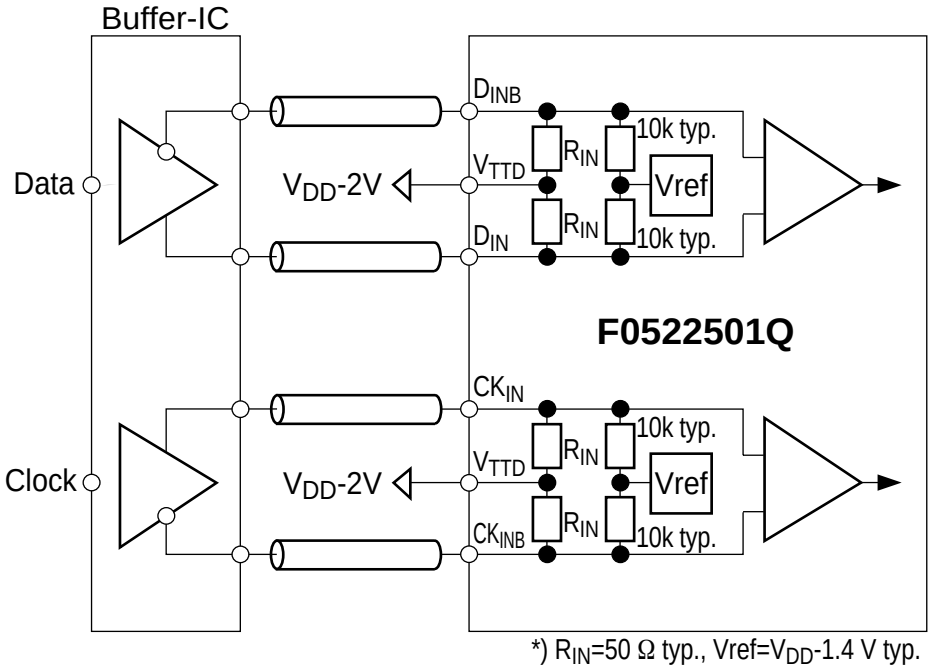



*) 1310nm DFB-LD:SLT4200Series (Sumitomo Electric Industries, LTD.)
1310nm FP-LD:SLT4100Series (Sumitomo Electric Industries, LTD.)

## ♦ *Application Guide*

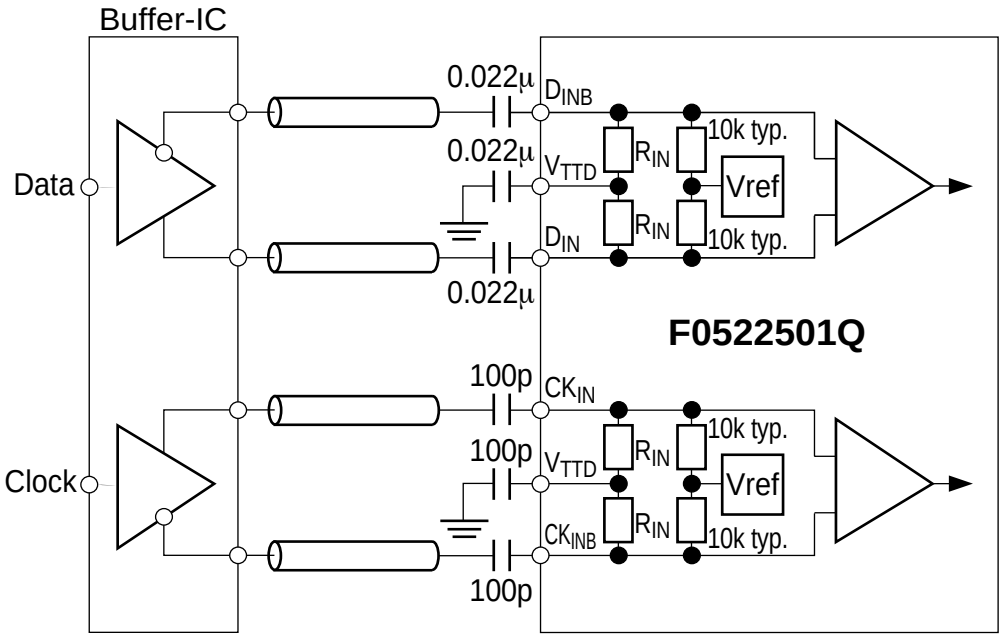
(1) Data and Clock Input Interface

(a) Differential ECL (or PECL) Interface



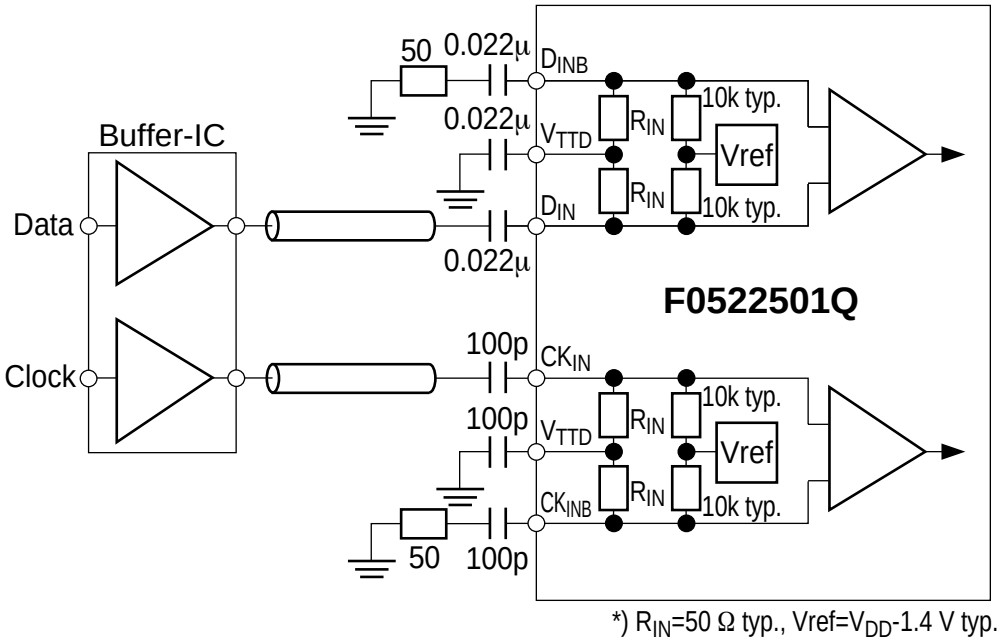

*) $R_{IN}$=50 Ω typ., Vref=$V_{DD}$-1.4 V typ.

(b) Differential AC Coupled Interface



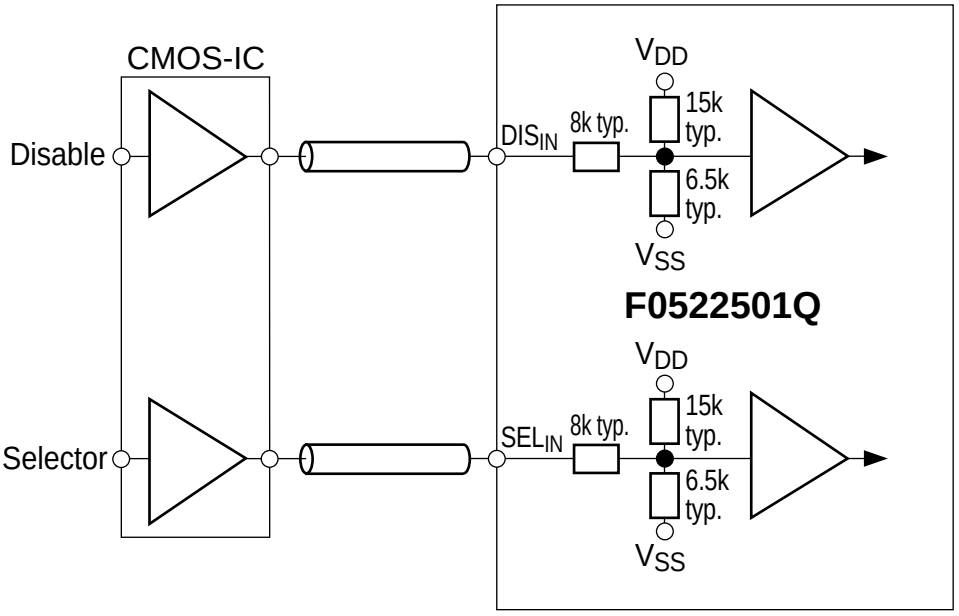

*) $R_{IN}$=50 Ω typ., Vref=$V_{DD}$-1.4 V typ.

(c) Single-Ended AC Coupled Interface

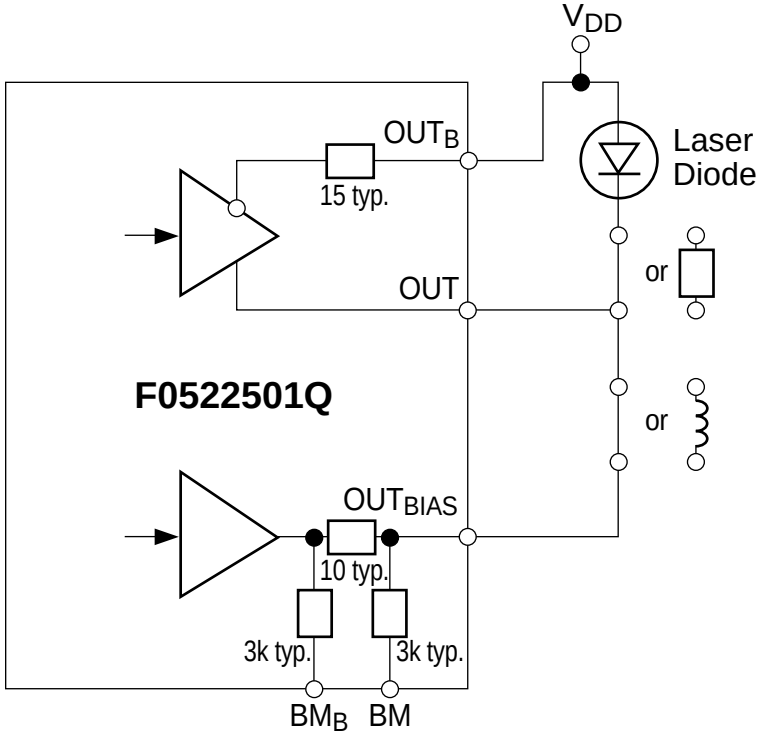



*) $R_{IN}$=50 Ω typ., Vref=$V_{DD}$-1.4 V typ.

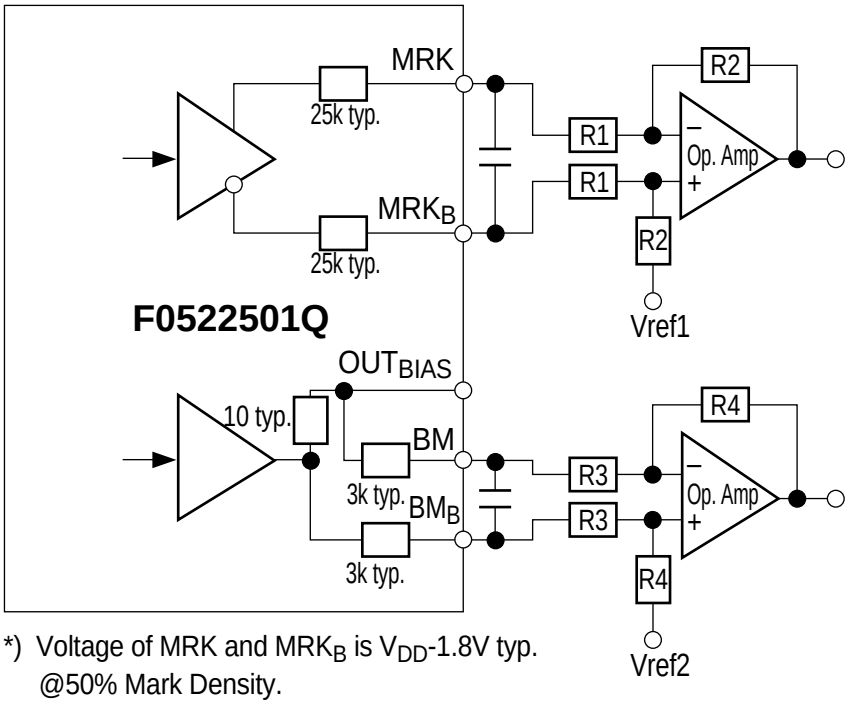
(2) Disable Input and Selector Input Interface




(3) Current Output Interface



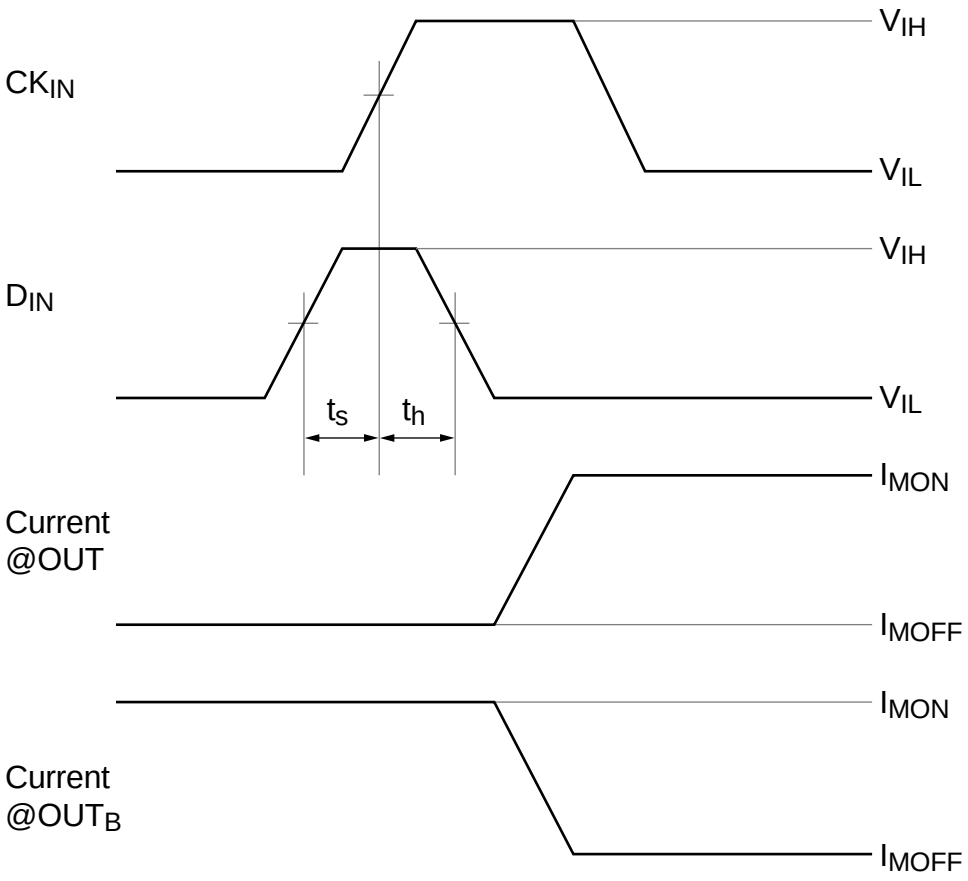
(4) Bias Current Monitor and Mark Density Monitor Interface



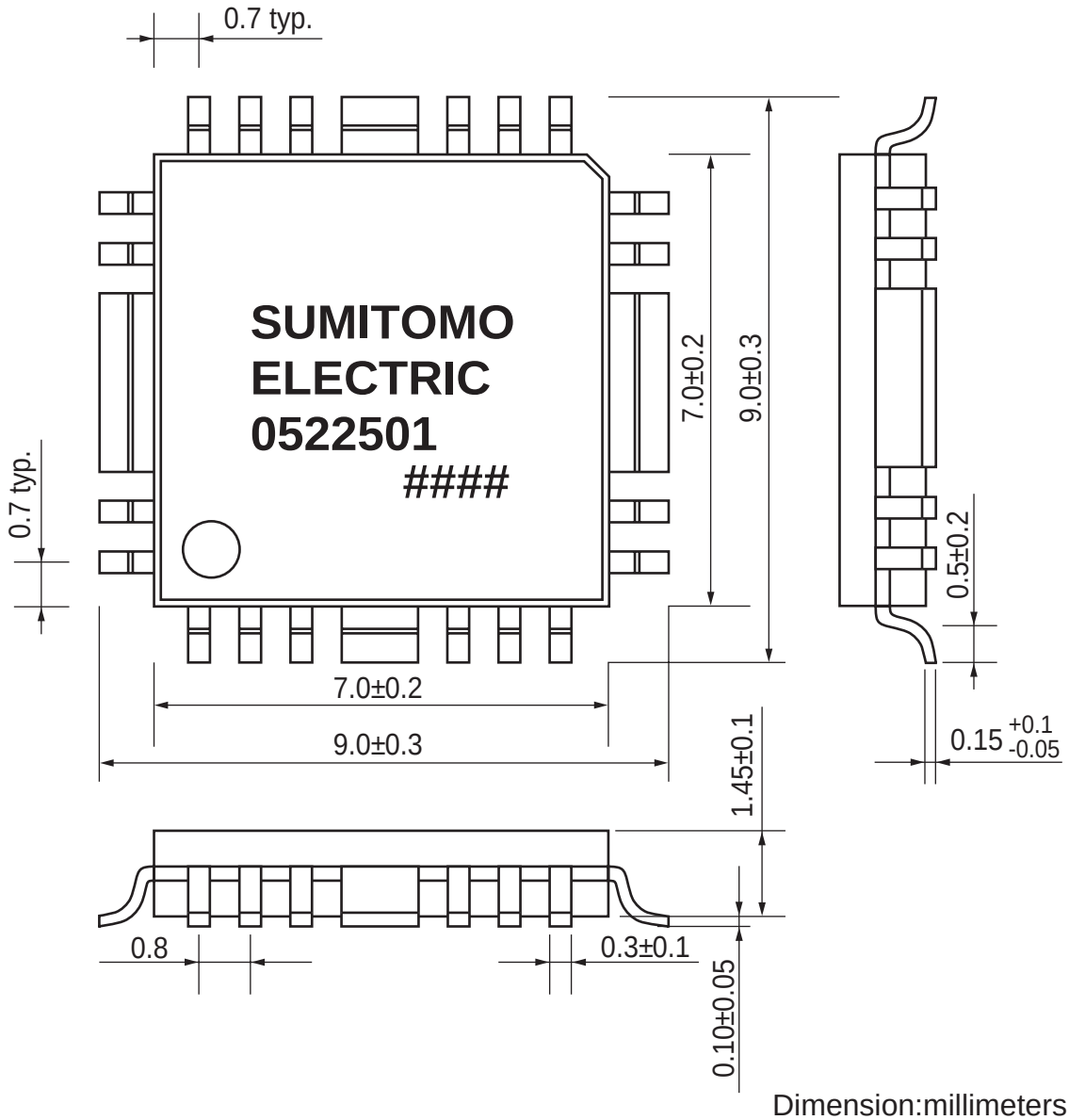

*) Voltage of MRK and MRK$_B$ is $V_{DD}$-1.8V typ.
@50% Mark Density.

**) Value of R1 to R4 should be enough larger than 25Ω.
Recommended value is 100k to 200kΩ.

(5) Timing Chart



## ♦ *Package Drawings*




Dimension:millimeters

## ♦ *APC (Auto Power Control) Sample Circuit*