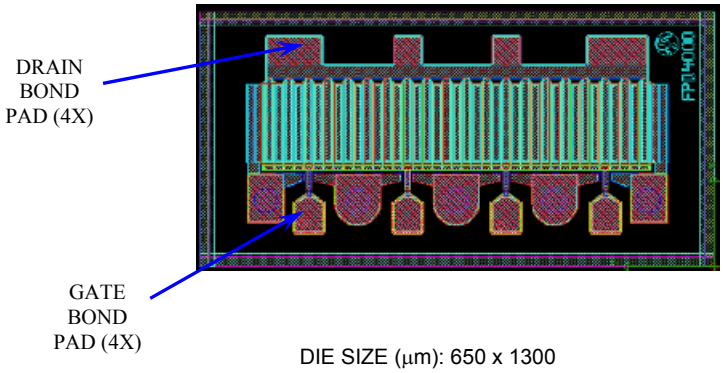
- **PERFORMANCE (1.8 GHz)**
  - ♦ 36.5 dBm Linear Output Power
  - ♦ 11 dB Power Gain
  - ♦ Useable Gain to 9 GHz
  - ♦ 47 dBm Output IP3
  - ♦ 19 dB Maximum Stable Gain
  - ♦ 45% Power-Added Efficiency
  - ♦ 10V Operation / Plated Source Thru-Vias



DIE SIZE (µm): 650 x 1300
DIE THICKNESS: 100 µm
BONDING PADS (µm): >70 x 65

- **DESCRIPTION AND APPLICATIONS**

The FPD4000V is a discrete depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT), optimized for power applications in L- and C-Bands. The FPD4000V includes Source plated thru-vias, and does not require wire bonds to the Source.

Typical applications include drivers or output stages in PCS/Cellular base station transmitter amplifiers, as well as other power applications in WLL/WLAN amplifiers.

- **ELECTRICAL SPECIFICATIONS AT 22°C**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
RF SPECIFICATIONS MEASURED AT f = 1.8 GHz USING CW SIGNAL						
Power at 1dB Gain Compression	P_{1dB}	V_{DS} = 10V; I_{DS} = 720 mA Γ_S and Γ_L tuned for Optimum IP3	35.5	36.5		dBm
Power Gain at dB Gain Compression	G_{1dB}	V_{DS} = 10V; I_{DS} = 720 mA Γ_S and Γ_L tuned for Optimum IP3	10.0	11.0		
Maximum Stable Gain S_{21}/S_{12}	MSG	V_{DS} = 10 V; I_{DS} = 720 mA P_{IN} = 0dBm, 50Ω system		19		dB
Power-Added Efficiency at 1dB Gain Compression	PAE	V_{DS} = 10V; I_{DS} = 750 mA Γ_S and Γ_L tuned for Optimum IP3		45		%
3rd-Order Intermodulation Distortion Γ_S and Γ_L tuned for Optimum IP3	IM3	V_{DS} = 10V; I_{DS} = 720 mA P_{OUT} = 25.5 dBm (single-tone level)		-46		dBc
Saturated Drain-Source Current	I_{DSS}	V_{DS} = 1.3 V; V_{GS} = 0 V	1.9	2.3	2.65	A
Maximum Drain-Source Current	I_{MAX}	V_{DS} = 1.3 V; V_{GS} ≅ +1 V		3.6		A
Transconductance	G_M	V_{DS} = 1.3 V; V_{GS} = 0 V		2.4		S
Gate-Source Leakage Current	I_{GSO}	V_{GS} = -3 V		70	170	µA
Pinch-Off Voltage	$\|V_P\|$	V_{DS} = 1.3 V; I_{DS} = 8 mA	0.7	0.9	1.4	V
Gate-Source Breakdown Voltage	$\|V_{BDGS}\|$	I_{GS} = 8 mA	6	8		V
Gate-Drain Breakdown Voltage	$\|V_{BDGD}\|$	I_{GD} = 8 mA	20	22		V
Thermal Resistivity	Θ_{CC}	See Note on following page		10		°C/W

- ## RECOMMENDED OPERATING BIAS CONDITIONS

  Drain-Source Voltage: From 5V to 10V

  Quiescent Current: From 25% I_{DSS} to 55% I_{DSS}

- ## ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	$-3V < V_{GS} < +0V$		12	V
Gate-Source Voltage	V_{GS}	$0V < V_{DS} < +8V$		-3	V
Drain-Source Current	I_{DS}	For $V_{DS} > 2V$		I_{DSS}	mA
Gate Current	I_G	Forward or reverse current		+25/-4	mA
RF Input Power[2]	P_{IN}	Under any acceptable bias state		1.5	W
Channel Operating Temperature	T_{CH}	Under any acceptable bias state		175	ºC
Storage Temperature	T_{STG}	Non-Operating Storage	-40	150	ºC
Total Power Dissipation	P_{TOT}	See De-Rating Note below		15.0	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits		80	%

[1] $T_{Ambient}$ = 22°C unless otherwise noted [2] Max. RF Input Limit must be further limited if input VSWR > 2.5:1
[3] Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings could result in permanent damage to the device.
- Thermal Resitivity specification assumes a Au/Sn eutectic die attach onto a Au-plated copper heatsink or rib.
- Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where
  P_{DC}: DC Bias Power
  P_{IN}: RF Input Power
  P_{OUT}: RF Output Power
- Absolute Maximum Power Dissipation to be de-rated as follows above 22°C:
  $P_{TOT} = 15.0W - (0.10W/°C) \times T_{HS}$
  where T_{HS} = heatsink or ambient temperature above 22°C

Example: For a 85°C heatsink temperature: $P_{TOT} = 15.0W - (0.10 \times (85 - 22)) = 8.7W$

- ## HANDLING PRECAUTIONS

  To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. This product has be tested to Class 1A (> 250V but < 500V) using JESD22 A114, Human Body Model, and to Class A, (< 200V) using JESD22 A115, Machine Model..

- ## ASSEMBLY INSTRUCTIONS

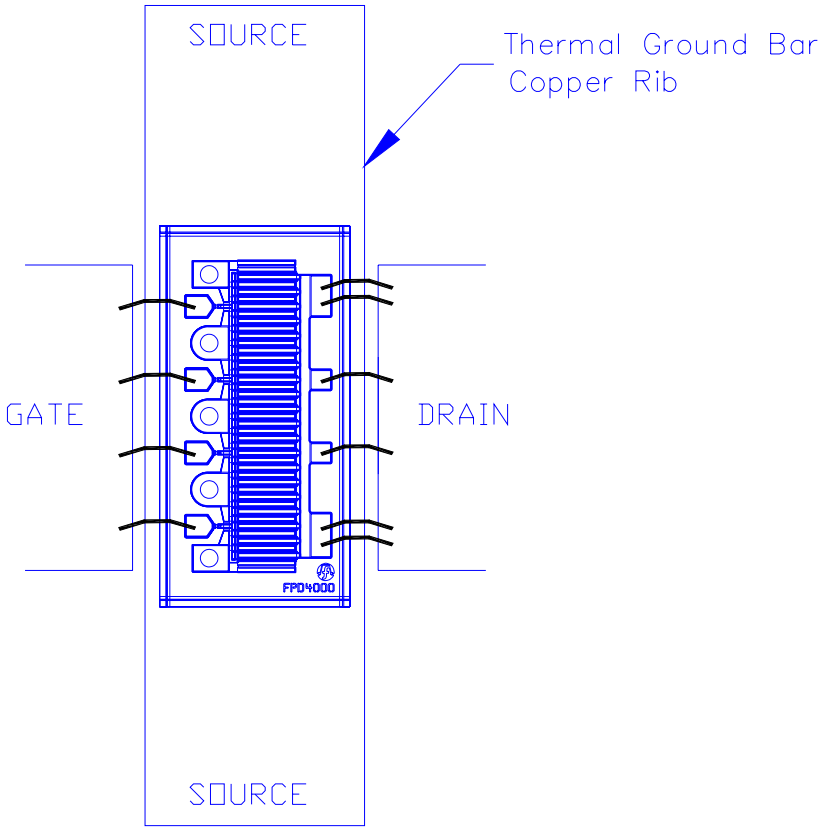
  The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be 280-290°C; maximum time at temperature is one minute. The recommended wire bond method is thermo-compression wedge bonding with 1.0 mil (0.025 mm) gold wire. Stage temperature should be 250-260°C.

- APPLICATIONS NOTES & DESIGN DATA

  Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site.

- BONDING DIAGRAM

  Note: 25 µm (0.001 in.) gold wire is recommended. No Source wire bonds are needed, device features Source thru-vias.



All information and specifications are subject to change without notice.