GDC21D401B
(Video Decoder)

Version 1.0

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HYUNDAI
MicroElectronics

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1. General Description

The Video Decoder(VD) decodes video elementary stream of MPEG-2(ISO/ICE 13818-2)MP@HL. It supports the ATSC digital TV video standard, and can be used for the video part of the ATSC digital TV with the Transport Decoder and the VDP(Video Display Processor). Picture decoding timing can be controlled internally for A/V lip synchronization, and externally for Video Trick Mode by host microprocessor via I^{2}C bus. The Video Decoder can extract video user data including caption from video elementary stream, and host microprocessor can read the video user data from the Video Decoder(VD) via I^{2}C. It uses four 16x1M SDRAMs and can support up to 81 MHz memory clock speed.

2. Features

• Supports MPEG-2 (ISO/ICE 13818-2) MP@HL

• Supports all video input formats of ATSC digital TV standard

• Supports picture decoding capability up to 1920x1088 30 Frame/Sec

• Supports all kinds of motion compensation methods of MPEG-2

• Supports MPEG-2 error code, syntax error detection, and slice-based error concealment

• Supports DTS synchronization

• Supports VBV delay mode and low delay mode decoding

• Supports film mode decoding (3:2 Pull down)

• Supports high level commands for trick mode

• Supports 8(w)x64(d) internal user data FIFO

• Outputs: macroblock format

    4-pel parallel output
    54 MHz synchronous I/F
    Data window (pdwin, sclk, and mbclk)
    Picture information (Picture structure, Field parity, and DCT type)

• External memory for VBV buffer , DTS FIFO and 2-frame memory:

    64-bit Data Bus
    81 MHz Synchronous Interface
    64-Mbyte
    Four 16x1M SDRAMs

• Host processor interface: I^{2}C bus interface

    Two interrupt signals
    Supports 23 programmable internal registers

3. Pin Description

Figure 1. Pin Description

(Package: 240 HQFP)

NAME	PIN	TYPE	DESCRIPTION
CLOCK			
VDCLK	165	I	**Operating clock**. - 54 MHz (max), 50 % duty cycle
MCLK	94	I	**SDRAM interface clock**. - 81 MHz (max), 50 % duty cycle
MCLK_IN	234	I	**SDRAM interface clock**. - 81 MHz (max), 50 % duty cycle (the same clock as MCLK)
MCLK_OUT	237	O	SDRAM interface clock through clock buffer for delay effect. This signal input is **MCLK_IN**.
CLK_27M	6	I	**External system time clock**. - 27 MHz
RESET			
\RESET	8	I	Power on reset(active low). At least 3 VDCLKs. Decoding starts after 128 VDCLKs from the last reset low state.
I^{2}C-BUS INTERFACE			
SCL	26	I	**I^{2}C-bus serial clock**. - 400 KHz(max)
SDA	28	I/O	**I^{2}C-bus serial data**
TRANSPORT INTERFACE			
VID_DATA[7:0]	25,23,21,20, 18,16,15,14	I	**Transport Decoder data bus**
\VID_REQ	29	O	**Transport data request**(active low)
VID_STRB	13	I	**Transport data strobe.** **VID_DATA**[7:0] is latched on the rising edge.
TSW	9	I	**PTS & DTS data enable**(active high). In LG DTV chipset, this signal is connected to the **PTS_DTS_STRB** pin of GDC21D301A.
\VIDEN	10	I	**Video bitstream data enable**(active low)
VSTCW	11	I	**STC data enable**(active high)
HOST INTERRUPT			
\INT_V	31	O	**Video decoder interrupt**(active low)
\UBUFF_FULL	30	O	**User data FIFO is full**(active low). When it happens, host microprocessor must read the user data from user data FIFO. Otherwise video decoder suspends decoding.
SDRAM INTERFACE			
CSN	109	O	**SDRAM chip selection**(active low)
WEN	106	O	**SDRAM write enable**(active low)
RASN	108	O	**SDRAM row address selection**(active low)
CASN	107	O	**SDRAM column address selection**(active low)
BA0	104	O	**SDRAM bank address**. This indicates bank address, and low value selects bank '0'.
SDRAM_ADDR [10:0]	103,102,101, 99,92,89,86, 84,87,91,98	O	**SDRAM address**
SDRAM_DATA [63:0]	163,162,161, 158,157,154, 152,150,43, 42,40,39,38, 36, 34, 33	I/O	**SDRAM data bus**

Pin Description (*continued*)

NAME	PIN	TYPE	DESCRIPTION
VDP INTERFACE - SYNC & PICTURE FORMAT			
DIS_INFO	174	O	**Serialized picture format data**
D_INFO_WIN	175	O	**Serialized picture format data enable**(active high)
PIC_DIS_SYNC	230	I	**Picture display sync**. - 30 Hz or 29.97 Hz, 50% duty
VDP INTERFACE – PICTURE DATA			
P_WAIT	231	I	**PDATA wait**(active high). This signal makes PDATA output to be suspended after 50 VDCLKs from the last high value. This signal is the output of the VDP.
PDWIN	177	O	**Picture data window**(active high). During 1 picture data decoding, this signal is high.
PSTR[1:0]	179,178	O	**Picture structure**. This indicates the structure of output picture. If this is equal to '1', the output picture is top field picture. If this is equal to '2', the output picture is bottom field picture. If this is equal to '3', the output picture is frame picture.
\FFPN	171	O	**First field parity**(active low). This signal is the first_field_parity flag of output picture. When output picture is interlaced frame picture, the field of output frame is the first output by the VDP.
SCLK	166	O	**Slice decoding window**(active high). This signal has high value when a macroblock with the same vertical position is decoded. There are at least 2-clock low value periods between each slice decoding window.
MBCLK	168	O	**Macroblock decoding window**(active high). This signal has high value when a macroblock data is decoded. The width of high value is always 96 VDCLKs. There are at least 2-clock low value periods between each macroblock decoding window.
DEC_ERROR	233	O	**Decoding Error** (active high) This is a multiplexed output signal. It is used to inform VDP R1.2 (GDC21D701B) of an error in Picture or Macro Block.
FP_FD	235	O	**Frame_Pred_Frame_Dct** (active high) **This signal is explained in ISO/IEC 13818-2 (Information technology – Generic coding of moving pictures and associated audio information : Video)** If this flag is set to '1', only frame_DCT and frame prediction are used. In a field picture, it should be '0'. If progressive_frame is '1', Frame_pred_frame_dct should be set to '1'. This flag affects the syntax of the bitstream.

Pin Description (*continued*)

| NAME	PIN	TYPE	DESCRIPTION
MBFI	169	O	**Macroblock Field IDCT**. This signal has the meaning when a decoded picture is a frame picture. If this is set to '0', the output of a decoded macroblock has the form of frame IDCT. If this is set to '1', the output of a decoded macroblock has the form of field IDCT.
PDATA[31:0]	227,226,225, 224,221,220, 191,190,187, 184,183,182	O	**Picture data**. This is a bundle of four adjacent pixel data. A decoded macroblock consists of 96 consequent PDATA. The order of PDATA in a decoded macroblock depends on the MBFI signal.

4. Block Diagram
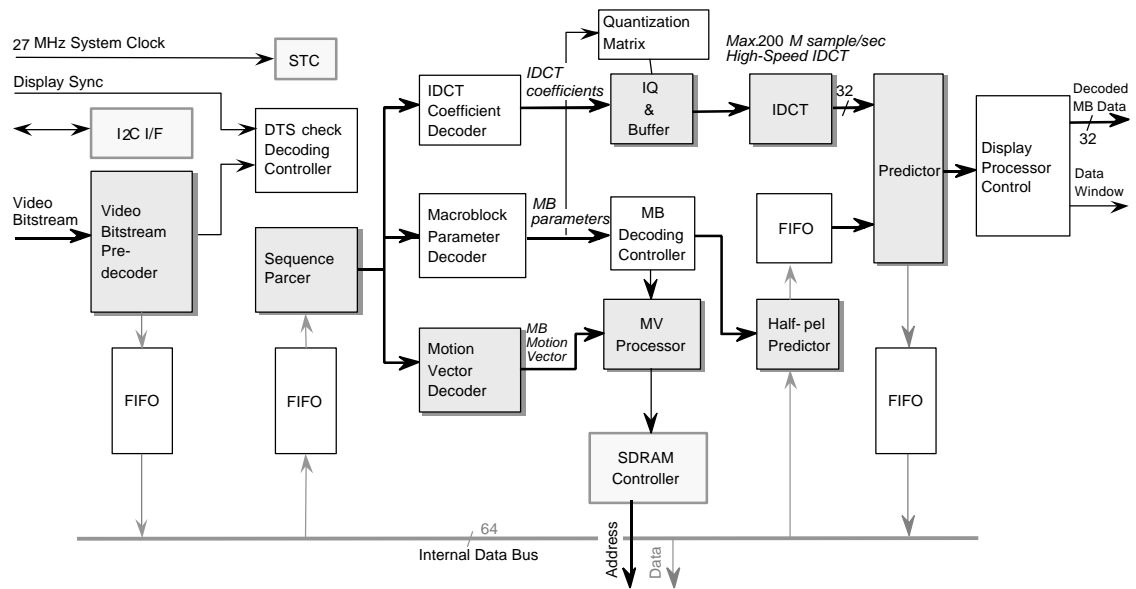
Figure 2. MPEG-2 MP@HL Video Decoder Block Diagram

5. Functional Description

5.1 Initialization and Decoding Start

¥ ₰ Power on reset: \RESET = '0' during several clocks. In this state, bitstream buffers are flushed, all decoding controllers are reset, and all internal registers have default values.

¥ ₵ Decoding start: \RESET = '1'. In this state, the bitstream buffers begin to be filled with input video bitstreams. First, the bitstream is discarded until the 1st sequence header code appears, and then the sequence headers are decoded. Next, the picture data bitstream is decoded, and it continues to be decoded unless the buffers are underflow.

5.2 Picture Decoding

Picture decoding control state diagram is shown in Fig 3. Each picture decoding is synchronized with the external 'pic_dis_sync' signal. If 'pic_dis_sync' signal is changed, command is executed, then some decoding conditions are checked (sync parity: top or bottom, underflow, DTS check and skip check). If the condition is "repeat", decoding is suspended until this condition is ended. If the condition is "skip", one picture frame data is skipped. Or else decoding sync is generated, and controller is suspended for given 'pic_dis_sync' duration which is determined by picture format information. If picture decoding is completed within the given 'pic_dis_sync' duration, the state is changed to wait sync state, and next decoding cycle is executed. If picture decoding is not completed within the given duration, the state is changed to task overrun state. In the task overrun state, as soon as picture decoding is completed, next decoding cycle is executed without waiting 'pic_dis_sync' transition.
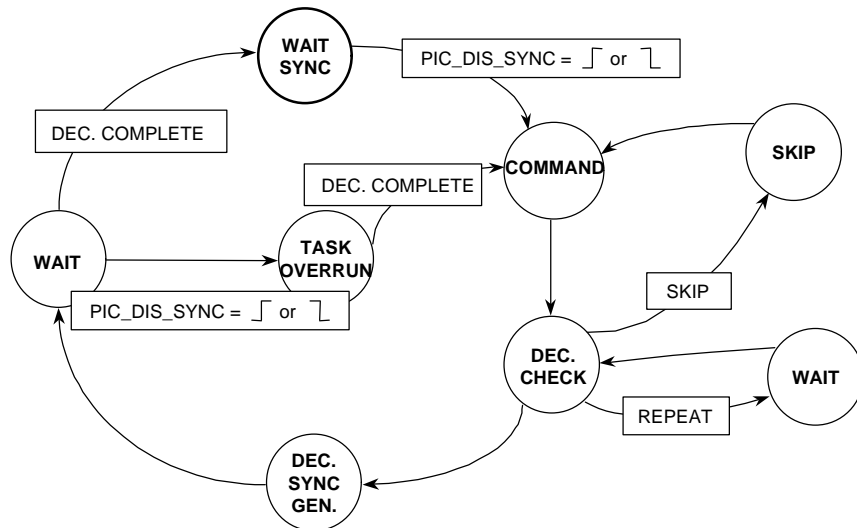

Figure 3. Picture Decoding Control State Diagram

5.3 STC (System Time Clock) Generation

Internal STC counter is supported. STC value should be loaded after the reset by host microprocessor or transport decoder, and be counted at 90 KHz clock derived from external 27 MHz system clock. Also it should be loaded whenever the system time base is changed. 27 MHz system clock is supplied by transport decoder through external 27 MHz clock input.

5.4 DTS (Decoding Time Stamp) Synchronization

The DTS values are determined when the associated pictures are decoded referring to the STC. The transport decoder must extract PTS & DTS values from MPEG-2 system layer, and transfer them to the VD through host interface or transport data interface. DTS values are extracted and stored in DTS-FIFO with 8-bit associated picture numbers(they are defined by the VD internally).

Before each picture decoding, picture decoding controller checks if there is a DTS associated with each picture. And it compares the DTS value from DTS-FIFO with STC value.
The DTS value is considered to match the current STC value if the DTS satisfies this equation:

$$STC + jitter\_b(negative) < DTS < STC + jitter\_f(positive)$$

In the case that jitter is the tolerance for the comparison:
If the DTS is less than $STC + jitter\_b$ (in other words, the time for current picture decoding has already passed), picture decoding controller discards B picture in VBV delay mode and any picture in low delay mode without decoding it.
If the DTS is greater than $STC + jitter\_f$ (the time for current picture decoding has not come yet), picture decoding controller pauses decoding process until the DTS value falls within the allowed tolerance of STC.

When system time base is changed, the time base of the current DTS can differ from that of the new STC temporarily because of video decoding delay. In this case, for about 0.5 sec, DTS synchronization mode must be disabled by using decoding mode register.

5.5 Error Concealment

When the VLD detects a bitstream syntax error or an MPEG-2 error code (0x000001B4), it performs appropriate error handling and error concealment to continue the decoding and to minimize the effect of the error on decoded video. If an error occurs at picture data layer, the slice-based error concealment is performed. If an error occurs at header layer, the associated sequence is skipped.

5.6 User Data Read

User data in MPEG Video Sequence can be read through host interface(I^2C) as follows. If user data interrupt is enabled, user data is stored in internal user data FIFO, and once 'PIC_DEC_SYNC' is set to 'high', a interrupt signal is generated which informs host that user data is stored in user data FIFO. If user data interrupt is disabled, user data is discarded.

When user data interrupt signal is generated, host reads the '**U_D_COUNT**' register for bytes of user data FIFO. And then it reads the '**USER_DATA**' register(user data FIFO output) repeatedly as many as the number of '**U_D_COUNT**' register. In this case, the host had better use I^2C burst read cycle for reading speed efficiency.

If internal user data FIFO becomes full during user data interrupts, '**UBUFF_FULL**' signal is generated. And also the host reads user data by using the same method as that of user data interrupt.

5.7 Bitstream Buffer Over/Underflow

The bitsream buffer should not be overflowed or underflowed in proper operation. When bitstream buffer is overflowed, video bitstream input is disabled during overflow. At the beginning of each picture, buffer underflow is checked. If the bitstream buffer doesn't include 1 picture bitstream, decoding is paused until this buffer is filled with 1 picture bitstream.

5.8 VLD (Variable Length Decoder)

The VLD executes the variable length decoding of MPEG-2 MP@HL. It is composed of sequence syntax parsing and code decoding. Headers, IDCT coefficients, and motion vectors are generated from input video bitstream by the VLD.

5.9 Inverse Quantization

For decoding a macroblock, various parameters are transmitted to IQ block and MC block in sequence of decoding syntax from the VLD. Coefficient data transmitted to IQ block is multiplied by quantization matrix and quantization scale. Quantized coefficients are stored in two coefficient buffers, and if a request from MC block occurs, the buffer outputs 4 coefficients in parallel. Inverse scan processing is performed in the coefficient buffer by varying read/write address according to scan type.

5.10 IDCT (Inverse Discrete Cosine Transform)

Coefficient data from IQ block is transmitted to IDCT block. IDCT block transforms these coefficients to pixel data or differential pixel data which have the values in the range of -256 to 255. For one 8x8 DCT block, the elapse time through IDCT block is a 30-VDCLK period. In the IDCT block, 8 adjacent coefficients are processed in parallel. The maximum transform speed of the IDCT block is 1 VDCLK x 4 Sample/sec. This speed is sufficient for decoding 1920x1088 30Hz frame data.

5.11 MC(Motion Compensation)

Motion Compensation Block restores macroblocks by using macroblock difference data from IDCT block and reference data which are read from external SDRAM. Address Generation Block in the MC generates SDRAM address by transforming macroblock address and motion vector to row/column address of SDRAM. The MC block supports all motion types of frames and field pictures. Motion vector range decoded in the MC has the range of f_code=9 for horizontal motion vector and f_code=8 for vertical motion vector. Reconstructed macroblock in the MC block is stored in the external frame memory for I or P picture, but in the case of B picture, decoded macroblock is transmitted directly to the VDP without being stored in the frame memory. Because reordering occurs in I or P picture decoding, macroblock data to be displayed is read from reference frame memory and is transmitted to the VDP in the form of macroblock.

5.12 Transport Interface

8-bit parallel data(**vid_data[7:0]**) interface is supported for transport data interface. Three kinds of data (Video bitstream, STC, and DTS) can be transferred through transport data interface.

If **vid_en** is low, video bitstream is transferred. If **vstcw** is high, STC is transferred. If **tsw** is high, PTS & DTS are transferred. Or else no data is transferred.

Vid_data[7:0] is latched on the rising edge of **vid_strb**. When **VID_REQ** is high, transport data interface is disabled, and when **VID_REQ** is low, transport data interface is enabled. See the following Fig. 4.
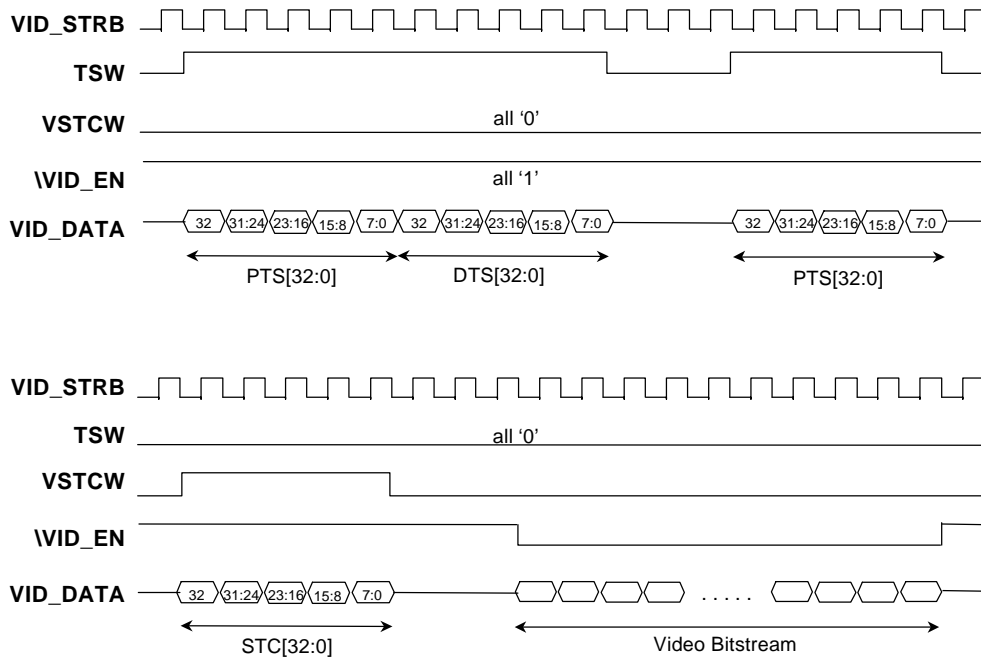
Figure 4. Transport Data Interface Timing Diagram

5.13 Host Interface

I²C bus interface

I²C bus interface is used for host data interface. It operates only as a Slave. The Chip-ID(dev address) of this IC is "0001111"b. Data on the I²C-bus can be transferred at the rate up to 100 kbit/s in the standard mode, or up to 400 kbit/s in the fast mode. I²C bus data read/write formats of this IC are shown in the Fig 5, 6, and 7. Burst Read Cycle can be used for the user data reading. For more information, see the I²C bus interface standard.

```
START           WRITE                      START        WRITE              PAUSE
     CHIP ID          ACK        ACK            CHIP ID       ACK      ACK
+---+----------+---+---+--------------+---+---+----------+---+---+--------------+---+---+
| S | 0001111  | 0 | 0 | REG. ADDR.(7:0) | 0 | S | 0001111  | 0 | 0 | REG. DATA(7:0) | 0 | P |
+---+----------+---+---+--------------+---+---+----------+---+---+--------------+---+---+
```

Figure 5. Write Cycle Diagram

```
START           WRITE                      START        READ               PAUSE
     CHIP ID          ACK        ACK            CHIP ID       ACK      ACK
+---+----------+---+---+--------------+---+---+----------+---+---+--------------+---+---+
| S | 0001111  | 0 | 0 | REG. ADDR.(7:0) | 0 | S | 0001111  | 1 | 0 | REG. DATA(7:0) | 1 | P |
+---+----------+---+---+--------------+---+---+----------+---+---+--------------+---+---+
```

Figure 6. Read Cycle Diagram

```
START              WRITE                       START          READ
      CHIP ID            ACK          ACK            CHIP ID         ACK          ACK
+---+----------+---+---+--------------+---+---+----------+---+---+--------------+---+
| S | 0001111  | 0 | 0 | REG. ADDR.(7:0) | 0 | S | 0001111  | 1 | 0 | REG. DATA(7:0) | 0 |
+---+----------+---+---+--------------+---+---+----------+---+---+--------------+---+

         +--------------+---+------------+--------------+---+---+
         | REG. DATA(7:0) | 0 |  . . . . . | REG. DATA(7:0) | 1 | P |
         +--------------+---+------------+--------------+---+---+
                          ACK                            ACK
                                                        PAUSE
```

Figure 7. Burst Read Cycle Diagram

Interrupt Mechanism

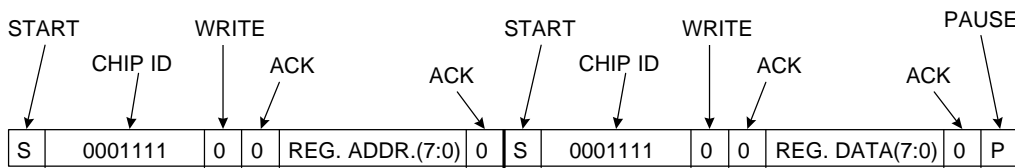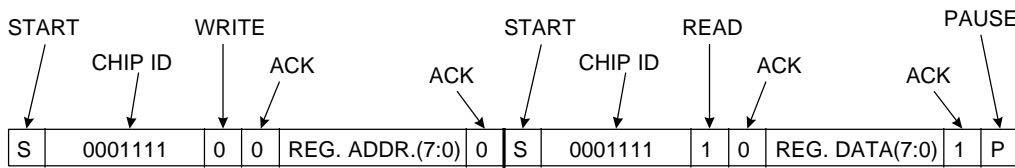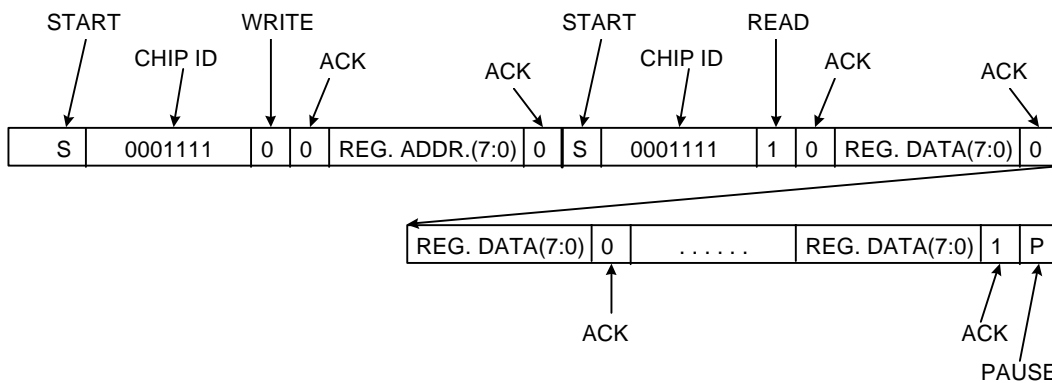The host enables specific interrupt events to occur by setting the mask value of internal interrupt. When an event occurs and corresponding interrupt enable is set, an interrupt bit is set in an interrupt register. Everytime each picture decodes sync, host checks the contents of that register, and if any bit is set, it generates an interrupt. Exceptionally, in the case of OVF, UND and ERR interrupt signals are generated as soon as the error is detected. When the host serves the interrupt, interrupt register and interrupt signal are reset.

Table 2. Bit Definitions for Interrupt Register & Mask

BIT #	MNEMONIC	EVENT	EVENT DEFINITION
0	PIC_S	Picture decoding	New picture is decoded.
1	GOP_H	GOP header decoding	GOP headers are decoded.
2	SEQ_H	Seq. header decoding	Sequence headers are decoded.
3	SEQ_E	Seq. end decoding	Sequence end code is decoded.
4	USR	User data ready	User data has been extracted and stored in the buffer. *When the interrupt is disabled, user data is discarded.*
5	OVF	Buffer overflow	Bitstream buffer is full.
6	UND/PTS	Buffer underflow/ PTS received	Dec_mode(4) = '0': Bitstream buffer doesn't have 1 picture bitstream. Dec_mode(4) = '1' PTS value is received through transport interface.
7	ERR	Bitstream error	Error code or syntax error is detected in the bitstream (header layer).

Register Description

Table 3. Internal Register Description

NO	NAME	SIZE	DESCRIPTION	DEFAULT	R/W
0	Command	3	High level decoding command.	play()	R/W
1	Interrupt	8	Interrupt register.	all '0'	R
2	DTS0	8	DTS[7:0]. When it is written by host microprocessor, DTS[19:0] values are stored in the DTS-FIFO. When DTS value is received through transport interface, it can be read via the DTS registers	all '0'	R/W
3	DTS1	8	DTS[15:8].	all '0'	R/W
4	DTS2	4	DTS[19:16].	all '0'	R/W
5	Jitter_f0	8	Forward tolerance of DTS synchronization, Jitter_f[7:0]. When it is written by host microprocessor, Jitter_f[19:16] values are applied.	h"10"	R/W
6	Jitter_f1	8	Jitter_f[15:8].	h"0E"	R/W
7	Jitter_f2	4	Jitter_f[19:16].	h"0"	R/W
8	Jitter_b0	8	Backward tolerance of DTS synchronization, Jitter_b[7:0]. When it is written by host microprocessor, Jitter_b[19:16] values are applied.	h"BA"	R/W
9	Jitter_b1	8	Jitter_b[15:8].	h"FA"	R/W
10	Jitter_b2	4	Jitter_b[19:16].	h"F"	R/W
11	Slm_num	6	Slow motion command of repeated numbers.	h'8'	R/W
12	Header	8	Header data register. It has header value indicated by H_addr.	all '0'	R
13	H_addr	8	Header data address.	all '0'	R/W
14	User_data	8	User data register. It is an output of the User data FIFO.	all '0'	R
15	U_d_count	7	User data count in the User data FIFO.	all '0'	R
16	Int_mask	8	Interrupt mask.	all '0'	R/W
17	Dec_mode	8	Decoding mode.	all '0'	R/W
18	STC0	8	System time clock, STC[7:0]. When it is written by host microprocessor, STC[19:0] values are loaded to internal STC counter.	all '0'	R/W
19	STC1	8	STC[15:8].	all '0'	R/W
20	STC2	4	STC[19:16].	all '0'	R/W
21	W_ptr	8	Write address pointer of the bitstream buffer. Unit value is 65,536 bits.	all '0'	R
22	R_ptr	8	Read address pointer of the bitstream buffer. Unit value is 65,536 bits.	all '0'	R
23	PTS0	8	PTS[7:0]. When PTS value is received through tranport interface, it is stored in the PTS registers.	all '0'	R
24	PTS1	8	PTS[15:8].	all '0'	R
25	PTS2	4	PTS[19:16].	all '0'	R

Table 4. Definitions of Command Register.

REG. VALUE	COMMAND	DESCRIPTION
0	Reset()	Bitstream buffer is flushed and decoding controllers are reset.
1	Play()	Start normal bitstream decoding.
2	Slow_motion()	Decode pictures and pause during **slm_num** duration, and repeat this process.
3	Scan()	Skip to I picture and continue decoding.
4	Single_step()	Decode 1 picture and pause.
5	Pause()	Decoding pause.
6	Fast_forward()	Decode only I or P picture.
7	NoCOM()	No command is loaded in the register. In this state bitstream buffer continues to be filled with input bitstreams.

Table 5. Definition of Header Address

H_ADDR	HEADER
0	H_size[7:0]
1	V_size[7:0]
2	'0' & h_size[10;8] & '0' & v_size[10:8]
3	Aspect_ratio[3:0] & frame_rate[3:0]
4	'0'&prog_seq&'0'&low_delay& pict_cod_type[1:0]& '0'&repeat_first_field
5	Matrix_coefficients[7:0]
6	VBV_delay[7:0]
7	VBV_delay[15:8]
8	Time_code[7:0]
9	Time_code[15:8]
10	Time_code[23:16]
11	"0000000"&Time_code[24]
12	Temporal_reference[7:0]
13	"000000"&Temporal reference[8:9]
14	Copyright_extension[7:0]
15	Copyright_extension[15:8]
16	Copyright_extension[23:16]
17	Copyright_extension[31:24]
18	Copyright_extension[39:32]
19	Copyright_extension[47:40]
20	Copyright_extension[55:48]
21	Copyright_extension[63:56]
22	Copyright_extension[71:64]
23	Copyright_extension[79:72]
24	"0000"&Copyright_extension[83:80]

Table 6. Definition of Decoding Mode Register

BIT #	DESCRIPTION
0	It must have "High".
1	DTS input timing: '0' => DTS values are transferred to VD before the associated PSTC. '1' => DTS values are transferred to VD after the associated PSTC. PSTC represents the Picture Start Code.
2	DTS synchronization: '0' => disabled '1' => enabled
3	Picture reordering in VBV delay mode: '0' => enabled '1' => disabled
4	Int_reg(6) & Int_mask(6) selection: '0' => UND '1' => PTS
5~7	"000" : Not used

5.14 Video Data Output Format

Video decoder transmits decoded macroblock data to the VDP via 32-bit bus. This bus consists of 4 adjacent pixel components. For a macroblock data, the number of 32-bit data is 96. The order of output data is the same of decoded block in the MPEG-2 Video bitstream syntax. For this reason, output sequence depends on the **DCT_TYPE** of decoded macroblock. Except for the macroblock whose parameter is Frame picture and Field DCT, all macroblock outputs have the sequence of below figure(MBFI=0) in Fig 8. The top field data of the macroblock whose **DCT_TYPE** is field type(MBFI=1) is transmitted before the macroblock bottom field data for the luminance data. But the chrominance data has always the same sequence.

0	1	16	17	64	65
2	3	18	19	66	67
4	5	20	21	68	69
6	7	22	23	70	71
8	9	24	25	72	73
10	11	26	27	74	75
12	13	28	29	76	77
14	15	30	31	78	79
32	33	48	49		
34	35	50	51	80	81
36	37	52	53	82	83
38	39	54	55	84	85
40	41	56	57	86	87
42	43	58	59	88	89
44	45	60	61	90	91
46	47	62	63	92	93
				94	95

MBFI == 0

0	1	16	17	64	65
32	33	48	49	66	67
2	3	18	19	68	69
34	35	50	51	70	71
4	5	20	21	72	73
36	37	52	53	74	75
6	7	22	23	76	77
38	39	54	55	78	79
8	9	24	25		
40	41	56	57	80	81
10	11	26	27	82	83
42	43	58	59	84	85
12	13	28	29	86	87
44	45	60	61	88	89
14	15	30	31	90	91
46	47	62	63	92	93
				94	95

MBFI == 1

Figure 8. The Sequence of Macroblock Output

5.15 Video Data Output Timing

During decoding the picture which is field picture or frame picture, PDWIN signal is high. Between each picture decoding time, there is low level period of PDWIN signal, and it is longer than 128 VDCLKs. Picture parameter such as PSTR[1:0] or \FFPN is determined 2 clocks before PDWIN

rising edge. Its value is not changed until PDWIN falling edge. SCLK shows that new slice decoding is started on its rising edge. Width of MBCLK high pulse is always 96 clocks, and low value period is longer than 2 clocks.
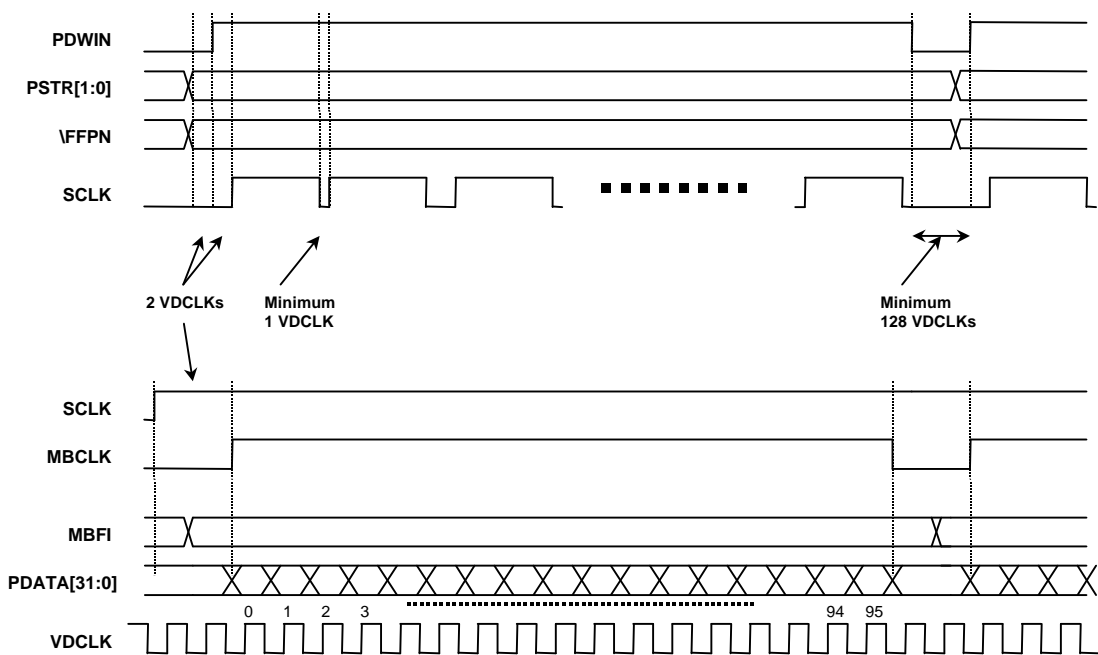
Figure 9. Timing Diagram

5.16 SDRAM Interface

For storing reference frame data and bitstream, very large external memory is required. For this reason, 64-Mbit external memory (GM72V161621AT or same type of memory) is needed. The memory configuration is shown in the following Fig 10. Four 16-Mbit memories are directly attached to the VD. Data bus for SDRAMs is configured to 64-bit bus. Memory interface clock should be supplied to the VD and four SDRAMs with same clock phase. Higher frequency for MCLK and higher decoding speed can be achieved. The maximum frequency of MCLK is 81 MHz. This clock doesn't need to be locked with any other input clock.

**Revision Note for SDRAM Clock Application Note(1):
Recommended**

Figure 10. External Memory Interface 1

Revision Note for SDRAM Clock Application Note(2)

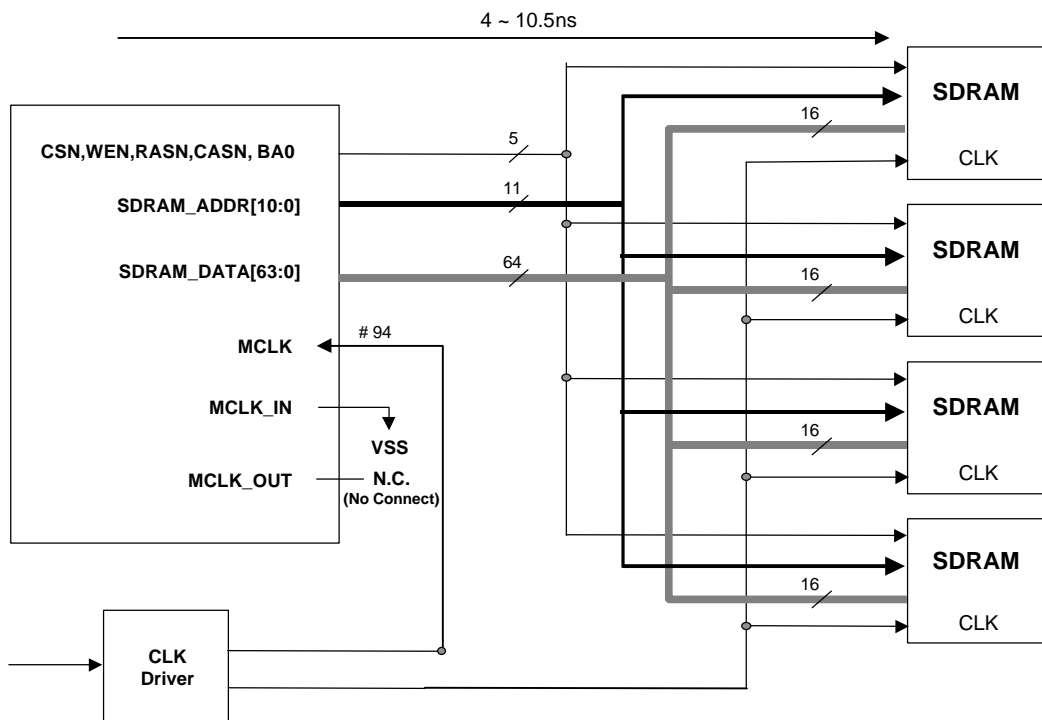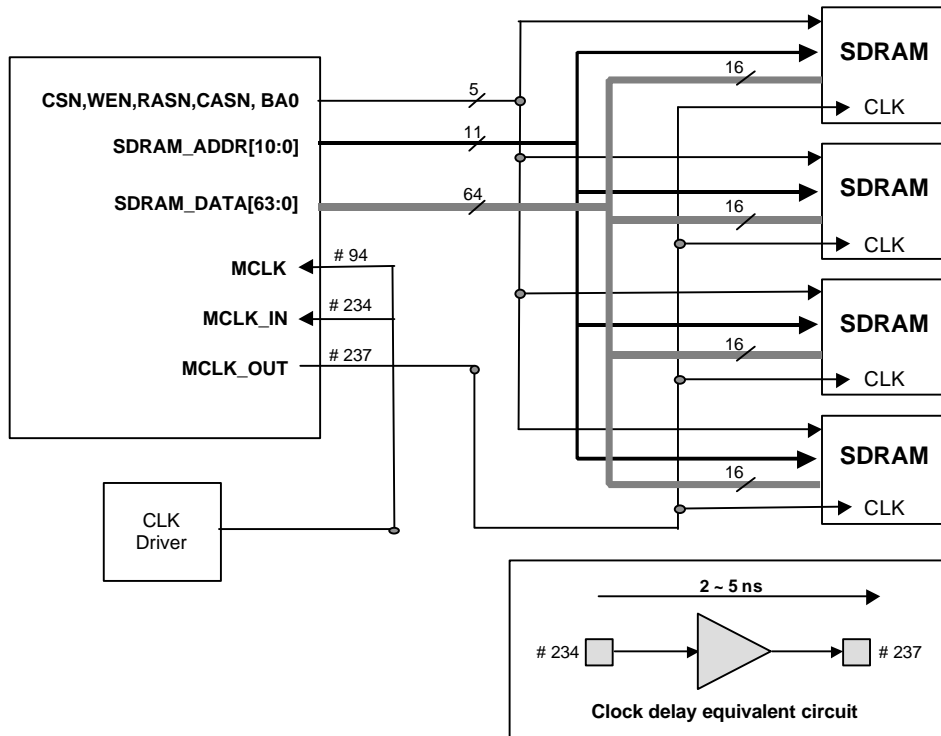**Figure 11. External Memory Interface 2**

6. Electrical Specification

6.1 Absolute Maximum Rating

SYMBOL	PARAMETERS	VALUES	UNIT
V_{DD}	Power Supply Voltage	-0.33 to 5.5	V
V_I	Digital Input Voltage	-0.33 to V_{DD} + 0.5	V
V_O	Digital Output Voltage	-0.33 to V_{DD} + 0.5	V
T_{stg}	Storage Temperature	-55 to 125	°C
P_d	Power Dissipation	4.6	W

*Note :Absolute Maximum Ratings mean that the safety of the device cannot be guaranteed beyond these values, and this doesn't imply that the device should be operated within these limits.

6.2 Recommended Operating Range

SYMBOL	PARAMETERS	VALUES	UNIT
V_{DD}	Power Supply Voltage	3.3 ± 10%	V
T_{opr}	Operating Temperature	0 to 70	°C

6.3 DC Characteristics (VDD = 3.3 V ¡¾ 10%, TA = 0 ~ 70 ¡É)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IH}	Input High Voltage	0.7X V_{DD}	V_{DD} +0.33	V
V_{IL}	Input Low Voltage	-0.33	0.2X V_{DD}	V
V_{OH}	Output High Voltage	2.4	V_{DD}	V
V_{OL}	Output Low Voltage	0	0.4	V
I_{DD}	Operating Current	-	900	mA
I_{DDQ}	Standby Current	-	10	uA
F_{OPR}	Operating Frequency	-	54	MHz

6.4 AC Characteristics (VDD = 3.3 V ¡ ¾0%, TA = 0 ~ 70¡É)
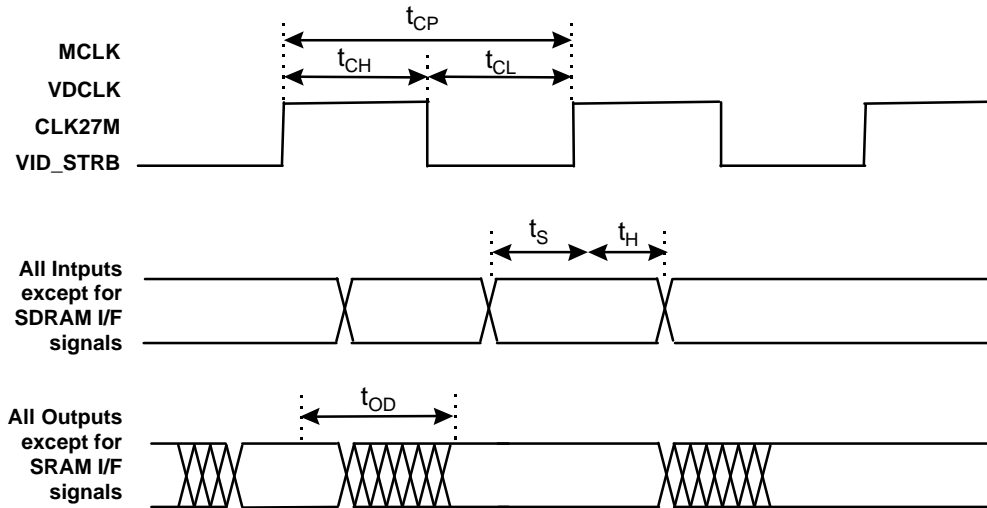
Figure 12. Input/Output Timing

SYMBOL	PARAMETERS	MIN	MAX	TYPE	UNIT
t_{CPmclk}	Clock Period	-	-	13	ns
$t_{CPvdclk}$	Clock Period	-	-	20	ns
$t_{CPclk27m}$	Clock Period	-	-	36	ns
$t_{CPvid strb}$	Clock Period	-	-	36	ns
t_{CHmclk}/t_{CLmclk}	Clock High Time/Clock Low Time	5.5	7.5	-	ns
$t_{CHvdclk}/t_{CLvdclk}$	Clock High Time/Clock Low Time	8	12	-	ns
$t_{CHclk27m}/t_{CLvdclk}$	Clock High Time/Clock Low Time	16	20	-	ns
$t_{CHvid strb}/t_{CLvdclk}$	Clock High Time/Clock Low Time	16	20	-	ns
t_H	Input Hold Time	7	-	-	ns
t_S	Input Setup Time	7	-	-	ns
t_{OD}	Output Delay Time	-	17	-	ns

*Note : Low voltage input signal rising and falling edge switching time = 1.0 ns

SDRAM I/F AC Characteristics (GDC21D401HQ)

SIGNAL	SYMBOL	MIN	MAX	TYPE	UNIT
SDRAM_DATA[63:0]	Propagation Delay	4	10.5	-	ns
	Setup Time	0	0	-	ns
	Hold Time	2	3	-	ns
SDRAM_ADDR[10:0]	Propagation Delay	4	10.5	-	ns
BA0	Propagation Delay	4	10.5	-	ns
CSN, WEN, RASN, CASN	Propagation Delay	4	10.5	-	ns

*Test Condition : Load Capacitance = 20pF

  1.Min. Condition : Temperature = 0 °C, VDD = 3.6 V

  2. Max. Condition : Temperature = 100 °C, VDD = 3.0 V

7. Package Mechanical Data

7.1 Package Pin Out

PIN	TYPE	NAME	PIN	TYPE	NAME
1	GND	VSS	41	PWR	VDD
2	I	SCANTESTON	42	I/O	SDRAM_DATA[6]
3	PWR	VDD	43	I/O	SDRAM_DATA[7]
4	I	IDCTTESTON	44	PWR	VDD
5	I	MEMTESTON	45	I/O	SDRAM_DATA[8]
6	I	CLK_27M	46	GND	VSS
7	GND	VSS	47	I/O	SDRAM_DATA[9]
8	I	\RESET	48	I/O	SDRAM_DATA[10]
9	I	TSW	49	PWR	VDD
10	I	\VIDEN	50	I/O	SDRAM_DATA[11]
11	I	VSTCW	51	I/O	SDRAM_DATA[12]
12	GND	VSS	52	GND	VSS
13	I	VID_STRB	53	I/O	SDRAM_DATA[13]
14	I	VID_DATA[0]	54	I/O	SDRAM_DATA[14]
15	I	VID_DATA[1]	55	PWR	VDD
16	I	VID_DATA[2]	56	I/O	SDRAM_DATA[15]
17	PWR	VDD	57	I/O	SDRAM_DATA[16]
18	I	VID_DATA[3]	58	GND	VSS
19	GND	VSS	59	I/O	SDRAM_DATA[17]
20	I	VID_DATA[4]	60	I/O	SDRAM_DATA[18]
21	I	VID_DATA[5]	61	GND	VSS
22	PWR	VDD	62	I/O	SDRAM_DATA[19]
23	I	VID_DATA[6]	63	PWR	VDD
24	GND	VSS	64	I/O	SDRAM_DATA[20]
25	I	VID_DATA[7]	65	GND	VSS
26	I	SCL	66	I/O	SDRAM_DATA[21]
27	GND	VSS	67	PWR	VDD
28	I/O	SDA	68	I/O	SDRAM_DATA[22]
29	O	\VID_REQ	69	GND	VSS
30	O	\UBUFF_FULL	70	I/O	SDRAM_DATA[23]
31	O	\INT_V	71	PWR	VDD
32	PWR	VDD	72	I/O	SDRAM_DATA[24]
33	I/O	SDRAM_DATA[0]	73	I/O	SDRAM_DATA[25]
34	I/O	SDRAM_DATA[1]	74	PWR	VDD
35	GND	VSS	75	I/O	SDRAM_DATA[26]
36	I/O	SDRAM_DATA[2]	76	I/O	SDRAM_DATA[27]
37	PWR	VDD	77	GND	VSS
38	I/O	SDRAM_DATA[3]	78	I/O	SDRAM_DATA[28]
39	I/O	SDRAM_DATA[4]	79	I/O	SDRAM_DATA[29]
40	I/O	SDRAM_DATA[5]	80	PWR	VDD

Package Pin Out(*continued*)

PIN	TYPE	NAME	PIN	TYPE	NAME
81	I/O	SDRAM_DATA[30]	124	GND	VSS
82	I/O	SDRAM_DATA[31]	125	I/O	SDRAM_DATA[41]
83	GND	VSS	126	I/O	SDRAM_DATA[42]
84	O	SDRAM_ADDR[3]	127	PWR	VDD
85	GND	VSS	128	I/O	SDRAM_DATA[43]
86	O	SDRAM_ADDR[4]	129	PWR	VDD
87	O	SDRAM_ADDR[2]	130	I/O	SDRAM_DATA[44]
88	PWR	VDD	131	GND	VSS
89	O	SDRAM_ADDR[5]	132	GND	VSS
90	PWR	VDD	133	I/O	SDRAM_DATA[45]
91	O	SDRAM_ADDR[1]	134	I/O	SDRAM_DATA[46]
92	O	SDRAM_ADDR[6]	135	PWR	VDD
93	PWR	VDD	136	I/O	SDRAM_DATA[47]
94	I	MCLK	137	PWR	VDD
95	GND	VSS	138	I/O	SDRAM_DATA[48]
96	GND	VSS	139	I/O	SDRAM_DATA[49]
97	GND	VSS	140	GND	VSS
98	O	SDRAM_ADDR[0]	141	I/O	SDRAM_DATA[50]
99	O	SDRAM_ADDR[7]	142	I/O	SDRAM_DATA[51]
100	PWR	VDD	143	PWR	VDD
101	O	SDRAM_ADDR[8]	144	I/O	SDRAM_DATA[52]
102	O	SDRAM_ADDR[9]	145	I/O	SDRAM_DATA[53]
103	O	SDRAM_ADDR[10]	146	GND	VSS
104	O	BA0	147	I/O	SDRAM_DATA[54]
105	GND	VSS	148	I/O	SDRAM_DATA[55]
106	O	WEN	149	PWR	VDD
107	O	CASN	150	I/O	SDRAM_DATA[56]
108	O	RASN	151	GND	VSS
109	O	CSN	152	I/O	SDRAM_DATA[57]
110	PWR	VDD	153	PWR	VDD
111	PWR	VDD	154	I/O	SDRAM_DATA[58]
112	I/O	SDRAM_DATA[32]	155	GND	VSS
113	I/O	SDRAM_DATA[33]	156	GND	VSS
114	I/O	SDRAM_DATA[34]	157	I/O	SDRAM_DATA[59]
115	GND	VSS	158	I/O	SDRAM_DATA[60]
116	I/O	SDRAM_DATA[35]	159	PWR	VDD
117	I/O	SDRAM_DATA[36]	160	PWR	VDD
118	I/O	SDRAM_DATA[37]	161	I/O	SDRAM_DATA[61]
119	PWR	VDD	162	I/O	SDRAM_DATA[62]
120	I/O	SDRAM_DATA[38]	163	I/O	SDRAM_DATA[63]
121	I/O	SDRAM_DATA[39]	164	GND	VSS
122	GND	VSS	165	I	VDCLK
123	I/O	SDRAM_DATA[40]	166	O	SCLK

Package Pin Out(*continued*)

PIN	TYPE	NAME	PIN	TYPE	NAME
167	PWR	VDD	204	O	PDATA[14]
168	O	MBCLK	205	PWR	VDD
169	O	MBFI	206	O	PDATA[15]
170	GND	VSS	207	O	PDATA[16]
171	O	\FFPN	208	O	PDATA[17]
172	PWR	VDD	209	PWR	VDD
173	PWR	VDD	210	O	PDATA[18]
174	O	DIS_INFO	211	O	PDATA[19]
175	O	D_INFO_WIN	212	GND	VSS
176	GND	VSS	213	O	PDATA[20]
177	O	PDWIN	214	O	PDATA[21]
178	O	PSTR[0]	215	O	PDATA[22]
179	O	PSTR[1]	216	O	PDATA[23]
180	GND	VSS	217	PWR	VDD
181	GND	VSS	218	O	PDATA[24]
182	O	PDATA[0]	219	O	PDATA[25]
183	O	PDATA[1]	220	O	PDATA[26]
184	O	PDATA[2]	221	O	PDATA[27]
185	PWR	VDD	222	GND	VSS
186	PWR	VDD	223	GND	VSS
187	O	PDATA[3]	224	O	PDATA[28]
188	GND	VSS	225	O	PDATA[29]
189	GND	VSS	226	O	PDATA[30]
190	O	PDATA[4]	227	O	PDATA[31]
191	O	PDATA[5]	228	PWR	VDD
192	O	PDATA[6]	229	PWR	VDD
193	O	PDATA[7]	230	I	PIC_DIS_SYNC
194	PWR	VDD	231	I	P_WAIT
195	O	PDATA[8]	232	GND	VSS
196	O	PDATA[9]	233	O	DEC_ERROR
197	PWR	VDD	234	I	MCLK_IN
198	O	PDATA[10]	235	O	FP_FD
199	GND	VSS	236	O	TEST_OUT[2]
200	O	PDATA[11]	237	O	MCLK_OUT
201	GND	VSS	238	I	P_SHARE_IN[8]
202	O	PDATA[12]	239	I	P_SHARE_IN[9]
203	O	PDATA[13]	240	I	P_SHARE_IN[10]

7.2 Physical Dimension

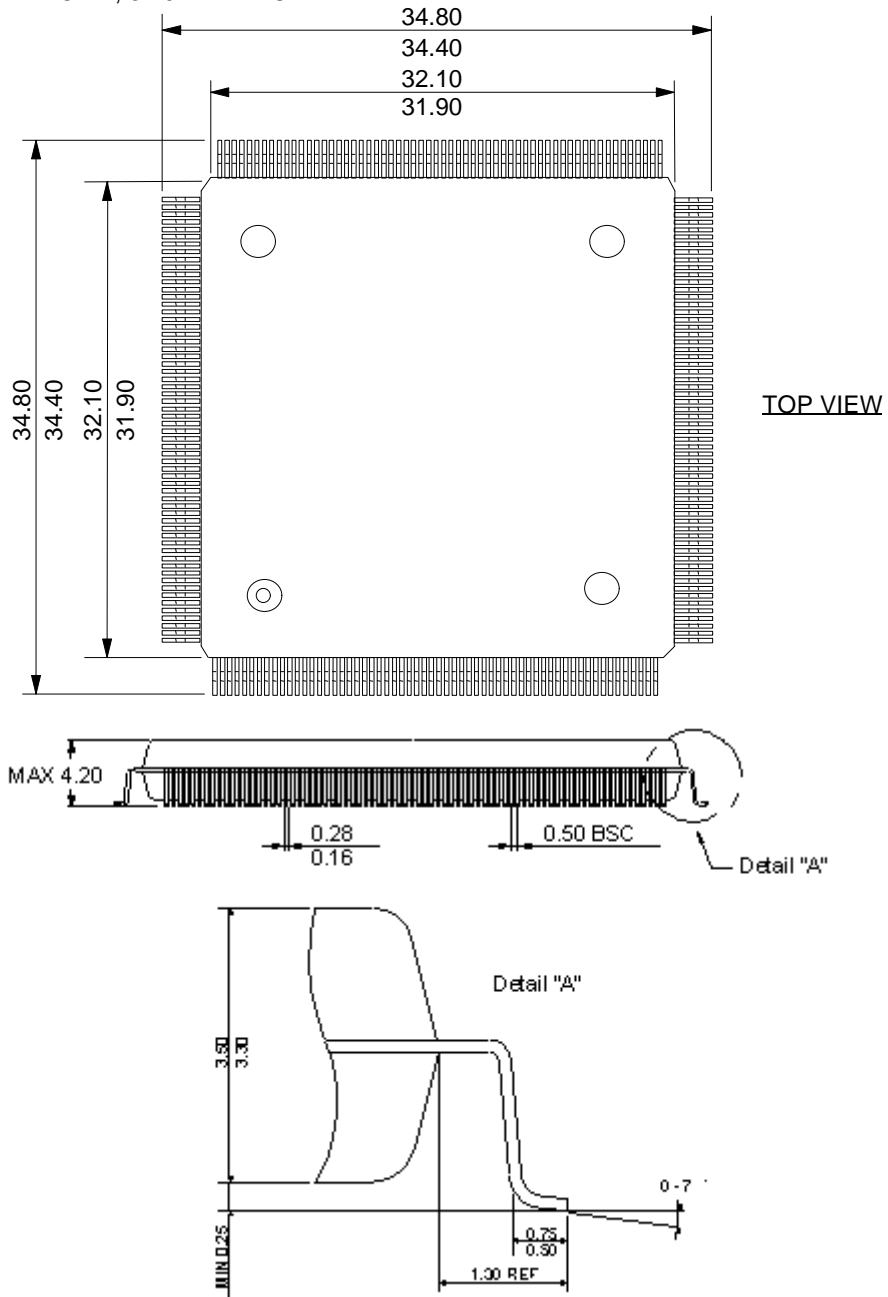PACKAGE CONTROL OUTLINE, 240Pin Hit-spread Quad Flat Package(HQFP), 32x32 mm^2 BODY, 1.30/0.38 mm FORM, 3.40 mm THICK

Figure 13. Physical Dimensions