

PRELIMINARY

September 1998

OBSOLETE PRODUCT
 No Recommended Replacement
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**CDMA/AMPS, UpConverter
 with Gain Control**

Features

- RF Frequency Range 825MHz to 850MHz
- IF Operation 10MHz to 210MHz
- Gain Control Range >40dB
- Single Supply Battery Operation 2.7V to 3.3V
- High Output 1dB Compression +13dBm
- High Power Gain 30dB
- Power Enable/Disable Control

Applications

- IS95A CDMA/AMPS Dual Mode Handsets
- Cellular Data
- CDMA/TDMA Packet Protocol Radios
- Full Duplex Transceivers
- Portable Battery Powered Equipment



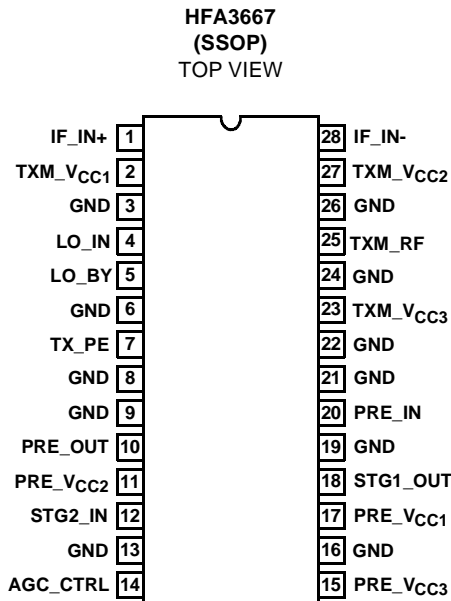
Description

The HFA3667 UpConverter is a monolithic bipolar upconverter with gain control for CDMA/AMPS cellular applications. Manufactured in the Intersil UHF1X process, the device consists of a double balanced mixer followed by a variable gain power preamplifier. The device is designed for high output compression of +13dBm and requires low drive levels from the local oscillator. The HFA3667 is one of the four chips in the PRISM™ chip set and is housed in a small outline 28 lead SSOP package ideally suited for cellular handset applications.

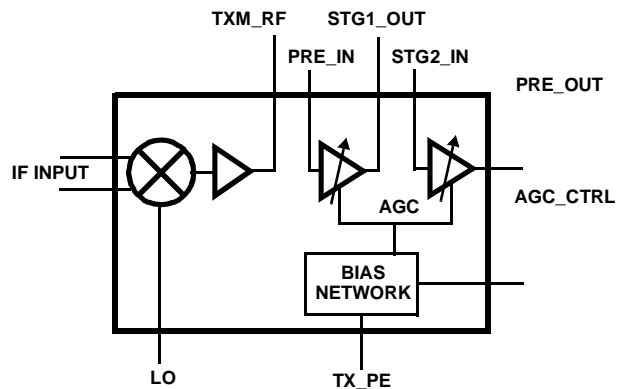
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3667IA	-40 to 85	28 Ld SSOP	M28.15
HFA3667IA96	-40 to 85	Tape and Reel	

Pinout



Block Diagram



HFA3667

Pin Descriptions

PIN NUMBER	NAME	DESCRIPTION
1	IF_IN+	Transmit Mixer Positive IF Input. Requires DC blocking capacitor.
2	TXM_VCC1	Mixer Power Supply Pin.
4	LO_IN	Local Oscillator Input. Requires DC blocking capacitor.
5	LO_BY	Local Oscillator Input Bypass. Requires high quality decoupling to ground.
3, 6, 8, 9, 13, 16, 19, 21, 22, 24, 26	GND	Internal Circuits Ground Returns.
7	TX_PE	Power Enable Control Input. HIGH for normal operation. LOW for power down.
10	PRE_OUT	Second Stage Preamplifier Output. Requires DC blocking capacitor.
11	PRE_VCC2	Second Stage Preamplifier Power Supply Pin. Use high quality decoupling capacitors.
12	STG2_IN	Second Stage Preamplifier Input. Requires DC blocking capacitor.
14	AGC_CTRL	Preamplifiers Gain control DC Voltage input.
15	PRE_VCC3	Preamplifiers Bias Power Supply Pin. Use high quality decoupling capacitors.
17	PRE_VCC1	First Stage Preamplifier Power Supply Pin. Use high quality decoupling capacitors.
18	STG1_OUT	First Stage Preamplifier Output. Requires DC blocking capacitor.
20	PRE_IN	First Stage Preamplifier Input. Requires DC blocking capacitor.
23	TXM_VCC2	Transmit Mixer Bias Power Supply Pin. Use high quality decoupling capacitors.
25	TXM_RF	Transmit Mixer RF Output. Requires DC blocking capacitor.
27	TXM_VCC3	Transmit Mixer Output Buffer Power Supply Pin. Use high quality decoupling capacitors.
28	IF_IN-	Transmit Mixer Negative IF Input. Requires DC blocking capacitor.

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Absolute Maximum Ratings

Supply Voltage -0.3 to 3.6V
 Voltage on Any Other Pin -0.3 to V_{CC} +0.3V

Operating Conditions

Supply Voltage Range 2.7V to 3.3V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
 SSOP Package 88
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Temperature Range -40°C ≤ T_A ≤ 85°C
 Maximum Storage Temperature Range -65°C ≤ T_A ≤ 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C
 (Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{CC} = 2.7V, LO_IN = -3dBm, AGC_CTRL = 0.7VDC (Max Gain), TXM_IF = -30dBm

PARAMETER	TEST CONDITION	(NOTE 2) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
OVERALL CASCADED PERFORMANCE: LO_IN = -3dBm at 980MHz, TXM_IF = Differential -30dBm, at 130MHz, Interstage Filter Insertion Loss of -3.7dB with an LO rejection of 35dB. Refer to applications diagram							
Power Gain 250Ω In, 50Ω Out	Refer to applications diagram and single to differential input network. (0dB Attenuation) AGC_CTRL = 0.7V	A	25	25	31.9	35	dB
Voltage Gain 250Ω In, 50Ω oUt		B	25	18	23	28	dB
SSB NF		B	25	-	15	-	dB
P1dBO		A	25	11.4	13.8	-	dBm
SSB NF	AGC_CTRL set for 10dB attenuation	B	25	-	15	-	dB
P1dBO		A	25	-	7.2	-	dBm
SSB NF	AGC_CTRL set for 20dB attenuation	B	25	-	15.5	-	dB
P1dBO		A	25	-	-7.4	-	dBm
SSB NF	AGC_CTRL set for 30dB attenuation	B	25	-	17.8	-	dB
P1dBO		A	25	-	-22	-	dBm
SSB NF	AGC_CTRL set for 40dB attenuation	B	25	-	24	-	dB
P1dBO		A	25	-	-35.9	-	dBm
Gain Flatness Across 825 to 850MHz	(0dB Attenuation)	B	25	-1.7	-	+1.7	dB
LO Leakage	(0dB attenuation)	A	25	-	-43	-30	dB
CASCADED AMPLIFIERS SPECIFICATIONS AT 850MHz							
RF Frequency Range (typical)		B	25	825	-	850	MHz
Power/Voltage Gain	(0dB Attenuation) AGC_CTRL = 0.7V	B	25	-	22	-	dB
SSB NF		B	25	-	7.4	-	dB
P1dBO		B	25	-	14.5	-	dBm
SSB NF	AGC_CTRL set for 10dB attenuation	B	25	-	8.2	-	dB
P1dBO		B	25	-	9.5	-	dBm
SSB NF	AGC_CTRL set for 20dB attenuation	B	25	-	11.8	-	dB
P1dBO		B	25	-	-8.2	-	dBm
CASCADED AMPLIFIERS SPECIFICATIONS AT 850MHz							
SSB NF	AGC_CTRL set for 30dB attenuation	B	25	-	17.9	-	dB
P1dBO		B	25	-	-22	-	dBm

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Electrical Specifications $V_{CC} = 2.7V$, $LO_IN = -3dBm$, $AGC_CTRL = 0.7VDC$ (Max Gain), $TXM_IF = -30dBm$ (Continued)

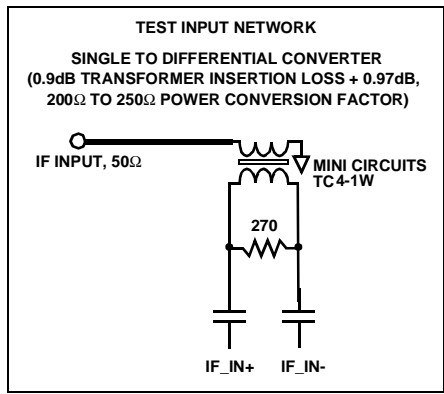
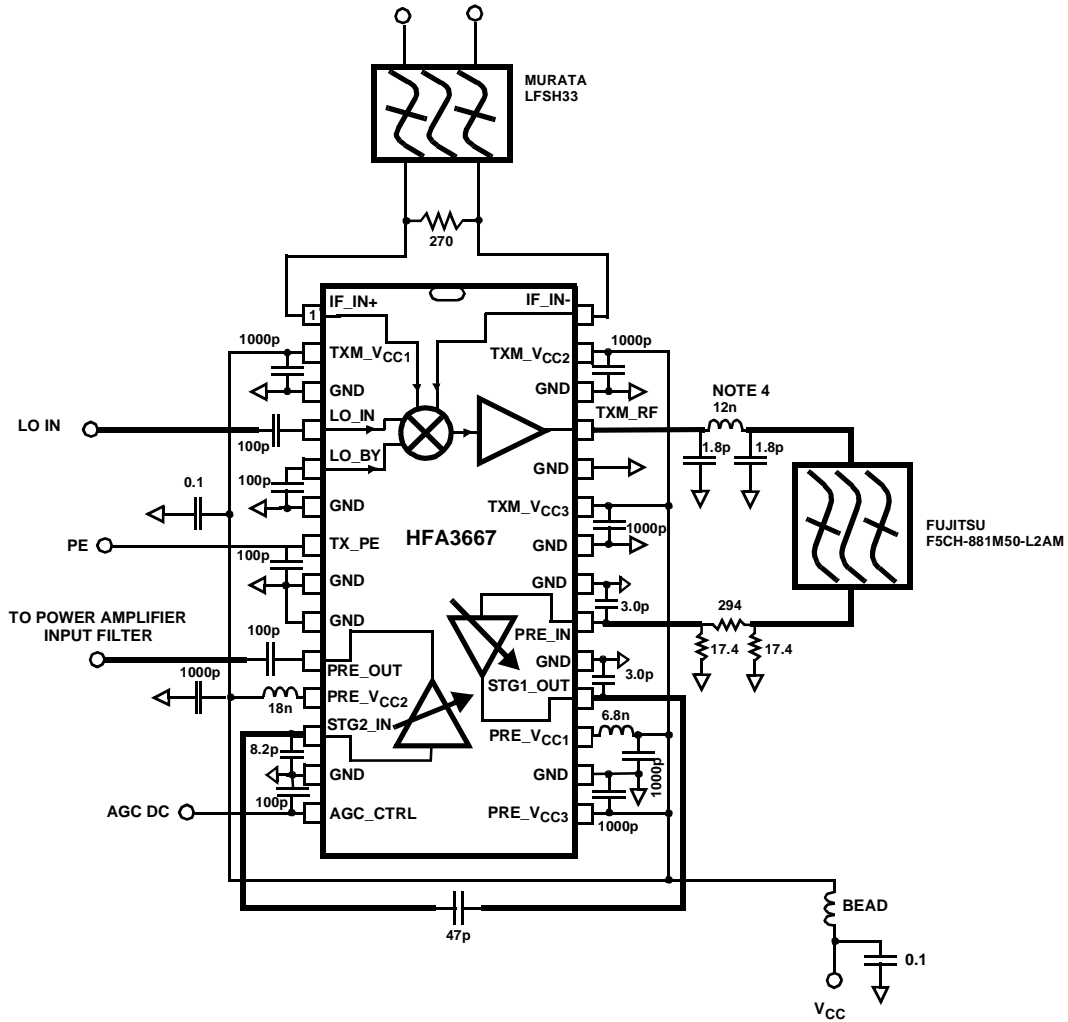
PARAMETER	TEST CONDITION	(NOTE 2) TEST LEVEL	TEMP (°C)	MIN	TYP	MAX	UNITS
SSB NF	AGC_CTRL set for 40dB attenuation	B	25	-	27	-	dB
P1dBO		B	25	-	-36	-	dBm
Output Return Loss	Over AGC Range	A	25	-	-14	-7.4	dB
Input Return Loss		B	25	-	-14	-7.4	dB
Insertion Phase vs AGC		B	25	-	2	-	Deg/dB
Reverse Isolation		B	25	-	-50	-	dB
Gain Control Voltage		A	25	0.5	-	2.0	V
Gain Control Sensitivity		A	25	-	76	-	dB/V
Gain Control Slope Change		B	25	-	-	3:1	-
Gain Control Input Impedance		C	25	-	1	-	MΩ
Gain Switching Speed, Full Scale	To ±1dB Settling	B	25	-	0.5	10	μs
MIXER SPECIFICATIONS AT TXM_IF = Differential -30dBm at 130MHz, LO_IN = -3dBm at 980MHz							
RF Output Frequency Range (Typical)		B	25	825	-	850	MHz
IF Input Frequency Range (Typical)		B	25	10	130	200	MHz
LO Frequency Range		B	25	955	-	980	MHz
LO Input Drive Level		B	25	-10	-3	0	
Power Gain 250Ω In 50Ω Out		B	25	-	11	-	dB
Voltage Gain 250Ω In 50Ω Out		B	25	-	4	-	dB
SSB NF		B	25	-	15.0	17	dB
P1dBO		B	25	-	-1	-	dBm
LO to RF Leakage		B	25	-	-26	-20	dBm
RF Input Return Loss		B	25	-	-9	-	dB
LO Input Return Loss		A	25	-	-14	-	dB
IF Differential Input Resistance		C	25	-	700	-	Ω
IF Differential Input Capacitance		C	25	-	1.8	-	pF
POWER SUPPLY AND LOGIC SPECIFICATIONS							
Total Supply Current at G_{MAX}		A	25	-	85	-	mA
Total Supply Current at G_{MIN}		A	25	-	35	-	mA
PE Logic Input Low Level		A	25	-0.2	-	0.8	V
PE Logic Input High Level		A	25	2.0	-	V_{CC}	V
POWER SUPPLY AND LOGIC SPECIFICATIONS							
PE Logic High Input Bias Current	$V_{PE} = 3.0V$	A	25	-200	-	200	μA
PE Logic Low Input Bias Current	$V_{PE} = 0.0V$	A	25	-200	-	200	μA
Power Enable Time	50%(VPE) to 90%(Icc)	B	25	-	2.0	-	μs
Power Disable Time	50%(VPE) to 10%(Icc)	B	25	-	0.5	-	μs

NOTE:

2. A = Production Tested, B = Based on Characterization, C = By Design

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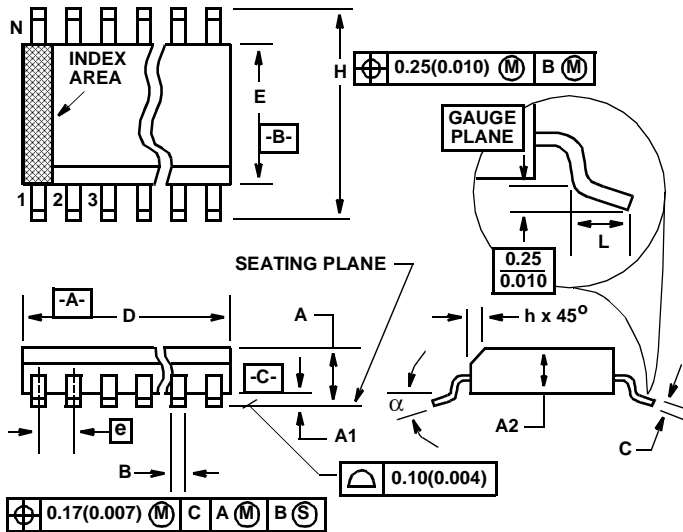
Typical Application Circuit



NOTES:

- 3. Suggested filters have no DC coupling paths. DC blocking capacitors are not required at the respective ports.
- 4. Pi network for gain flatness across the band.

Shrink Small Outline Plastic Packages (SSOP)



M28.15
28 LEAD SHRINK NARROW BODY SMALL OUTLINE
PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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