Data Sheet | May 1999 | FN3177.3

Dual FIR Filter

The HSP43168/883 Dual FIR Filter consists of two independent 8-tap FIR filters. Each filter supports decimation from 1 to 16 and provides on-board storage for 32 sets of coefficients. The Block Diagram shows two FIR cells each fed by a separate coefficient bank and one of two separate inputs. The outputs of the FIR cells are either summed or multiplexed by the MUX/Adder. The compute power in the FIR Cells can be configured to provide quadrature filtering, complex filtering, 2-D convolution, 1-D/2-D correlations, and interpolating/decimating filters.

The FIR cells take advantage of symmetry in FIR coefficients by pre-adding data samples prior to multiplication. This allows an 8-tap FIR to be implemented using only 4 multipliers per filter cell. These cells can be configured as either a single 16-tap FIR filter or dual 8-tap FIR filters. Asymmetric filtering is also supported.

Decimation of up to 16 is provided to boost the effective number of filter taps from 2 to 16 times. Further, the Decimation Registers provide the delay necessary for fractional data conversion and 2-D filtering with kernels to 16 x 16.

The flexibility of the dual is further enhanced by 32 sets of user programmable coefficients. Coefficient selection may be changed asynchronously from clock to clock. The ability to toggle between coefficient sets further simplifies applications such as polyphase or adaptive filtering.

The HSP43168 is a low power fully static design implemented in an advanced CMOS process. The configuration of the device is controlled through a standard microprocessor interface.

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Two Independent 8-Tap FIR Filters Configurable as a Single 16-Tap FIR
- 10-Bit Data and Coefficients
- On-Board Storage for 32 Programmable Coefficient Sets
- Up To: 256 FIR Taps, 16 x 16 2-D Kernels, or 10 x 20-Bit Data and Coefficients
- Programmable Decimation to 16
- Programmable Rounding on Output
- Standard Microprocessor Interface
- 33MHz, 25.6MHz Versions

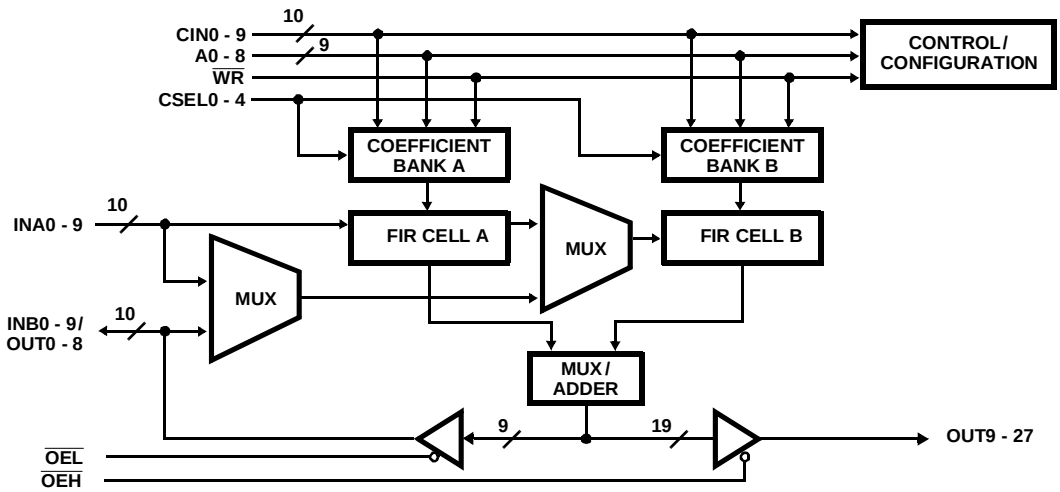
Applications

- Quadrature, Complex Filtering
- Correlation
- Image Processing
- PolyPhase Filtering
- Adaptive Filtering

Ordering Information

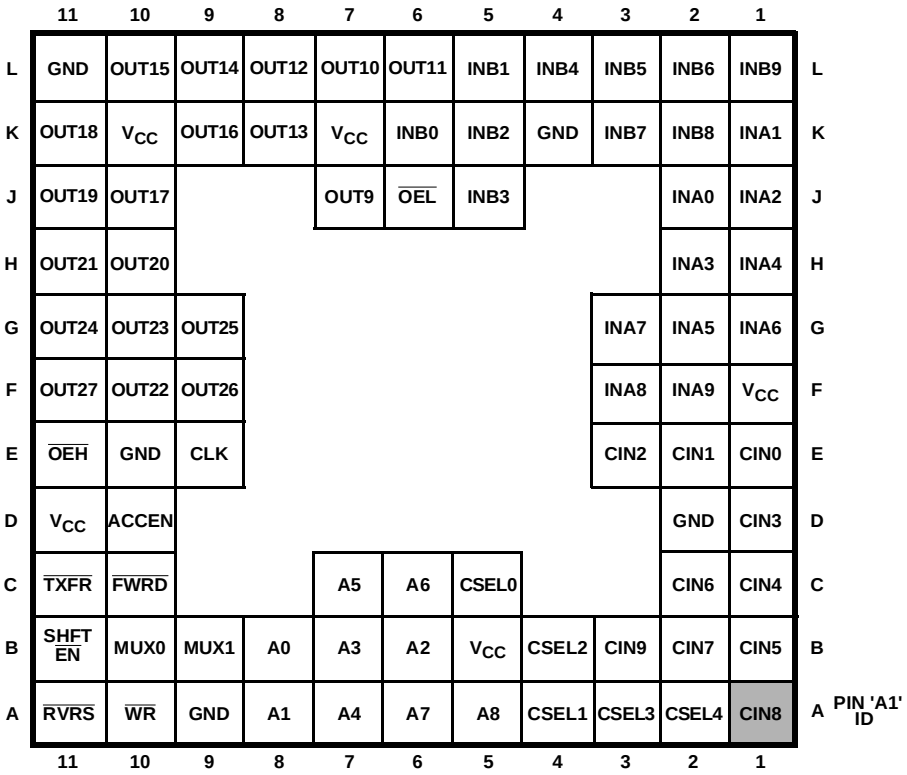
PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HSP43168GM-25/883	-55 to 125	84 Ld PGA	G84.A
HSP43168GM-33/883	-55 to 125	84 Ld PGA	G84.A

Block Diagram



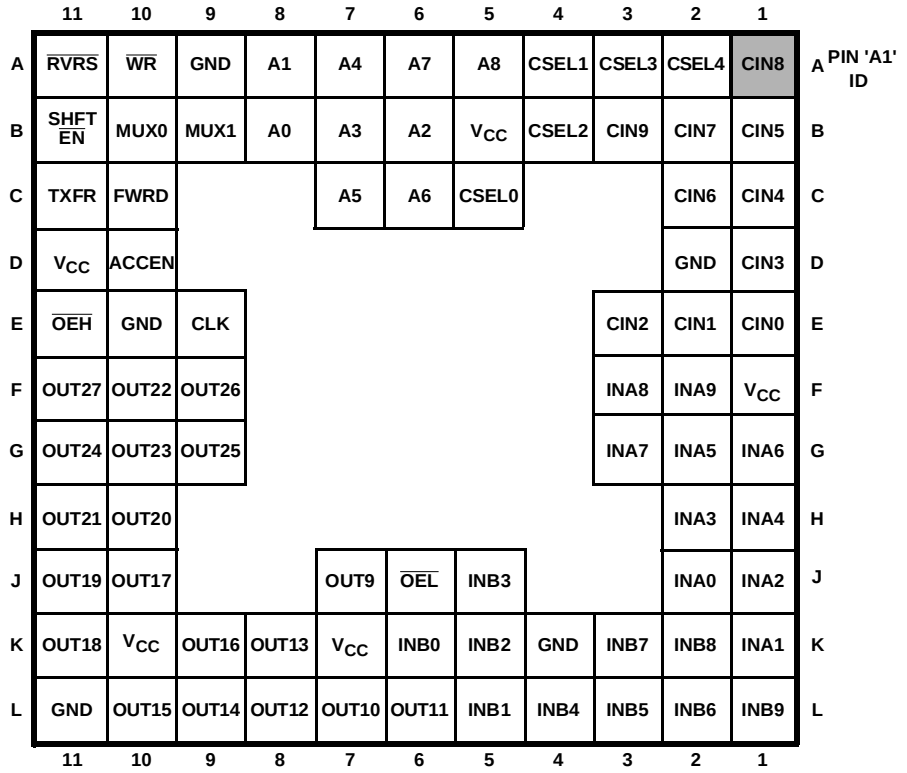
Pinouts

84 PIN PGA
TOP VIEW



	11	10	9	8	7	6	5	4	3	2	1	
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9	L
K	OUT18	V_{CC}	OUT16	OUT13	V_{CC}	INB0	INB2	GND	INB7	INB8	INA1	K
J	OUT19	OUT17			OUT9	$\overline{OEL}$	INB3			INA0	INA2	J
H	OUT21	OUT20								INA3	INA4	H
G	OUT24	OUT23	OUT25						INA7	INA5	INA6	G
F	OUT27	OUT22	OUT26						INA8	INA9	V_{CC}	F
E	$\overline{OEH}$	GND	CLK						CIN2	CIN1	CIN0	E
D	V_{CC}	ACCEN								GND	CIN3	D
C	$\overline{TXFR}$	$\overline{FWRD}$			A5	A6	CSEL0			CIN6	CIN4	C
B	SHFT $\overline{EN}$	MUX0	MUX1	A0	A3	A2	V_{CC}	CSEL2	CIN9	CIN7	CIN5	B
A	$\overline{RVRS}$	$\overline{WR}$	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8	A PIN 'A1' ID
	11	10	9	8	7	6	5	4	3	2	1	

84 PIN PGA
BOTTOM VIEW



	11	10	9	8	7	6	5	4	3	2	1	
A	$\overline{RVRS}$	$\overline{WR}$	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8	A PIN 'A1' ID
B	SHFT $\overline{EN}$	MUX0	MUX1	A0	A3	A2	V_{CC}	CSEL2	CIN9	CIN7	CIN5	B
C	TXFR	FWRD			A5	A6	CSEL0			CIN6	CIN4	C
D	V_{CC}	ACCEN								GND	CIN3	D
E	$\overline{OEH}$	GND	CLK						CIN2	CIN1	CIN0	E
F	OUT27	OUT22	OUT26						INA8	INA9	V_{CC}	F
G	OUT24	OUT23	OUT25						INA7	INA5	INA6	G
H	OUT21	OUT20								INA3	INA4	H
J	OUT19	OUT17			OUT9	$\overline{OEL}$	INB3			INA0	INA2	J
K	OUT18	V_{CC}	OUT16	OUT13	V_{CC}	INB0	INB2	GND	INB7	INB8	INA1	K
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9	L
	11	10	9	8	7	6	5	4	3	2	1	

Pin Description

NAME	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	B5, D11, K10, K7, F1		V_{CC}: +5V power supply pin.
GND	A9, E10, L11, K4, D2		Ground.
CIN0-9	E1-3, D1, C1-2, B1-3, A1	I	Control/Coefficient Data Bus. Processor interface for loading control data and coefficients. CIN0 is the LSB.
A0-8	A5-8, B6-8, C6-7	I	Control/Coefficient Address Bus. Processor interface for addressing control and Coefficient Registers. A0 is the LSB.
$\overline{WR}$	A10	I	Control/Coefficient Write Clock. Data is latched into the Control and Coefficient Registers on the rising edge of $\overline{WR}$.
CSEL0-4	A2-4, B4, C5	I	Coefficient Select. This input determines which of the 32 coefficient sets are to be used by FIR A and B. This input is registered and CSEL0 is the LSB.
INA0-9	K1, J1-2, H1-2, G1-3, F2-3	I	Input to FIR A. INA0 is the LSB.
INB0-9	L1-5, K2-3, K5-6, J5	I/O	Bidirectional Input for FIR B. INB0 is the LSB and is input only. When used as output, INB1-9 is the LSB's of the output bus.
OUT9-27	F9-11, G9-11, H10-11, J10-11, J7, K11, K8-9, L6-10	O	19 MSB's of Output Bus. Data format is either unsigned or two's complement depending on configuration. OUT27 is the MSB.
$\overline{SHFTEN}$	B11	I	Shift Enable. This active low input enables shifting of data through the Decimation Registers.
$\overline{FWRD}$	C10	I	Forward ALU Input Enable. When active low, data from the forward decimation path is input to the ALU's through the "a" input. When high, the "a" inputs to the ALUs are zeroed.
$\overline{RVRS}$	A11	I	Reverse ALU Input Enable. When active low, data from the reverse decimation path is input to the ALU's through the "b" input. When high, the "b" inputs to the ALUs are zeroed.
$\overline{TXFR}$	C11	I	Data Transfer Control. This active low input switches the LIFO being read into the reverse decimation path with the LIFO being written from the forward decimation path (see Figure 1).
MUX0-1	B9-10	I	Adder/Mux Control. This input controls data flow through the output Adder/Mux. Table 3.0 lists the various configurations.
CLK	E9	I	Clock. All inputs except those associated with the processor interface (CIN0-9, A0-8, $\overline{WR}$) and the output enables ($\overline{OEL}$, $\overline{OEH}$) are registered by the rising edge of CLK.
$\overline{OEL}$	J6	I	Output Enable Low. This tristate control enables the LSB's of the output bus to INB1-9 when $\overline{OEL}$ is low.
$\overline{OEH}$	E11	I	Output Enable High. This tristate control enables OUT9-27 when $\overline{OEH}$ is low.
ACCEN	D10	I	Accumulate Enable. This active high input allows accumulation in the FIR Cell Accumulator. A low on this input latches the FIR Accumulator contents into the Output Holding Registers while zeroing the feedback path in the accumulator.

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
Lead Temperature (Soldering 10s) . . . . . 300^oC
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
Ceramic PGA Package	33.5	7.5

Maximum Package Power Dissipation at 125^oC
Ceramic PGA Package . . . . . 1.49 W
Maximum Junction Temperature . . . . . 175^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Die Characteristics

Gate Count . . . . . 32529 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. DC ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE (^oC)	LIMITS		UNITS
					MIN	MAX	
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55 \le T_A \le 125$	-	0.8	V
Logical One Input Voltage Clock	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	3.0	-	V
Logical Zero Input Voltage Clock	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	$-55 \le T_A \le 125$	-	0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -400µA V_{CC}= 4.5V (Note 1)	1, 2, 3	$-55 \le T_A \le 125$	2.6	-	V
Output LOW Voltage	V_{OL}	I_{OL} = +2.0mA V_{CC}= 4.5V (Note 1)	1, 2, 3	$-55 \le T_A \le 125$	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	-10	+10	µA
Output Leakage Current	I_O	V_{IN} = V_{CC} or GND V_{CC} = 5.5V	1, 2, 3	$-55 \le T_A \le 125$	-10	+10	µA
Standby Power Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND V_{CC} = 5.5V, Outputs Open	1, 2, 3	$-55 \le T_A \le 125$	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 25.6MHz, V_{IN} = V_{CC} or GND, V_{CC} = 5.5V (Note 2)	1, 2, 3	$-55 \le T_A \le 125$	-	281.6	mA
Functional Test	FT	(Note 3)	7, 8	$-55 \le T_A \le 125$	-	-	-

NOTES:

2. Interchanging of force and sense conditions is permitted.
3. Operating Supply Current is proportional to frequency, typical rating is 11mA/MHz.
4. Tested as follows: f = 1MHz, V_{IH} (clock inputs) = 3.4V, V_{IH} (all other inputs) = 2.6V, V_{IL} = 0.4V, $V_{OH} \ge 1.5V$, and $V_{OL} \le 1.5V$.

TABLE 2. AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 5) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE (^{O}C)	(-33MHz)		(-25MHz)		UNITS
					MIN	MAX	MIN	MAX	
CLK Period	T_{CP}		9, 10, 11	$-55 \le T_A \le 125$	30	-	39	-	ns
CLK High	T_{CH}		9, 10, 11	$-55 \le T_A \le 125$	12	-	15	-	ns
CLK Low	T_{CL}		9, 10, 11	$-55 \le T_A \le 125$	12	-	15	-	ns
$\overline{WR}$ Period	T_{WP}		9, 10, 11	$-55 \le T_A \le 125$	30	-	39	-	ns
$\overline{WR}$ High	T_{WH}		9, 10, 11	$-55 \le T_A \le 125$	12	-	15	-	ns
$\overline{WR}$ Low	T_{WL}		9, 10, 11	$-55 \le T_A \le 125$	12	-	15	-	ns
Set-up Time; A0-8 to $\overline{WR}$ Low	T_{AWS}		9, 10, 11	$-55 \le T_A \le 125$	10	-	10	-	ns
Hold Time; A0-8 to $\overline{WR}$ High	T_{AWH}		9, 10, 11	$-55 \le T_A \le 125$	1	-	1	-	ns
Set-up Time; CIN0-9 to $\overline{WR}$ High	T_{CWS}		9, 10, 11	$-55 \le T_A \le 125$	12	-	15	-	ns
Hold Time; CIN0-9 to $\overline{WR}$ High	T_{CWH}		9, 10, 11	$-55 \le T_A \le 125$	1.5	-	1.5	-	ns
Set-up Time; $\overline{WR}$ Low to CLK Low	T_{WLCL}	Note 7	9, 10, 11	$-55 \le T_A \le 125$	5	-	8	-	ns
Set-up Time; CIN0-9 to CLK Low	T_{CVCL}	Note 7	9, 10, 11	$-55 \le T_A \le 125$	8	-	8	-	ns
Set-up Time; $\overline{CSEL0\text{-}5}$, $\overline{SHFTEN}$, $\overline{FWRD}$, $\overline{RVRS}$, $\overline{TXFR}$, MUX0-1 to CLK High	T_{ECS}		9, 10, 11	$-55 \le T_A \le 125$	15	-	17	-	ns
Hold Time; $\overline{CSEL0\text{-}5}$, $\overline{SHFTEN}$, $\overline{FWRD}$, $\overline{RVRS}$, $\overline{TXFR}$, MUX0-1 to CLK High	T_{ECH}		9, 10, 11	$-55 \le T_A \le 125$	0	-	0	-	ns
CLK to Output Delay OUT0-27	T_{DO}		9, 10, 11	$-55 \le T_A \le 125$	-	15	-	17	ns
Output Enable Time	T_{OE}	Note 6	9, 10, 11	$-55 \le T_A \le 125$	-	12	-	12	ns

NOTES:

5. AC testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; input levels (all other inputs) 3.0V and 0V; timing reference levels (CLK) 2.0V; all others 1.5V. V_{CC} = 4.5V and 5.5V. Output load per test load circuit with C_L = 40 pF. Output transition is measured at V_{OH} Š > 1.5V and V_{OL} < 1.5V.
6. Transition is measured at ±200mV from steady state voltage, Output loading per test load circuit, C_L = 40pF.
7. Set-up time requirements for loading of data on CIN0-9 to guarantee recognition on the following clock.

TABLE 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE (^{O}C)	(-33MHz)		(-25MHz)		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1 MHz, All measurements are referenced to device GND.	1	T_A = 25	-	12	-	12	pF
Output Capacitance	C_{OUT}		1	T_A = 25	-	12	-	12	pF
Output Disable Time	T_{OD}		1, 2	$-55 \le T_A \le 125$	-	12	-	12	ns
Output Rise Time	t_R	From 0.8V to 2.0V	1, 2	$-55 \le T_A \le 125$	-	8	-	8	ns
Output Fall Time	t_F	From 2.0V to 0.8V	1, 2	$-55 \le T_A \le 125$	-	8	-	8	ns

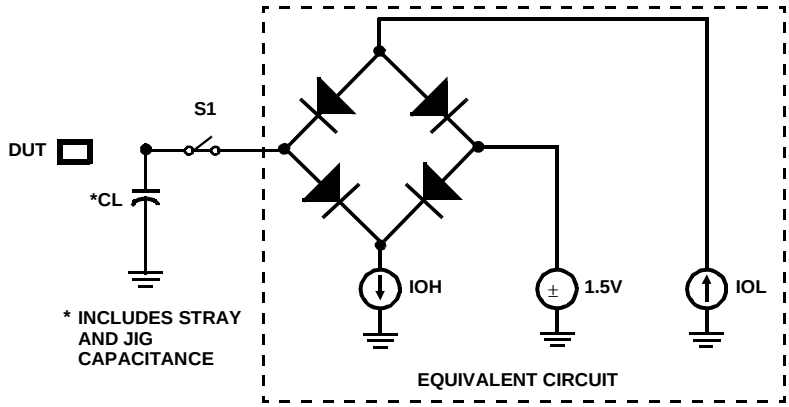
NOTES:

8. The parameters in Table 3 are controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.
9. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

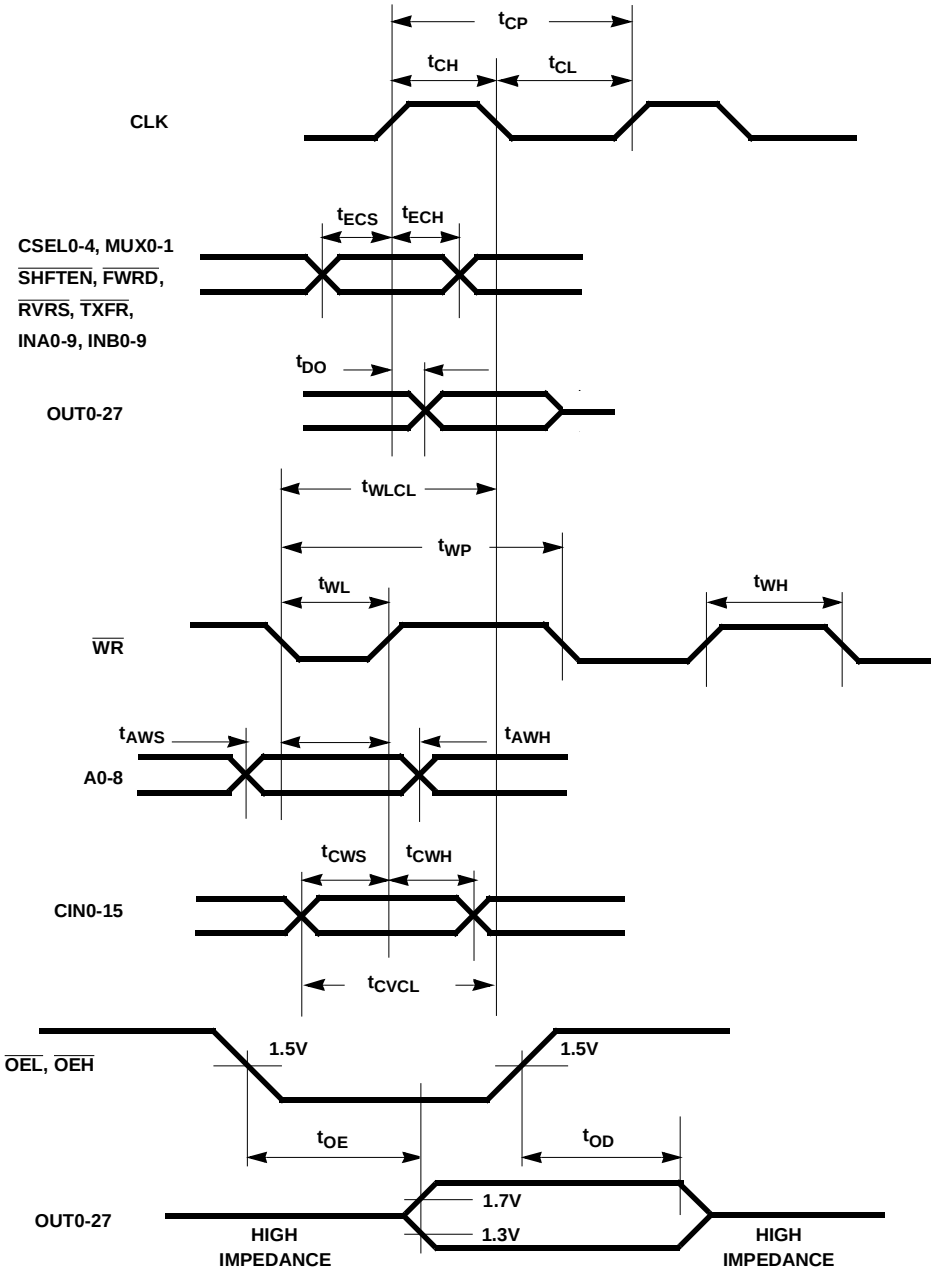
CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

AC Test Load Circuit



SWITCH S1 OPEN FOR I_{CCSB} AND I_{CCOP} TEST

Waveforms



OUTPUT ENABLE, DISABLE TIMING

OUTPUT RISE AND FALL TIMES

Burn-In Circuit

84 PIN PGA
BOTTOM VIEW

	11	10	9	8	7	6	5	4	3	2	1	
A	RVRS	$\overline{WR}$	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8	A
B	SHFT $\overline{EN}$	MUX0	MUX1	A0	A3	A2	V_{CC}	CSEL2	CIN9	CIN7	CIN5	B
C	$\overline{TXFR}$	$\overline{FWRD}$			A5	A6	CSEL0			CIN6	CIN4	C
D	V_{CC}	ACCEN								GND	CIN3	D
E	$\overline{OEH}$	GND	CLK						CIN2	CIN1	CIN0	E
F	OUT27	OUT22	OUT26						INA8	INA9	V_{CC}	F
G	OUT24	OUT23	OUT25						INA7	INA5	INA6	G
H	OUT21	OUT20								INA3	INA4	H
J	OUT19	OUT17			OUT9	$\overline{OEL}$	INB3			INA0	INA2	J
K	OUT18	V_{CC}	OUT16	OUT13	V_{CC}	INB0	INB2	GND	INB7	INB8	INA1	K
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9	L
	11	10	9	8	7	6	5	4	3	2	1	

PIN 'A1' ID

NOTES:

1. $V_{CC}/2$ (2.7V ±10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. V_{CC} = 5.5 ±0.5V.
4. 0.1µf (Min) capacitor between V_{CC} and GND per position.
5. F0 = 100KHz ±10%, F1 = F0/2, F2 = F1/2. . . , F16 = F15/2, 40 to 60% duty cycle.
6. Input voltage limits:
   V_{IL} = 0.8V Max, V_{IH} = 4.5 ±10%.

PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	CIN8	F9
A2	CSEL4	F12
A3	CSEL3	F11
A4	CSEL1	F9
A5	A8	F12
A6	A7	F10
A7	A4	F11
A8	A1	F12
A9	GND	GND
A10	WRB	F6
A11	RVRS	F12
B1	CIN5	F8
B2	CIN7	F10
B3	CIN9	F10
B4	CSEL2	F10
B5	V_{CC}	V_{CC}
B6	A2	F11
B7	A3	F10
B8	A0	F13
B9	MUX1	F13
B10	MUX0	F12
B11	SHFTEN	F14
C1	CIN4	F7
C2	CIN6	F9
C5	CSEL0	F8
C6	A6	F11
C7	A5	F12
C10	FWRD	F13
C11	TXFR	F11
D1	CIN3	F10
D2	GND	GND
D10	ACCEN	F13
D11	V_{CC}	V_{CC}
E1	CIN0	F7
E2	CIN1	F8
E3	CIN2	F9
E9	CLK	F0
E10	GND	GND
E11	OEHB	F14
F1	V_{CC}	V_{CC}
F2	INA9	F10
F3	INA8	F9

PGA PIN	PIN NAME	BURN-IN SIGNAL
F9	SUM26	$V_{CC}/2$
F10	SUM22	$V_{CC}/2$
F11	SUM27	$V_{CC}/2$
G1	INA6	F7
G2	INA5	F6
G3	INA7	F8
G9	SUM25	$V_{CC}/2$
G10	SUM23	$V_{CC}/2$
G11	SUM24	$V_{CC}/2$
H1	INA4	F5
H2	INA3	F4
H10	SUM20	$V_{CC}/2$
H11	SUM21	$V_{CC}/2$
J1	INA2	F3
J2	INA0	F1
J5	INB3	F4
J6	OELB	F13
J7	SUM9	$V_{CC}/2$
J10	SUM17	$V_{CC}/2$
J11	SUM19	$V_{CC}/2$
K1	INA1	F2
K2	INB8	F9
K3	INB7	F8
K4	GND	GND
K5	INB2	F3
K6	INB0	F1
K7	V_{CC}	V_{CC}
K8	SUM13	$V_{CC}/2$
K9	SUM16	$V_{CC}/2$
K10	V_{CC}	V_{CC}
K11	SUM18	$V_{CC}/2$
L1	INB9	F10
L2	INB6	F7
L3	INB5	F6
L4	INB4	F5
L5	INB1	F2
L6	SUM11	$V_{CC}/2$
L7	SUM10	$V_{CC}/2$
L8	SUM12	$V_{CC}/2$
L9	SUM14	$V_{CC}/2$
L10	SUM15	$V_{CC}/2$
L11	GND	GND

Die Characteristics

DIE DIMENSIONS:

314 x 348 x 19 ± 1mils

METALLIZATION:

Type: Si-Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:

Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:

1.93 x 105 A/cm2

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