

Features

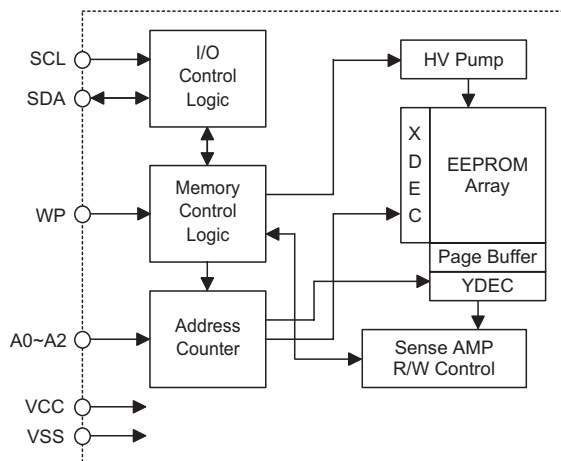
- Operating voltage: 2.2V~5.5V
- Low power consumption
 - Operation: 5mA max.
 - Standby: 5 μ A max.
- Internal organization: 1024 \times 8
- 2-wire Serial Interface
- Write cycle time: 5ms max.
- Automatic erase-before-write operation
- Partial page write allowed
- 16-byte Page Write Mode
- Write operation with built-in timer
- Hardware controlled write protection
- 40-year data retention
- 10⁶ rewrite cycles per word
- Commercial temperature range (0°C to +70°C)
- 8-pin DIP/SOP package

General Description

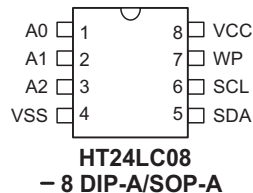
The HT24LC08 is an 8K-bit serial read/write non-volatile memory device using the CMOS floating gate process. Its 8192 bits of memory are organized into 1024 words and each word is 8 bits. The device is optimized for use in many industrial and commercial applications where

low power and low voltage operation are essential. Up to two HT24LC08 devices may be connected to the same 2-wire bus. The HT24LC08 is guaranteed for 1M erase/write cycles and 40-year data retention.

Block Diagram



Pin Assignment



Pin Description

Pin Name	I/O	Description
A0~A2	I	Address input
SDA	I/O	Serial data
SCL	I	Serial clock input
WP	I	Write protect
VSS	—	Negative power supply, ground
VCC	—	Positive power supply

Absolute Maximum Ratings

Operating Temperature (Commercial)	0°C to 70°C
Storage Temperature	-50°C to 125°C
Applied VCC Voltage with Respect to VSS	-0.3V to 6.0V
Applied Voltage on any Pin with Respect to VSS	-0.3V to V _{CC} +0.3V

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=0°C to 70°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{CC}	Conditions				
V _{CC}	Operating Voltage	—	—	2.2	—	5.5	V
I _{CC1}	Operating Current	5V	Read at 100kHz	—	—	2	mA
I _{CC2}	Operating Current	5V	Write at 100kHz	—	—	5	mA
V _{IL}	Input Low Voltage	—	—	-1	—	0.3V _{CC}	V
V _{IH}	Input High Voltage	—	—	0.7V _{CC}	—	V _{CC} +0.5	V
V _{OL}	Output Low Voltage	2.4V	I _{OL} =2.1mA	—	—	0.4	V
I _{LI}	Input Leakage Current	5V	V _{IN} =0 or V _{CC}	—	—	1	μA
I _{LO}	Output Leakage Current	5V	V _{OUT} =0 or V _{CC}	—	—	1	μA
I _{STB1}	Standby Current	5V	V _{IN} =0 or V _{CC}	—	—	5	μA
I _{STB2}	Standby Current	2.4V	V _{IN} =0 or V _{CC}	—	—	4	μA
C _{IN}	Input Capacitance (See Note)	—	f=1MHz 25°C	—	—	6	pF
C _{OUT}	Output Capacitance (See Note)	—	f=1MHz 25°C	—	—	8	pF

Note: These parameters are periodically sampled but not 100% tested

A.C. Characteristics

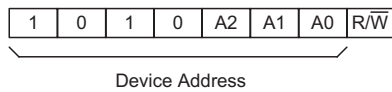
Ta=0°C to 70°C

Symbol	Parameter	Remark	Standard Mode*		V _{CC} =5V±10%		Unit
			Min.	Max.	Min.	Max.	
f _{SK}	Clock Frequency	—	—	100	—	400	kHz
t _{HIGH}	Clock High Time	—	4000	—	600	—	ns
t _{LOW}	Clock Low Time	—	4700	—	1200	—	ns
t _r	SDA and SCL Rise Time	Note	—	1000	—	300	ns
t _f	SDA and SCL Fall Time	Note	—	300	—	300	ns
t _{HD:STA}	START Condition Hold Time	After this period the first clock pulse is generated	4000	—	600	—	ns
t _{SU:STA}	START Condition Setup Time	Only relevant for repeated START condition	4000	—	600	—	ns
t _{HD:DAT}	Data Input Hold Time	—	0	—	0	—	ns
t _{SU:DAT}	Data Input Setup Time	—	200	—	100	—	ns
t _{SU:STO}	STOP Condition Setup Time	—	4000	—	600	—	ns

These page addressing bits on the 8K device should be considered the most significant bits of the data word address which follows. The A0, A1 and A2 pins have no connection.

The 8th bit device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

If the comparison of the device address succeed the EEPROM will output a zero at ACK bit. If not, the chip will return to a standby state.



Write Operations

• **Byte write**

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. After receiving the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle and EEPROM will not respond until write is complete (refer to Byte write timing).

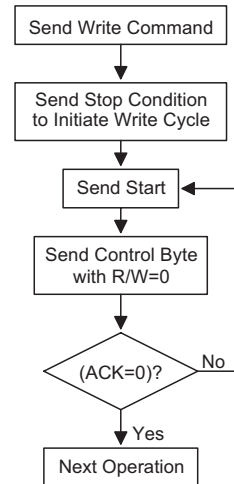
• **Page write**

The 8K EEPROM is capable of a 16-byte page write. A page write is initiated in the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges the receipt of the first data word, the microcontroller can transmit up to 15 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (refer to Page write timing).

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location.

• **Acknowledge polling**

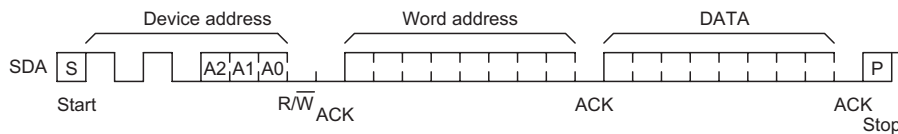
To maximize bus throughput, one technique is to allow the master to poll for an acknowledge signal after the start condition and the control byte for a write command have been sent. If the device is still busy implementing its write cycle, then no ACK will be returned. The master can send the next read/write command when the ACK signal has finally been received.



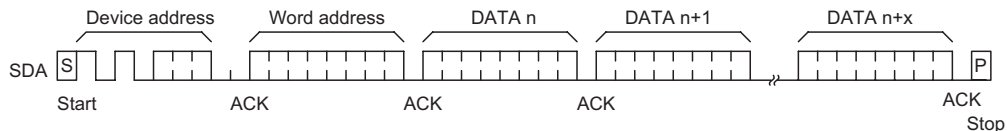
Acknowledge Polling Flow

• **Write protect**

The HT24LC08 has a write-protect function and programming will then be inhibited when the WP pin is connected to VCC. Under this mode, the HT24LC08 is used as a serial ROM.



Byte Write Timing



Page Write Timing

- Read operations

The HT24LC08 supports three read operations, namely, current address read, random address read and sequential read. During read operation execution, the read/write select bit should be set to "1".

- Current address read

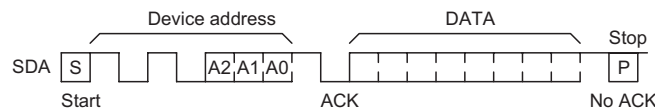
The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll over during read from the last byte of the last memory page to the first byte of the first page. The address roll over during write from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller should respond with a "no ACK" signal (high) followed by a stop condition (refer to Current read timing).

- Random read

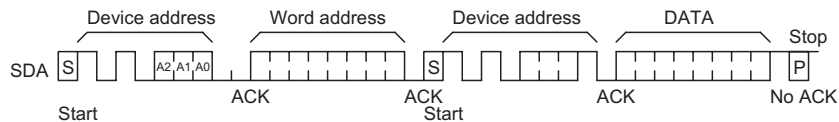
A random read requires a dummy byte write sequence to load in the data word address which is then clocked in and acknowledged by the EEPROM. The microcontroller must then generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller should respond with a "no ACK" signal (high) followed by a stop condition (refer to Random read timing).

- Sequential read

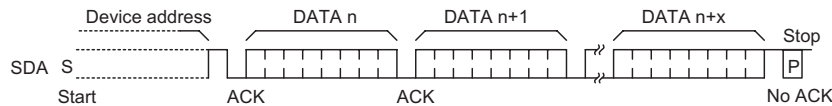
Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledgment. As long as the EEPROM receives an acknowledgment, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll over and the sequential read continues. The sequential read operation is terminated when the microcontroller responds with a "no ACK" signal (high) followed by a stop condition.



Current Read Timing

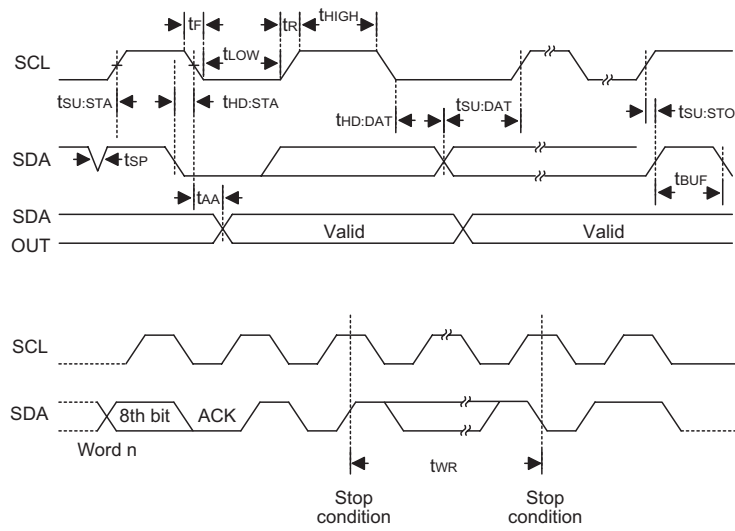


Random Read Timing



Sequential Read Timing

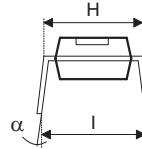
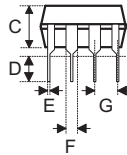
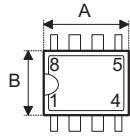
Timing Diagrams



Note: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the valid start condition of sequential command.

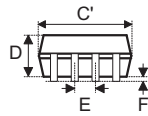
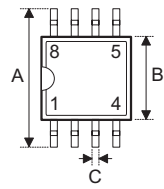
Package Information

8-pin DIP (300mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	355	—	375
B	240	—	260
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	335	—	375
α	0°	—	15°

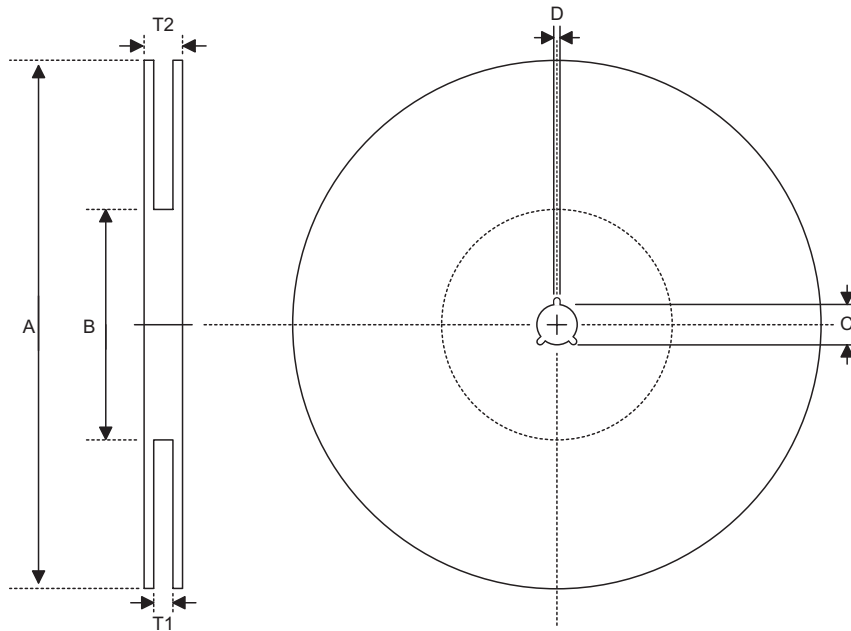
8-pin SOP (150mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	228	—	244
B	149	—	157
C	14	—	20
C'	189	—	197
D	53	—	69
E	—	50	—
F	4	—	10
G	22	—	28
H	4	—	12
α	0°	—	10°

Product Tape and Reel Specifications

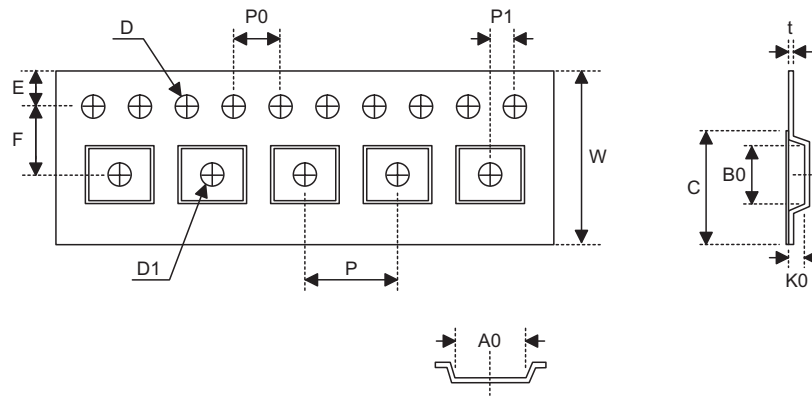
Reel Dimensions



SOP 8N

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330±1.0
B	Reel Inner Diameter	62±1.5
C	Spindle Hole Diameter	13.0+0.5 -0.2
D	Key Slit Width	2.0±0.15
T1	Space Between Flange	12.8+0.3 -0.2
T2	Reel Thickness	18.2±0.2

Carrier Tape Dimensions



SOP 8N

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	12.0+0.3 -0.1
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.1
D1	Cavity Hole Diameter	1.5+0.25
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.20±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.3±0.05
C	Cover Tape Width	9.3

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