## 75A, 30V, 0.0045 Ohm, N-Channel, Logic Level UltraFET Power MOSFETs

These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

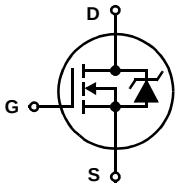
Formerly developmental type TA76145.

## Ordering Information

| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| HUF76145P3 | TO-220AB | 76145P |
| HUF76145S3S | TO-263AB | 76145S |

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF76145S3ST.

## Symbol

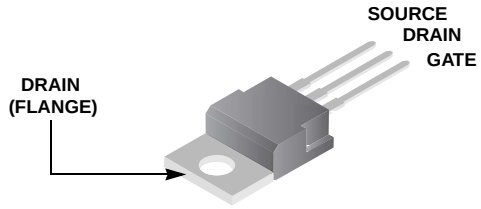



## Features

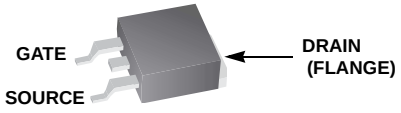
- Logic Level Gate Drive
- 75A, 30V
- Ultra Low On-Resistance, $r_{DS(ON)} = 0.0045\Omega$
- Temperature Compensating PSPICE® Model
- Temperature Compensating SABER™ Model
- Thermal Impedance SPICE Model
- Thermal Impedance SABER Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

## Packaging

**JEDEC TO-220AB**




**JEDEC TO-263AB**



## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

| | | | UNITS |
|---|---|---|---|
| Drain to Source Voltage (Note 1) | $V_{DSS}$ | 30 | V |
| Drain to Gate Voltage ($R_{GS}$ = 20kΩ) (Note 1) | $V_{DGR}$ | 30 | V |
| Gate to Source Voltage | $V_{GS}$ | ±16 | V |
| Drain Current | | | |
| Continuous ($T_C = 25^oC$, $V_{GS}$ = 10V) (Figure 2) | $I_D$ | 75 | A |
| Continuous ($T_C = 100^oC$, $V_{GS}$ = 5V) | $I_D$ | 75 | A |
| Continuous ($T_C = 100^oC$, $V_{GS}$ = 4.5V) (Figure 2) | $I_D$ | 75 | A |
| Pulsed Drain Current | $I_{DM}$ | Figure 4 | |
| Pulsed Avalanche Rating | $E_{AS}$ | Figure 6 | |
| Power Dissipation | $P_D$ | 270 | W |
| Derate Above $25^oC$ | | 2.17 | $W/^oC$ |
| Operating and Storage Temperature | $T_J$, $T_{STG}$ | -40 to 150 | $^oC$ |
| Maximum Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from Case for 10s | $T_L$ | 300 | $^oC$ |
| Package Body for 10s, See Techbrief 334 | $T_{pkg}$ | 260 | $^oC$ |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $T_J = 25^oC$ to $150^oC$.

## Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **OFF STATE SPECIFICATIONS** | | | | | | |
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = 250μA, $V_{GS}$ = 0V (Figure 12) | 30 | - | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 25V, $V_{GS}$ = 0V | - | - | 1 | μA |
| | | $V_{DS}$ = 25V, $V_{GS}$ = 0V, $T_C = 150^oC$ | - | - | 250 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±16V | - | - | ±100 | nA |
| **ON STATE SPECIFICATIONS** | | | | | | |
| Gate to Source Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA (Figure 11) | 1 | - | 3 | V |
| Drain to Source On Resistance | $r_{DS(ON)}$ | $I_D$ = 75A, $V_{GS}$ = 10V (Figures 9, 10) | - | 0.0035 | 0.0045 | Ω |
| | | $I_D$ = 75A, $V_{GS}$ = 5V (Figure 9) | - | 0.0043 | 0.0058 | Ω |
| | | $I_D$ = 75A, $V_{GS}$ = 4.5V (Figure 9) | - | 0.0046 | 0.0065 | Ω |
| **THERMAL SPECIFICATIONS** | | | | | | |
| Thermal Resistance Junction to Case | $R_{\theta JC}$ | (Figure 3) | - | - | 0.46 | $^oC/W$ |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | TO-220 and TO-263 | - | - | 62 | $^oC/W$ |
| **SWITCHING SPECIFICATIONS** ($V_{GS}$ = 4.5V) | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{DD}$ = 15V, $I_D \cong$ 75A, $R_L$ = 0.20Ω, $V_{GS}$ = 4.5V, $R_{GS}$ = 2.5Ω (Figure 15) | - | - | 255 | ns |
| Turn-On Delay Time | $t_{d(ON)}$ | | - | 26 | - | ns |
| Rise Time | $t_r$ | | - | 145 | - | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | - | 35 | - | ns |
| Fall Time | $t_f$ | | - | 39 | - | ns |
| Turn-Off Time | $t_{OFF}$ | | - | - | 110 | ns |

**Electrical Specifications** $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **SWITCHING SPECIFICATIONS** ($V_{GS}$ = 10V) | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{DD}$ = 15V, $I_D \cong$ 75A, $R_L$ = 0.20Ω, $V_{GS}$ = 10V, $R_{GS}$ = 2.2Ω (Figure 16) | | - | - | 110 | ns |
| Turn-On Delay Time | $t_{d(ON)}$ | | | - | 16 | - | ns |
| Rise Time | $t_r$ | | | - | 57 | - | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | - | 53 | - | ns |
| Fall Time | $t_f$ | | | - | 38 | - | ns |
| Turn-Off Time | $t_{OFF}$ | | | - | - | 135 | ns |
| **GATE CHARGE SPECIFICATIONS** | | | | | | | |
| Total Gate Charge | $Q_{g(TOT)}$ | $V_{GS}$ = 0V to 10V | $V_{DD}$ = 15V, $I_D \cong$ 75A, $R_L$ = 0.20Ω $I_{g(REF)}$ = 1.0mA (Figure 14) | - | 130 | 156 | nC |
| Gate Charge at 5V | $Q_{g(5)}$ | $V_{GS}$ = 0V to 5V | | - | 73 | 88 | nC |
| Threshold Gate Charge | $Q_{g(TH)}$ | $V_{GS}$ = 0V to 1V | | - | 4.65 | 5.6 | nC |
| Gate to Source Gate Charge | $Q_{gs}$ | | | - | 12.30 | - | nC |
| Gate to Drain “Miller” Charge | $Q_{gd}$ | | | - | 40.00 | - | nC |
| **CAPACITANCE SPECIFICATIONS** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{DS}$ = 25V, $V_{GS}$ = 0V, f = 1MHz (Figure 13) | | - | 4900 | - | pF |
| Output Capacitance | $C_{OSS}$ | | | - | 2520 | - | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | - | 560 | - | pF |

**Source to Drain Diode Specifications**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Source to Drain Diode Voltage | $V_{SD}$ | $I_{SD}$ = 75A | - | - | 1.25 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_{SD}$ = 75A, $dI_{SD}/dt$ = 100A/μs | - | - | 115 | ns |
| Reverse Recovered Charge | $Q_{RR}$ | $I_{SD}$ = 75A, $dI_{SD}/dt$ = 100A/μs | - | - | 255 | nC |

## *Typical Performance Curves*

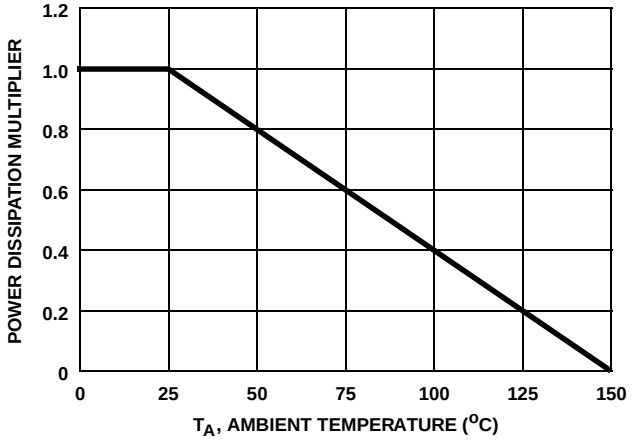



**FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE**

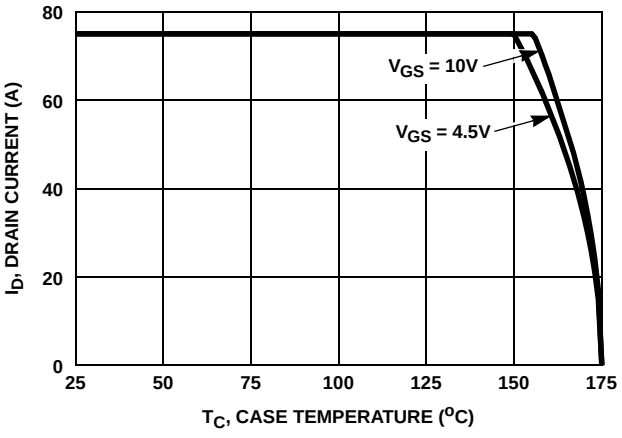



**FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE**

## Typical Performance Curves (Continued)

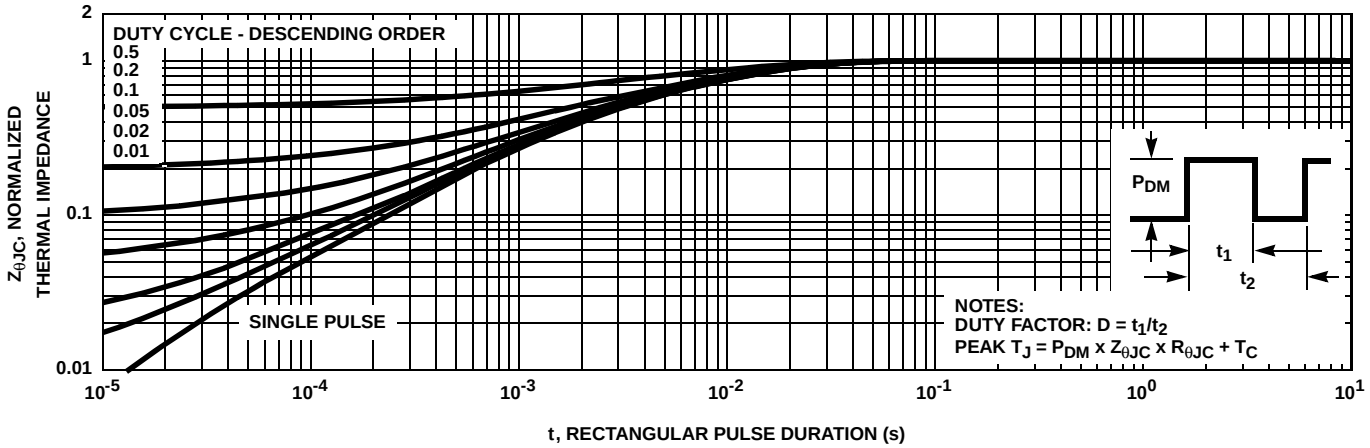



FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

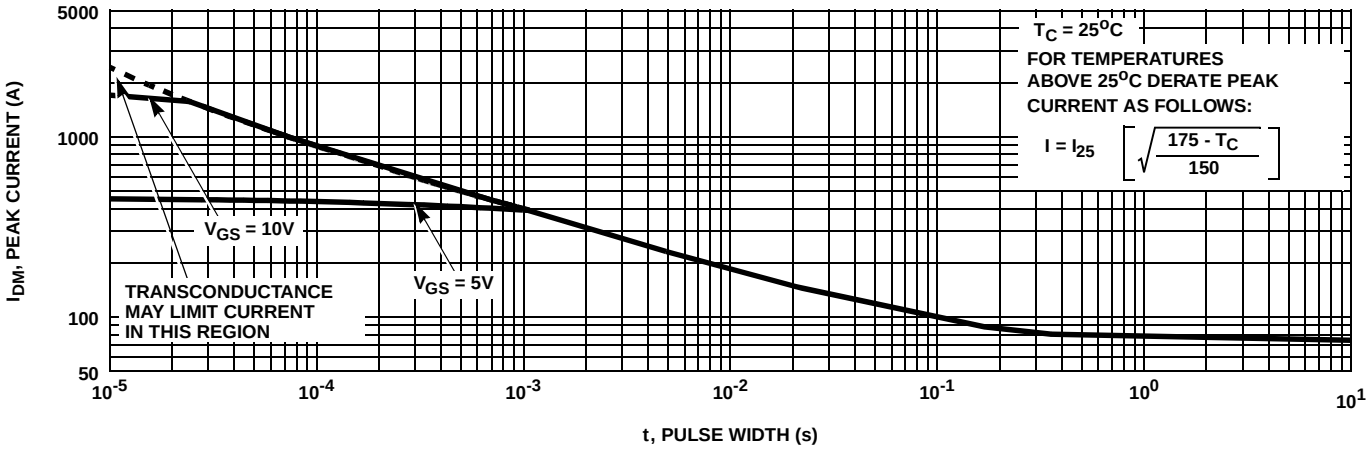



FIGURE 4. PEAK CURRENT CAPABILITY

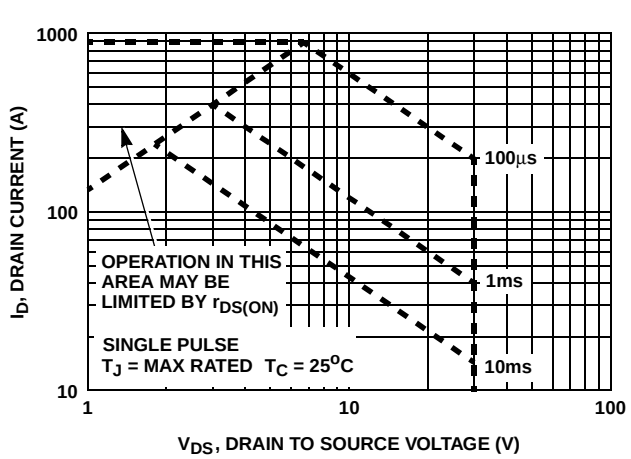
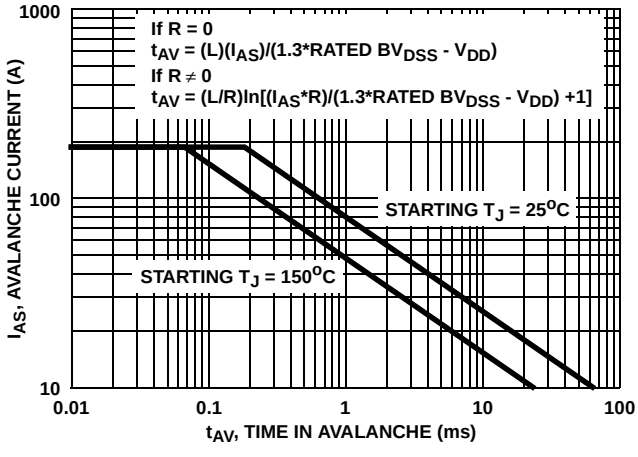



FIGURE 5. FORWARD BIAS SAFE OPERATING AREA




NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

## Typical Performance Curves (Continued)

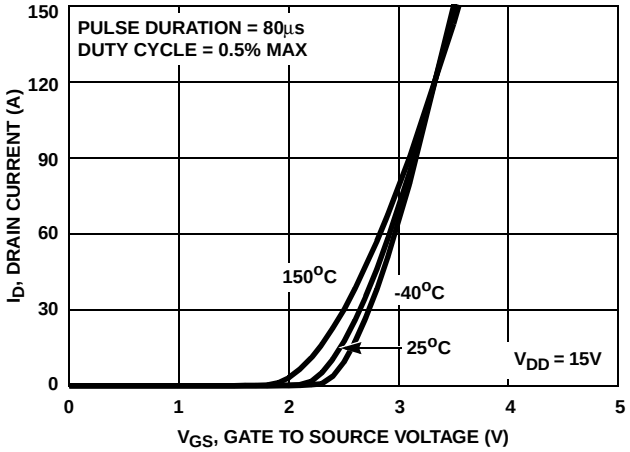



FIGURE 7. TRANSFER CHARACTERISTICS

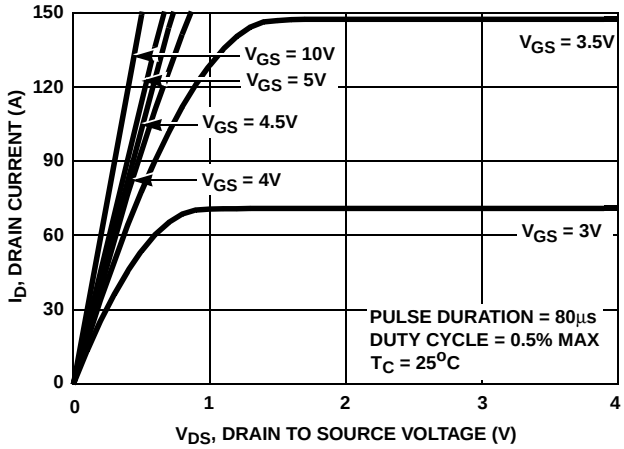



FIGURE 8. SATURATION CHARACTERISTICS

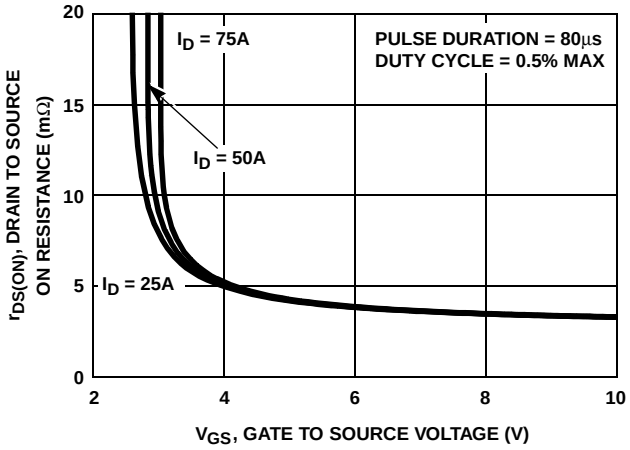



FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

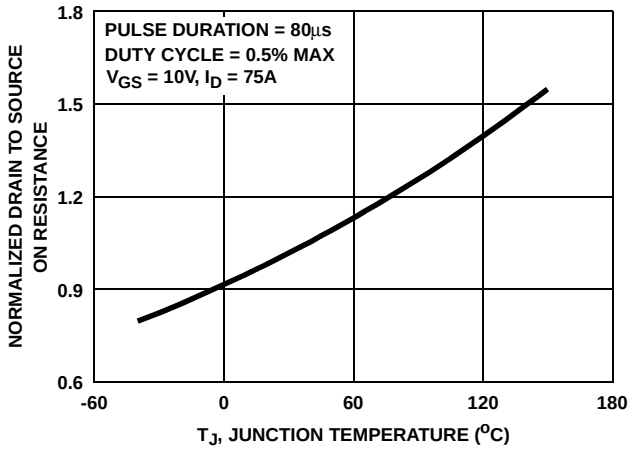



FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

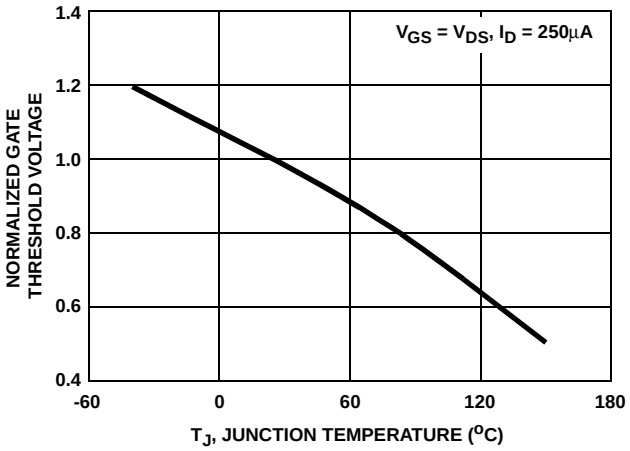



FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

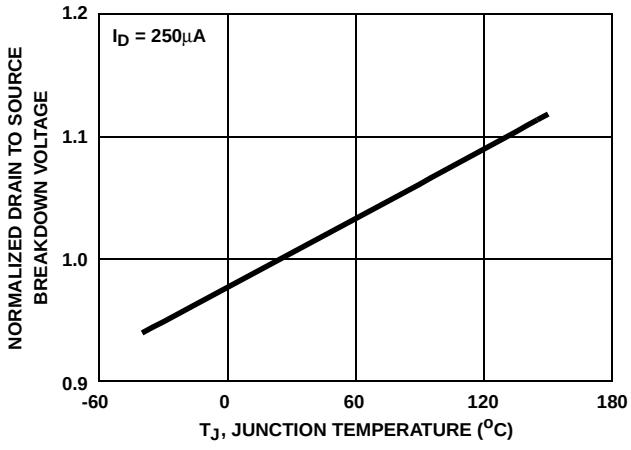



FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

## Typical Performance Curves (Continued)

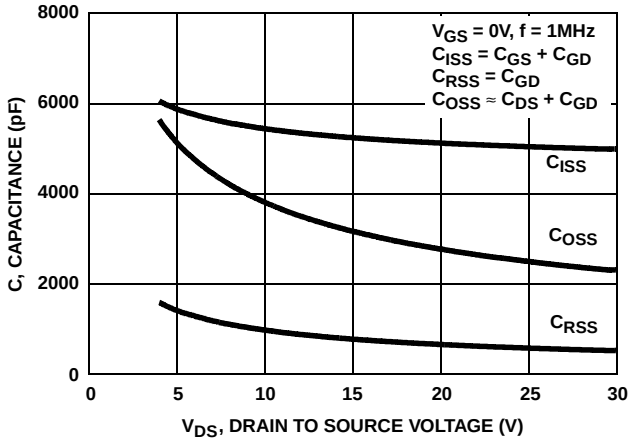
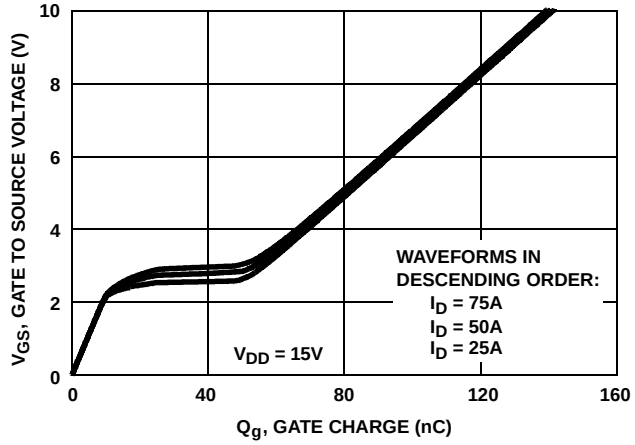



FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE




NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

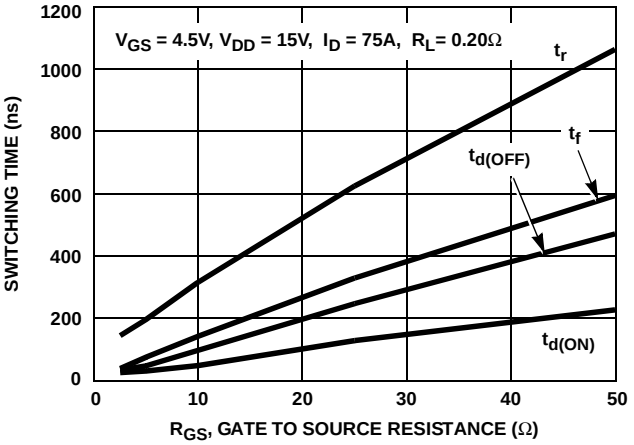



FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

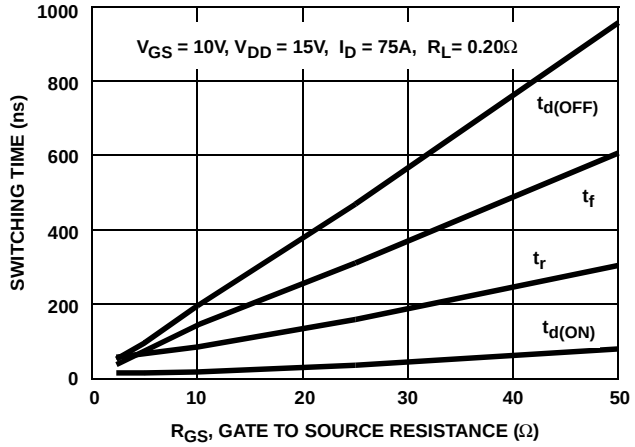



FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

## Test Circuits and Waveforms

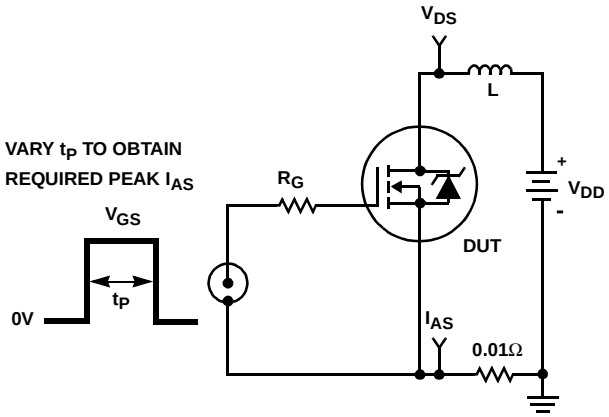



FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

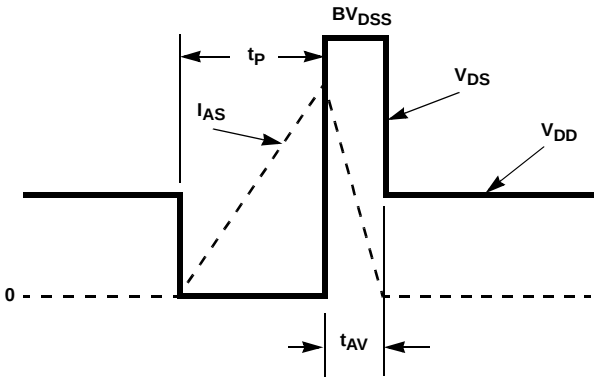



FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

## Test Circuits and Waveforms (Continued)

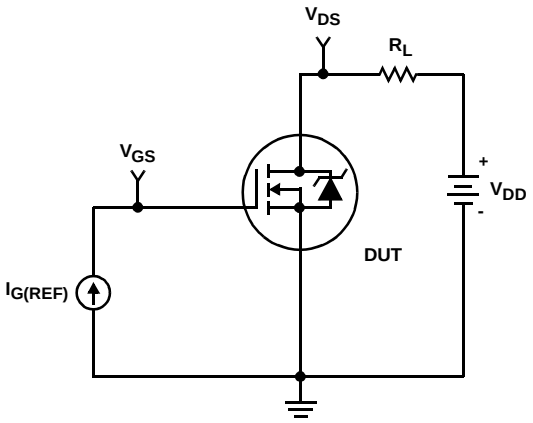



FIGURE 19. GATE CHARGE TEST CIRCUIT

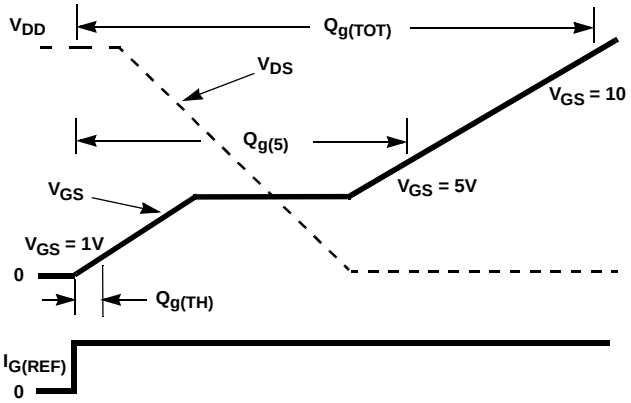



FIGURE 20. GATE CHARGE WAVEFORMS

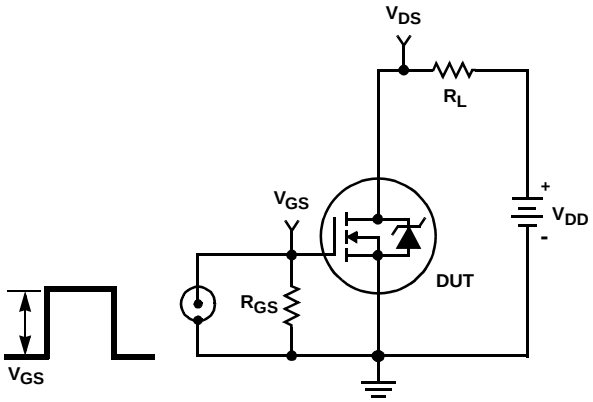



FIGURE 21. SWITCHING TIME TEST CIRCUIT

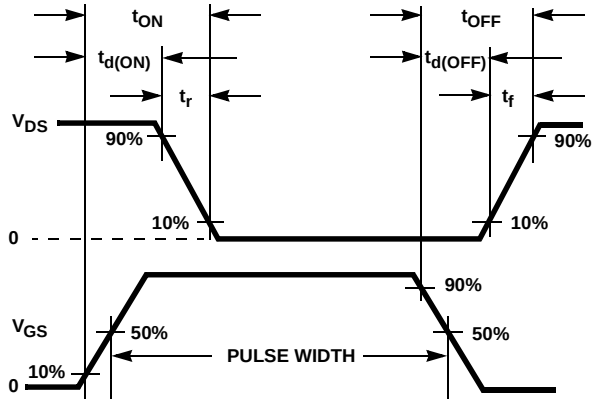



FIGURE 22. SWITCHING TIME WAVEFORM

## *PSPICE Electrical Model*

SUBCKT HUF76145 2 1 3 ; rev 6 Apr98

CA 12 8 7.75e-9
CB 15 14 7.45e-9
CIN 6 8 4.47e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 33.5
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

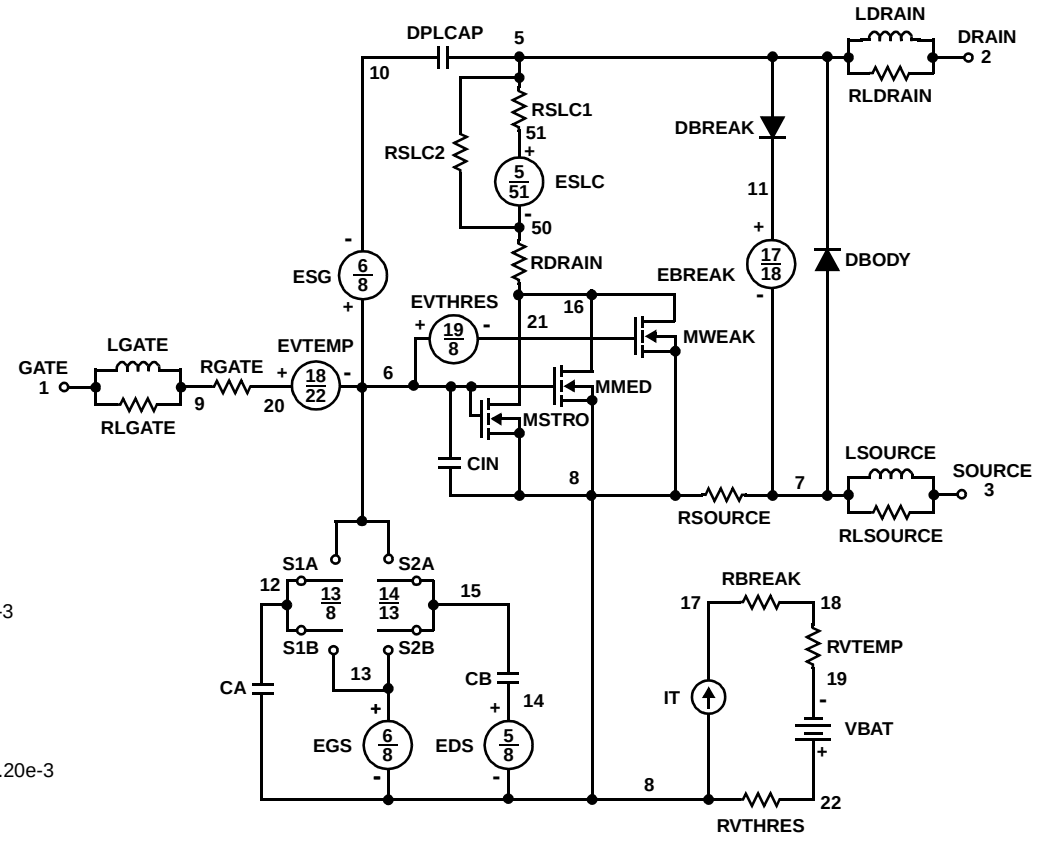
LDRAIN 2 5 1.00e-9
LGATE 1 9 2.60e-9
LSOURCE 3 7 1.10e-9
KGATE LSOURCE LGATE 0.0085

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 0.59e-3
RGATE 9 20 0.898
RLDRAIN 2 5 10
RLGATE 1 9 26
RLSOURCE 3 7 11
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 2.20e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1




.MODEL DBODYMOD D (IS = 6.01e-12 IKF = 20 RS = 1. 72e-3 TRS1 = 1.01e-3 TRS2 = 1.21e-6 CJO = 8.41e-9 TT = 4.84e-8 M = 0.45 )
.MODEL DBREAKMOD D (RS = 6.80e- 2TRS1 = 1.12e- 3TRS2 = 1.25e-6 )
.MODEL DPLCAPMOD D (CJO = 4.25e- 9IS = 1e-3 0N = 10 M = 0.61)
.MODEL MMEDMOD NMOS (VTO = 1.74 KP = 5.00 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.898)
.MODEL MSTROMOD NMOS (VTO = 2.10 KP = 245 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.48 KP = 0.10 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 8.98 RS= 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.01e- 3TC2 = 1.07e-7)
.MODEL RDRAINMOD RES (TC1 = 1.58e-2 TC2 = 3.76e-5)
.MODEL RSLCMOD RES (TC1 = 1.02e-4 TC2 = -1.13e-4)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -2.73e-3 TC2 = -1.01e-5)
.MODEL RVTEMPMOD RES (TC1 = -1.50e- 3TC2 = 1.25e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.00 VOFF= -1.50)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.50 VOFF= -6.00)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.00 VOFF= 0.45)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.45 VOFF= 0.00)

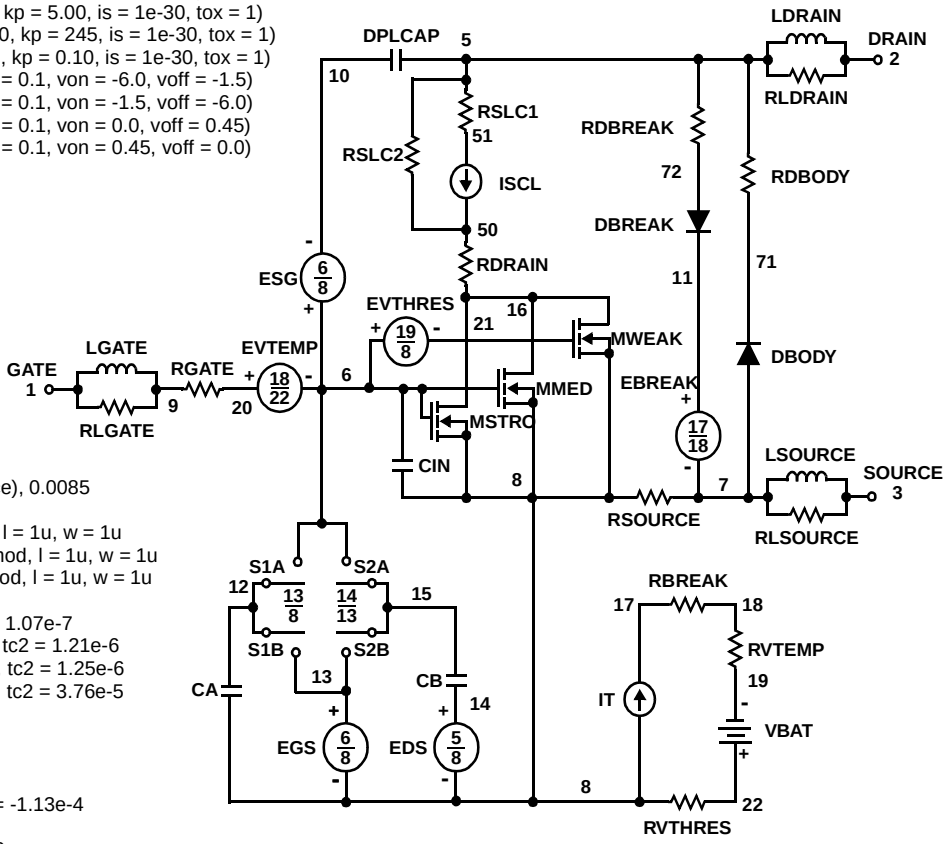
.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

## SABER Electrical Model

REV 6 Apr 1998

```
template huf76145 n2, n1, n3
electrical n2, n1, n3
{
var i iscl
d..model dbodymod =  (is = 6.01e-12, cjo = 8.41e-9, tt = 4.84e-8, m = 0.45)
d..model dbreakmod = ()
d..model dplcapmod =  (cjo = 4.25e-9, is = 1e-30, n = 10, m = 0.61)
m..model mmedmod = (type=_n, vto = 1.74, kp = 5.00, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.10, kp = 245, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.48, kp = 0.10, is = 1e-30, tox = 1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -6.0, voff = -1.5)
sw_vcsp..model s1bmod =  (ron = 1e-5, roff = 0.1, von = -1.5, voff = -6.0)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = 0.0, voff = 0.45)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = 0.45, voff = 0.0)

c.ca n12 n8 = 7.75e-9
c.cb n15 n14 = 7.45e-9
c.cin n6 n8 = 4.47e-9

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1.00e-9
l.lgate n1 n9 = 2.60e-9
l.lsource n3 n7 = 1.10e-9
k.k1 i(l.lgate) i(l.lsource) = l(l.lgate), l(l.lsource), 0.0085

m.mmed n16 n6 n8 n8 = model=mmedmod, l = 1u, w = 1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l = 1u, w = 1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l = 1u, w = 1u

res.rbreak n17 n18  = 1, tc1 = 1.01e-3, tc2 = 1.07e-7
res.rdbody n71 n5 = 1.72e-3, tc1 = 1.01e-3, tc2 = 1.21e-6
res.rdbreak n72 n5 = 6.80e-2, tc1 = 1.12e-3, tc2 = 1.25e-6
res.rdrain n50 n16  = 0.59e-3, tc1 = 1.58e-2, tc2 = 3.76e-5
res.rgate n9 n20 = 0.898
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 26
res.rlsource n3 n7 = 11
res.rslc1 n5 n51  = 1e-6, tc1 = 1.02e-4, tc2 = -1.13e-4
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 2.20e-3, tc1 = 0, tc2 = 0
res.rvtemp n18 n19  = 1, tc1 = -1.50e-3, tc2 = 1.25e-6
res.rvthres n22 n8  = 1, tc1 = -2.73e-3, tc2 = -1.01e-5

spe.ebreak n11 n7 n17 n18 = 33.50
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc = 1

equations {
i (n51->n50) + = iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/750))** 3))
}
}
```



## SPICE Thermal Model

REV Aug 2000

HUF76145T

CTHERM1 th 6 6.3e-3
CTHERM2 6 5 1.5e-2
CTHERM3 5 4 2.0e-2
CTHERM4 4 3 3.0e-2
CTHERM5 3 2 8.0e-2
CTHERM6 2 tl 1.5e-1

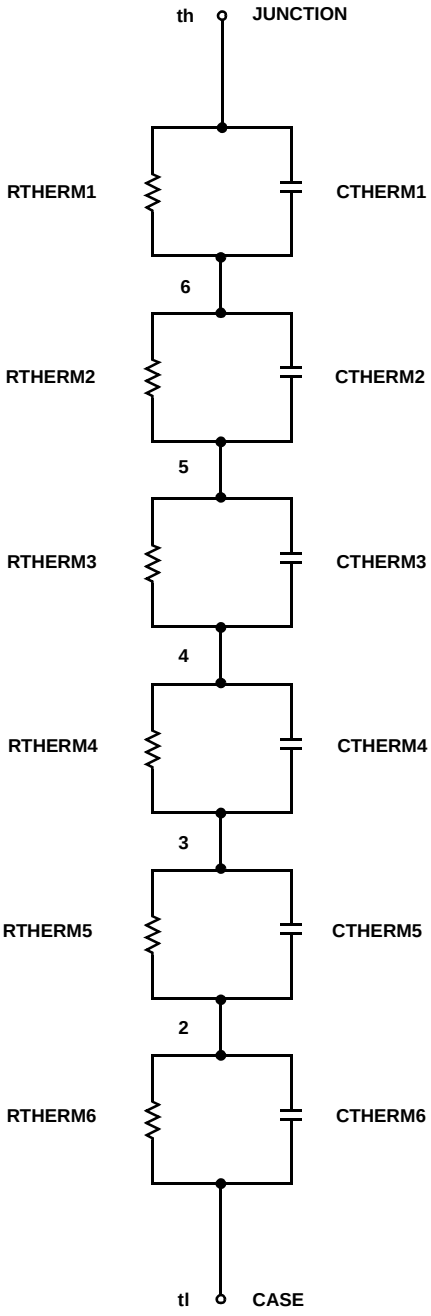
RTHERM1 th 6 5.0e-3
RTHERM2 6 5 1.8e-2
RTHERM3 5 4 5.0e-2
RTHERM4 4 3 8.5e-2
RTHERM5 3 2 1.0e-1
RTHERM6 2 tl 1.1e-1

## SABER Thermal Model

SABER thermal model HUF76145T

template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 6.3e-3
ctherm.ctherm2 6 5 = 1.5e-2
ctherm.ctherm3 5 4 = 2.0e-2
ctherm.ctherm4 4 3 = 3.0e-2
ctherm.ctherm5 3 2 = 8.0e-2
ctherm.ctherm6 2 tl = 1.5e-1

rtherm.rtherm1 th 6 = 5.0e-3
rtherm.rtherm2 6 5 = 1.8e-2
rtherm.rtherm3 5 4 = 5.0e-2
rtherm.rtherm4 4 3 = 8.5e-2
rtherm.rtherm5 3 2 = 1.0e-1
rtherm.rtherm6 2 tl = 1.1e-1
}



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| DOME™ | HiSeC™ | PowerTrench® | SuperSOT™-8 | |
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