PRELIMINARY

Integrated Circuit Systems, Inc.

ICS844251I-15
FEMTOCLOCKS™ CRYSTAL-TO-LVDS CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS844251I-15 is an Ethernet Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS844251I-15 uses an 18pF parallel resonant crystal over the range of 23.2MHz - 30MHz. For Ethernet applications, a 25MHz crystal is used. The device has excellent <1ps phase jitter performance, over the 1.875MHz - 20MHz integration range. The ICS844251I-15 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

FEATURES

- One Differential LVDS output
- Crystal oscillator interface, 18pF parallel resonant crystal (23.2MHz - 30MHz)
- Output frequency ranges: 116MHz - 150MHz and 580MHz - 750MHz
- VCO range: 580MHz - 750MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.46ps (typical)
- 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
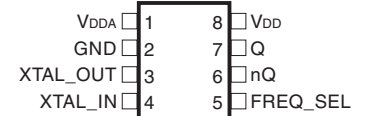- Available in both standard and lead-free RoHS-compliant packages

COMMON CONFIGURATION TABLE

Inputs					Output Frequency (MHz)
Crystal Frequency (MHz)	FREQ_SEL	M	N	Multiplication Value M/N	
25	1	25	1	25	625
26.667	1	25	1	25	666.67
25	0	25	5	5	125
26.667	0	25	5	5	133.33

BLOCK DIAGRAM
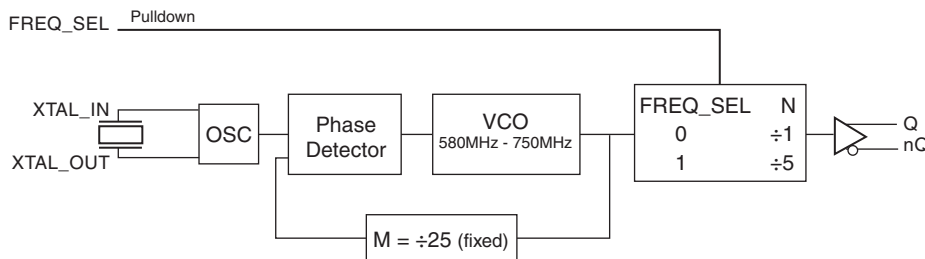
PIN ASSIGNMENT

ICS844251I-15
8-Lead TSSOP
4.4mm x 3.0mm x 0.925mm
package body
G Package
Top View

PRELIMINARY

Integrated
Circuit
Systems, Inc.

ICS844251I-15
FEMTOCLOCKS™ CRYSTAL-TO-LVDS
CLOCK GENERATOR

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	GND	Power		Power supply ground.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential clock outputs. LVDS interface levels.
8	V_{DD}	Power		Power supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Integrated Circuit Systems, Inc.

ICS844251I-15
FEMTOCLOCKS™ CRYSTAL-TO-LVDS
CLOCK GENERATOR

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} — 4.6V

Inputs, V_I — -0.5V to V_{DD} + 0.5 V

Outputs, I_O (LVDS)
 Continuous Current — 10mA
 Surge Current — 15mA

Package Thermal Impedance, θ_{JA} — 101.7°C/W (0 mps)

Storage Temperature, T_{STG} — -65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			100		mA
I_{DDA}	Analog Supply Current			8		mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			95		mA
I_{DDA}	Analog Supply Current			8		mA

TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{DD} = 3.3V	2		V_{DD} + 0.3	V
		V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	V_{DD} = 3.3V	-0.3		0.8	V
		V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA

PRELIMINARY

ICS844251I-15
FEMTOCLOCKS™ CRYSTAL-TO-LVDS
CLOCK GENERATOR

Integrated
Circuit
Systems, Inc.

TABLE 3D. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			400		mV
ΔV_{OD}	V_{OD} Magnitude Change			TBD		mV
V_{OS}	Offset Voltage			1.4		V
ΔV_{OS}	V_{OS} Magnitude Change			TBD		mV

TABLE 3E. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			400		mV
ΔV_{OD}	V_{OD} Magnitude Change			TBD		mV
V_{OS}	Offset Voltage			1.15		V
ΔV_{OS}	V_{OS} Magnitude Change			TBD		mV

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		23.2		30	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	f_SEL = 0	116		150	MHz
		f_SEL = 1	580		750	MHz
$t$jit(Ø)	RMS Phase Jitter (Random); NOTE 1	125MHz @ Integration Range: 1.875MHz - 20MHz		0.46		ps
		625MHz @ Integration Range: 1.875MHz - 20MHz		0.35		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		300		ps
odc	Output Duty Cycle			50		%

NOTE 1: Please refer to the Phase Noise Plots following this section.
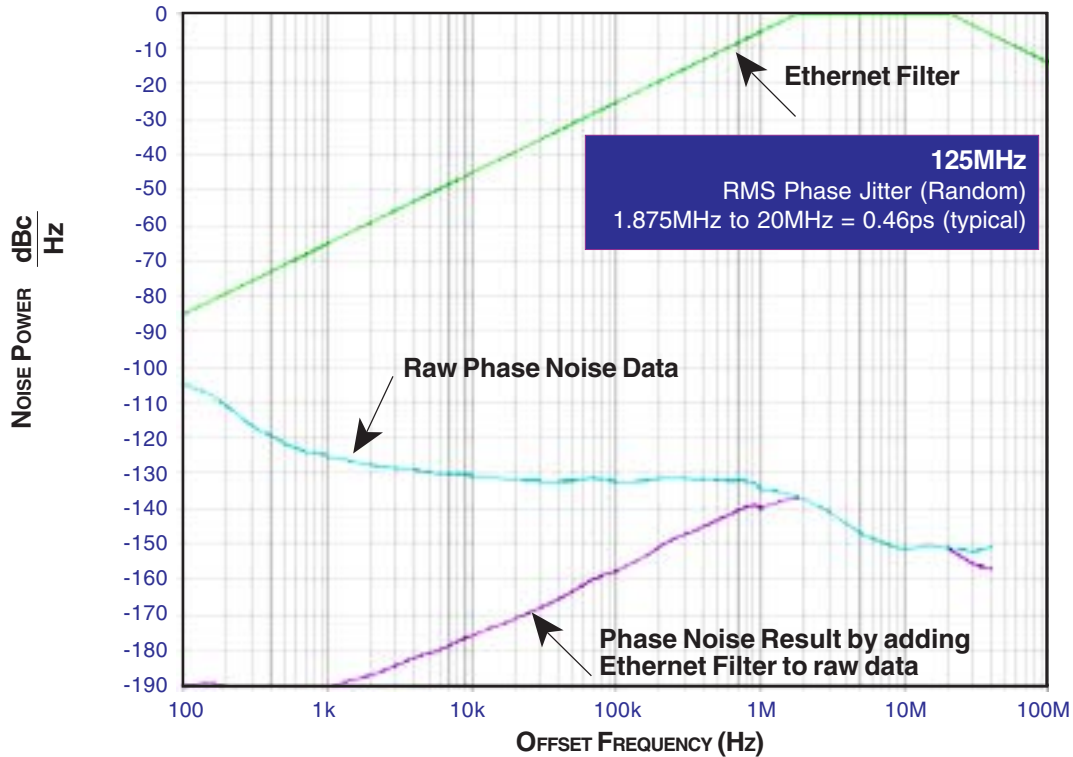
TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 2.5V \pm 5\%$, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	f_SEL = 0	116		150	MHz
		f_SEL = 1	580		750	MHz
$t$jit(Ø)	RMS Phase Jitter (Random); NOTE 1	125MHz @ Integration Range: 1.875MHz - 20MHz		0.46		ps
		625MHz @ Integration Range: 1.875MHz - 20MHz		0.35		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		300		ps
odc	Output Duty Cycle			50		%

NOTE 1: Please refer to the Phase Noise Plots following this section.

Integrated
Circuit
Systems, Inc.

TYPICAL PHASE NOISE AT 125MHz @ 3.3V

Ethernet Filter

125MHz
RMS Phase Jitter (Random)
1.875MHz to 20MHz = 0.46ps (typical)

Raw Phase Noise Data

Phase Noise Result by adding
Ethernet Filter to raw data

NOISE POWER $\frac{dBc}{Hz}$

OFFSET FREQUENCY (Hz)

TYPICAL PHASE NOISE AT 625MHz @ 3.3V

Ethernet Filter

625MHz
RMS Phase Jitter (Random)
1.875MHz to 20MHz = 0.35ps (typical)

Raw Phase Noise Data

Phase Noise Result by adding
Ethernet Filter to raw data

NOISE POWER $\frac{dBc}{Hz}$

OFFSET FREQUENCY (Hz)

PRELIMINARY

ICS844251I-15
FEMTOCLOCKS™ CRYSTAL-TO-LVDS
CLOCK GENERATOR

Integrated
Circuit
Systems, Inc.
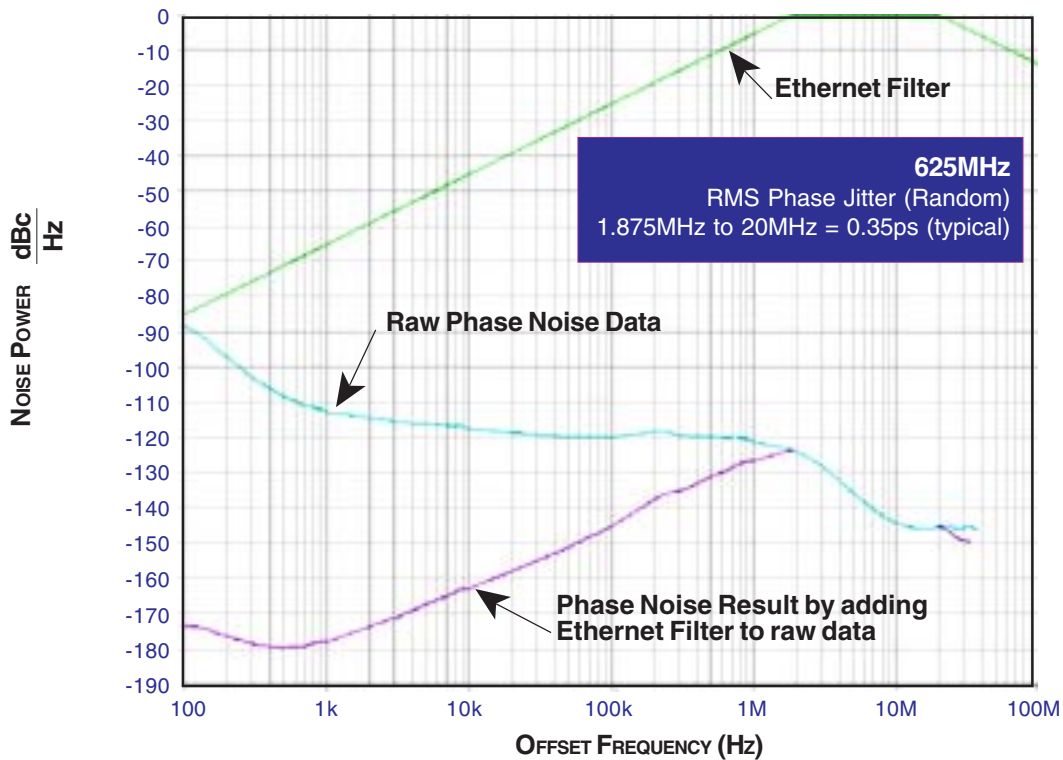
PARAMETER MEASUREMENT INFORMATION
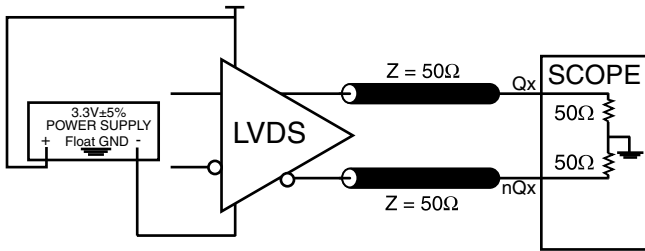
LVDS 3.3V OUTPUT LOAD AC TEST CIRCUIT
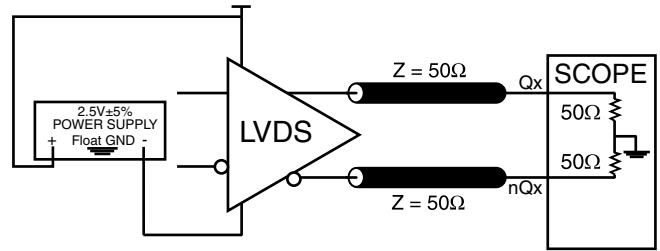
LVDS 2.5V OUTPUT LOAD AC TEST CIRCUIT
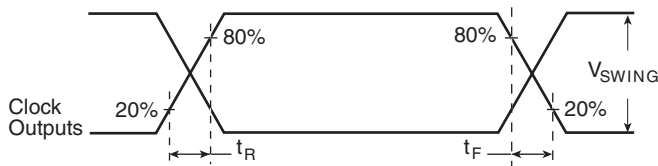
OUTPUT RISE/FALL TIME
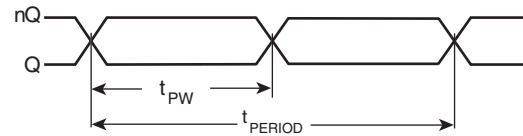
$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD
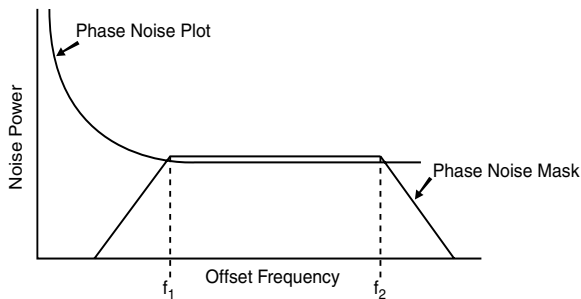
RMS Jitter = $\sqrt{\text{Area Under the Masked Phase Noise Plot}}$

RMS PHASE JITTER
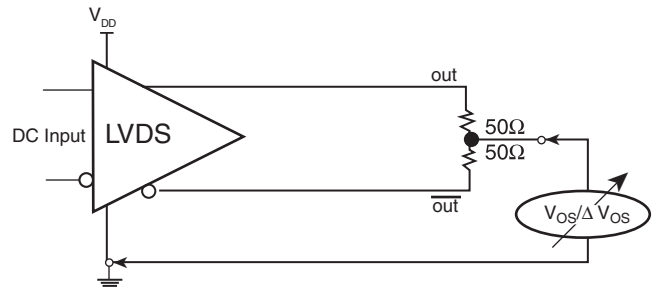
OFFSET VOLTAGE SETUP

DIFFERENTIAL OUTPUT VOLTAGE SETUP

Integrated
Circuit
Systems, Inc.
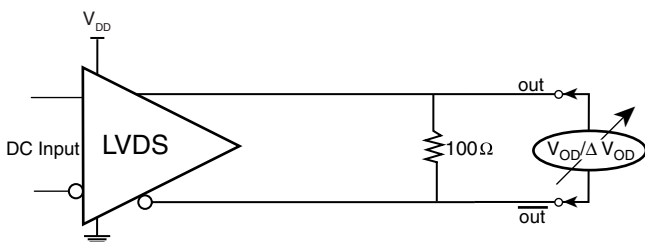
APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844251I-15 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin. The 10Ω resistor can also be replaced by a ferrite bead.
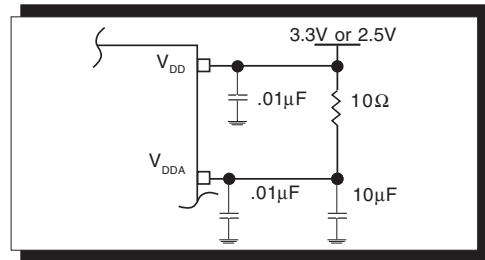
FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS844251I-15 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.
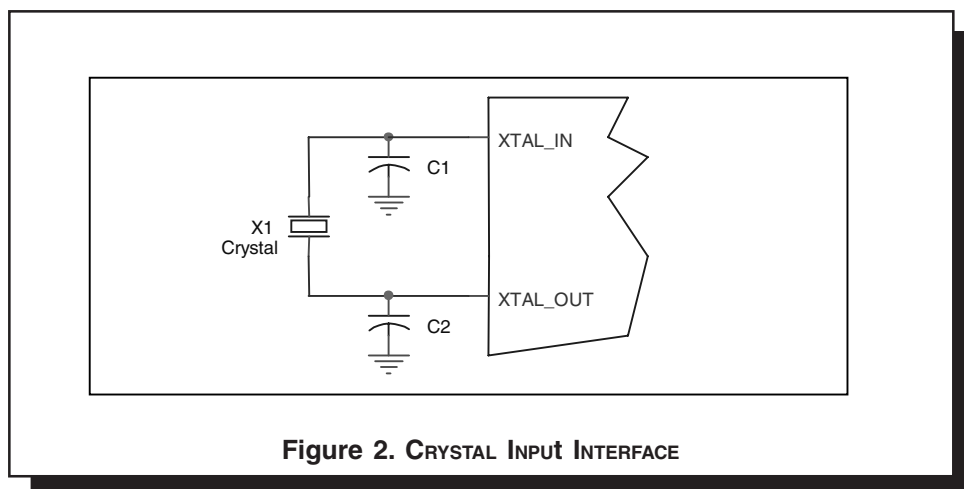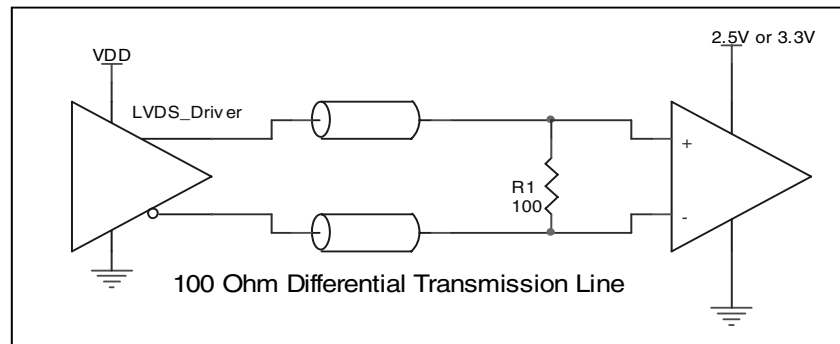

Figure 2. CRYSTAL INPUT INTERFACE

3.3V, 2.5V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

FIGURE 3. TYPICAL LVDS DRIVER TERMINATION

Integrated
Circuit
Systems, Inc.

RELIABILITY INFORMATION

TABLE 6. θ_{JA} **VS. AIR FLOW TABLE FOR 8 LEAD TSSOP**

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TRANSISTOR COUNT

The transistor count for ICS844251I-15 is: 2398

Integrated
Circuit
Systems, Inc.

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP
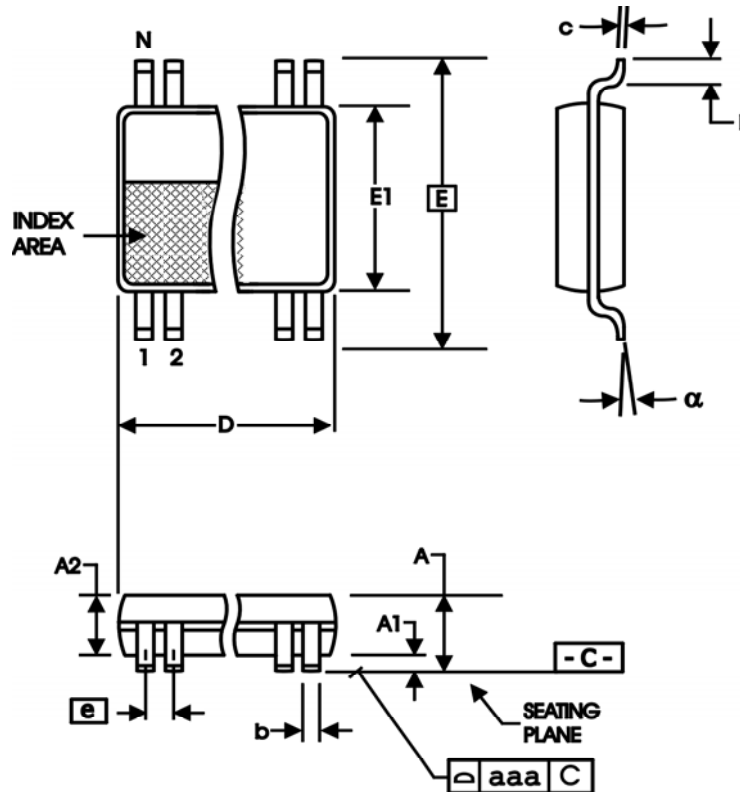
TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

PRELIMINARY

Integrated
Circuit
Systems, Inc.

ICS844251I-15
FEMTOCLOCKS™ CRYSTAL-TO-LVDS
CLOCK GENERATOR

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844251BGI-15	4BI15	8 Lead TSSOP	tube	-40°C to 85°C
ICS844251BGI-15T	4BI15	8 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS844251BGI-15LF	TBD	8 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS844251BGI-15LFT	TBD	8 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts thar are ordered with an "LF" suffix to the part number are the Pb-Free configuraiton and are RoHS compliant.