



HIGH-PERFORMANCE CMOS 9-BIT NON-INVERTING TRANSCEIVER

IDT74FCT863A/B

FEATURES:

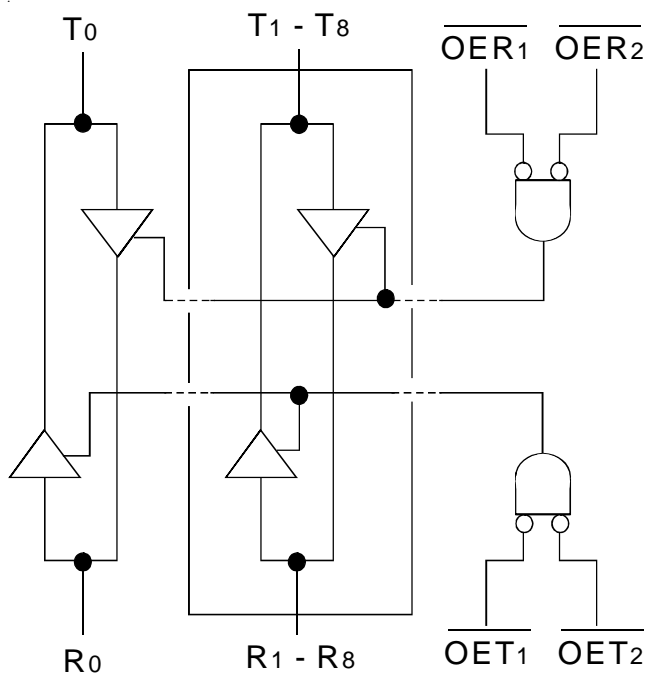
- Equivalent to AMD's Am29861-64 bipolar registers in pinout/function, speed, and output drive over full temperature and voltage supply extremes
- IDT74FCT863A equivalent to FAST™ speed
- IDT74FCT863B 25% faster than FAST
- High-speed symmetrical bidirectional transceivers
- $I_{OL} = 48\text{mA}$
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series ($5\mu\text{A}$ max.)
- Available in SOIC package

DESCRIPTION:

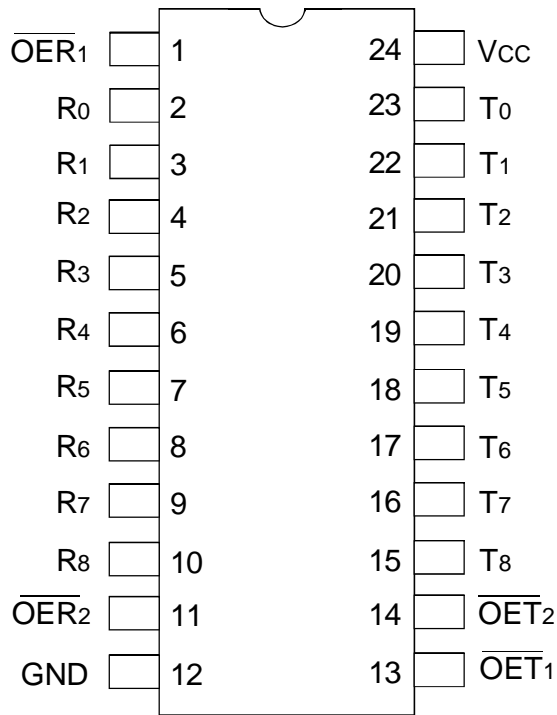
The IDT74FCT800 series is built using an advanced dual metal CMOS technology. The IDT74FCT863 9-bit transceivers have NAND-ed output enables for maximum control flexibility.

All of the IDT74FCT800 high-performance interface family is designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high-impedance state.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC}	V
T _A	Operating Temperature	0 to +70	°C
T _{BIAS}	Temperature under BIAS	-55 to +125	°C
T _{STG}	Storage Temperature	-55 to +125	°C
P _T	Power Dissipation	0.5	W
I _{OUT}	DC Output Current	120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Output and I/O terminals only.

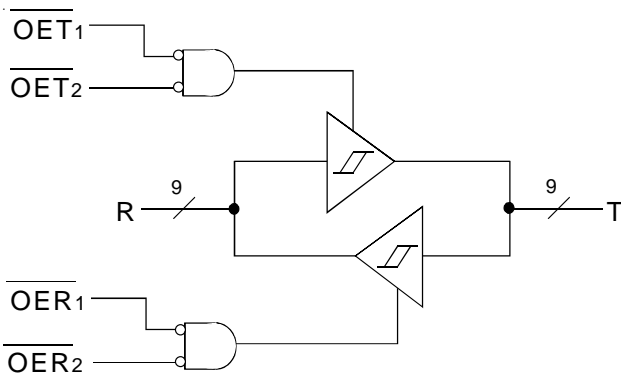
CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

- This parameter is measured at characterization but not tested.

LOGIC SYMBOL



PIN DESCRIPTION

Name	I/O	Description
\overline{OER}_i	I	When LOW in conjunction with \overline{OET}_i HIGH activates the RECEIVE mode.
\overline{OET}_i	I	When LOW in conjunction with \overline{OER}_i HIGH activates the TRANSMIT mode.
R _i	I/O	9-bit RECEIVE input/output.
T _i	I/O	9-bit TRANSMIT input/output.

FUNCTION TABLE⁽¹⁾

Inputs				Outputs		Function
\overline{OET}	\overline{OER}	R _i	T _i	R _i	T _i	
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	High Z

NOTE:

- H = HIGH
L = LOW
Z = High Impedance
X = Don't Care
N/A = Not Applicable

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Commercial: $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5.0V \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	5	μA
			$V_I = 2.7V$	—	—	5 ⁽⁴⁾	
I_{IL}	Input LOW Current (Except I/O pins)	$V_{CC} = \text{Max.}$	$V_I = 0.5V$	—	—	-5 ⁽⁴⁾	μA
			$V_I = GND$	—	—	-5	
I_{IH}	Input HIGH Current (I/O pins Only)	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	15	
			$V_I = 2.7V$	—	—	15 ⁽⁴⁾	
I_{IL}	Input LOW Current (I/O pins Only)	$V_{CC} = \text{Max.}$	$V_I = 0.5V$	—	—	-15 ⁽⁴⁾	
			$V_I = GND$	—	—	-15	
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = GND$		-75	-120	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$		V_{HC}	V_{CC}	—	V
		$V_{CC} = \text{Min.}$	$I_{OH} = -300\mu A$	V_{HC}	V_{CC}	—	
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -24mA$	2.4	4.3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$		—	GND	V_{LC}	V
		$V_{CC} = \text{Min.}$	$I_{OL} = 300\mu A$	—	GND	$V_{LC}^{(4)}$	
		$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 48mA^{(5)}$	—	0.3	0.5	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.
- These are maximum I_{OL} values per output, for 10 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 480mA. Derate I_{OL} for number of outputs exceeding 10 turned on simultaneously.

POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open \overline{OER} or $\overline{OET} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle \overline{OER} or $\overline{OET} = \text{GND}$ One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2	5	
		$V_{CC} = \text{Max.}$, Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle \overline{OER} or $\overline{OET} = \text{GND}$ Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.2	6.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5.2	14.5 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

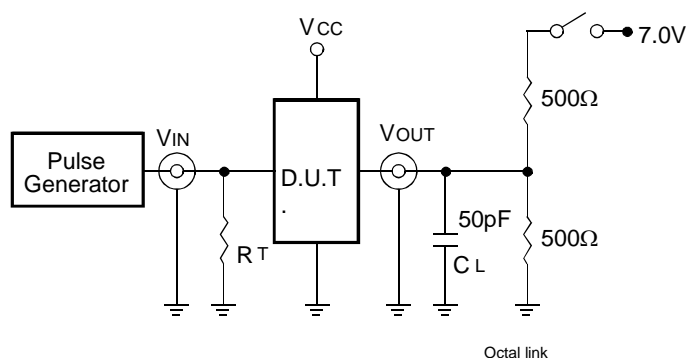
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	FCT863A		FCT863B		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
$t_{PLH/PHL}$	Propagation Delay R1 to T1 or T1 to R	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	8	1.5	6	ns
		$C_L = 300\text{pF}^{(3)}$ $R_L = 500\Omega$	1.5	15	1.5	13	
$t_{PZH/PZL}$	Output Enable Time \overline{OET} to T1 or \overline{OER} to R1	$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	12	1.5	8	ns
		$C_L = 300\text{pF}^{(3)}$ $R_L = 500\Omega$	1.5	20	1.5	15	
$t_{PHZ/PLZ}$	Output Disable Time \overline{OET} to T1 or \overline{OER} to R1	$C_L = 5\text{pF}^{(3)}$ $R_L = 500\Omega$	1.5	9	1.5	6	ns
		$C_L = 50\text{pF}$ $R_L = 500\Omega$	1.5	10	1.5	7	

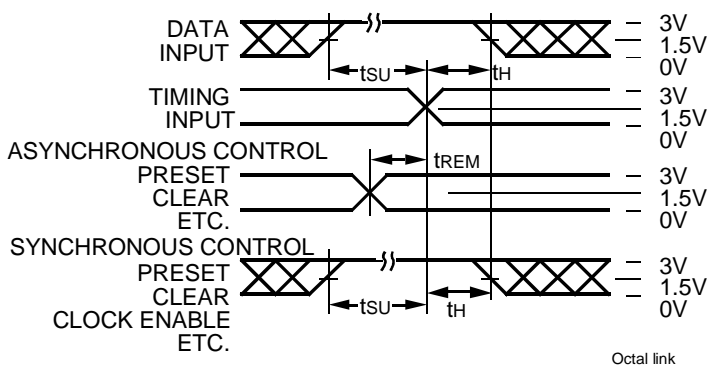
NOTES:

- See test circuits and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- This condition guaranteed but not tested.

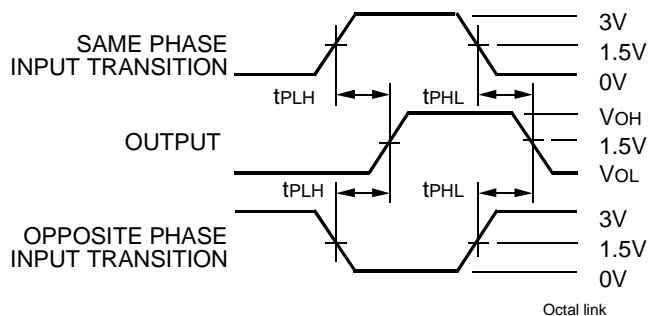
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



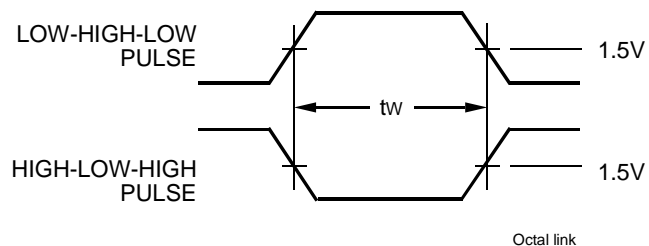
Propagation Delay

SWITCH POSITION

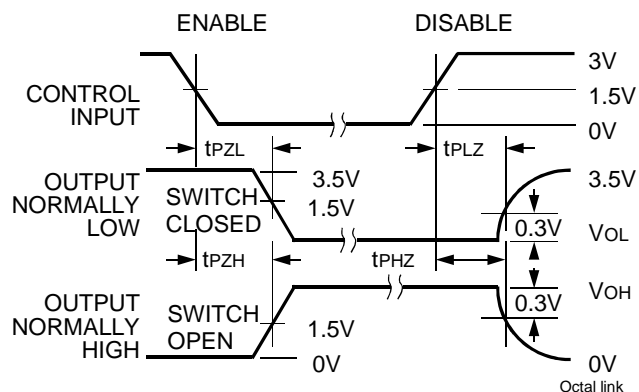
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width



Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_o \leq 50\Omega$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

