IN74LV138

3-to-8 line decoder/demultiplexer; inverting
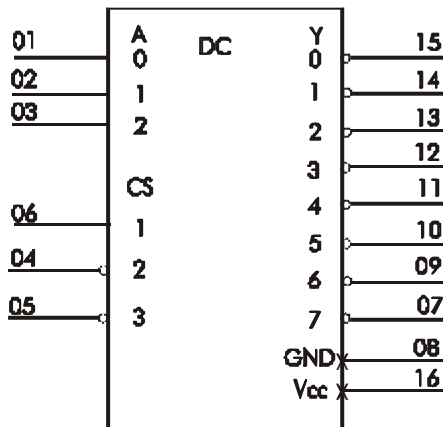
The IN74LV138 is a low-voltage Si-gate CMOS device and is pin and function compatible 74HCT138.

The 74LV138 accepts three binary weighted address inputs - (A_0, A_1, A_2) and when enabled, provide 8 - mutually exclusive active LOW outputs (Y_0 to Y_7).
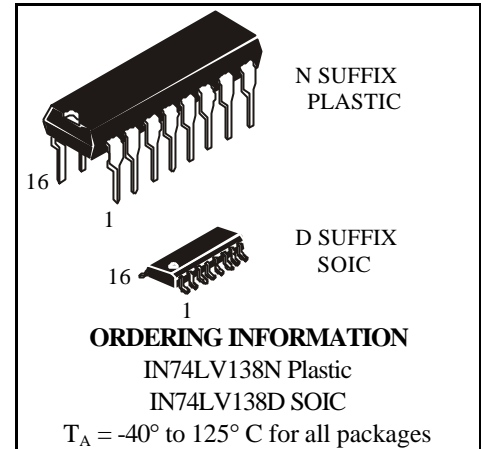
The "138" features three enable inputs: two active LOW ($\overline{CS_2}, \overline{CS_3}$ and one active HIGH (CS_1). Every output will be HIGH untess CS_2, and CS_3 are LOW and CS_1 is HIGH.

- Optimized for Low Voltage applications: 1.2 to 3.6 V
- Demultiplexing capability
- Multiple input enabte for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
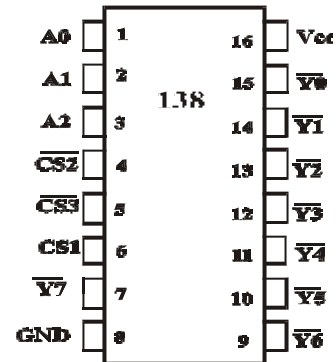- Output capability: standard

N SUFFIX
PLASTIC

D SUFFIX
SOIC

ORDERING INFORMATION
IN74LV138N Plastic
IN74LV138D SOIC
T_A = -40° to 125° C for all packages

PIN ASSIGNMENT

A0	1	16	Vcc
A1	2	15	$\overline{Y0}$
A2	3	14	$\overline{Y1}$
$\overline{CS2}$	4	13	$\overline{Y2}$
$\overline{CS3}$	5	12	$\overline{Y3}$
CS1	6	11	$\overline{Y4}$
$\overline{Y7}$	7	10	$\overline{Y5}$
GND	8	9	$\overline{Y6}$

138

LOGIC DIAGRAM

PIN 16 = V_{CC}
PIN 8 = GND

FUNCTION TABLE

Inputs			Outputs
CS1 CS2 CS3		A2 A1 A0	Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
X X H		X X X	H H H H H H H H
X H X		X X X	H H H H H H H H
L X X		X X X	H H H H H H H H
H L L		L L L	L H H H H H H H
H L L		L L H	H L H H H H H H
H L L		L H L	H H L H H H H H
H L L		L H H	H H H L H H H H
H L L		H L L	H H H H L H H H
H L L		H L H	H H H H H L H H
H L L		H H L	H H H H H H L H
H L L		H H H	H H H H H H H L

H = high level (steady state)
L = low level (steady state)
X = don't care

INTEGRAL

MAXIMUM RATINGS*

Symbol	Parameter	Value	Conditions	Unit
V_{CC}	DC supply voltage	-0.5 to +7.0		V
I_{IK}	DC input diode current	±20	$V_I < -0.5$ or $V_I >$ Vcc+0.5V	mA
I_{OK}	DC output diode current	±50	$V_O < -0.5$ or $V_O >$ Vcc+0.5V	mA
I_O	DC output source or sink current	±25	-0.5Â<Vo<Vcc+0.5B	mA
I_{CC}	DC V_{CC} or GND current for types with standard outputs	±50		mA
Tstg	Storage Temperature	-65 to +150		°C
P_D	Power Dissipation per package Plastic DIP+ SOIC Package+	750 500		mW
T_L	Lead temperature, 1.5 mm from Case for 4 seconds (Plastic DIP), 0.3 mm (SOIC Package)	260		°C

*
  Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C

SOIC Package: : - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC supply voltage		1.0	5.5	V
V_{IN},	DC input voltage,		0	V_{CC}	V
V_O	DC output voltage		0	V_{CC}	V
T_A	Operating ambient temperature range in free air		-40	+125	°C
t_r, t_f	Input rise and fall times except for Schmitt-trigger inputs	Vcc= 1.0 ? 2.0Â Vcc= 2.0 ? 2.7Â Vcc= 2.7 ? 3.6Â Vcc= 3.6 ? 5.5Â	0 0 0	500 200 100 50	ns/B

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC}, Â	Guaranteed Limit						Unit
				25°C		î ò -40°C to 85°C		î ò -40°C to 125°C		
				min	max	min	max	min	max	
V_{IH}	High-level input voltage		1.2 2.0 2.7 to 3.6 4.5 to 5.5	0.9 1.4 2.0 0.7 Vcc	- - - -	0.9 1.4 2.0 0.7 Vcc	- - - -	0.9 1.4 2.0 0.7 Vcc	- - - -	Â
V_{IL}	Low -level input voltage		1.2 2.0 2.7 to 3.6 4.5 to 5.5	- - - -	0.3 0.6 0.8 0.3 Vcc	- - - -	0.3 0.6 0.8 0.3 Vcc	- - - -	0.3 0.6 0.8 0.3 Vcc	Â
V_{OH}	High-level output voltage	$-I_0=100\mu A$ V_{IH} or V_{IL}	1.2 2.0 2.7 3.0 3.6 4.5 5.5	- 1.85 2.55 2.85 3.45 4.35 5.35	- - - - - - -	- 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	- 1.8 2.5 2.8 3.4 4.3 5.3	- - - - - - -	Â
		V_{IH} or V_{IL} $-I_{O=}6.0$ mA $-I_{O=}12.0$ mA	3.0 4.5	2.48 3.70	- -	2.40 3.60	- -	2.20 3.50	- -	B
V_{OL}	Low-level output voltage	V_{IH} or V_{IL} $I_0=100\mu A$	1.2 2.0 3.0	- - - -	0.15 0.15 0.15	- - - -	0.2 0.2 0.2	- - - -	0.2 0.2 0.2	B
		V_{IH} or V_{IL} $I_{O=}6.0$ mA $I_{O=}12.0$ mA	3.0 4.5	- -	0.33 0.40	- -	0.40 0.55	- -	0.50 0.65	B
I_I	Input leakage current	V_{CC} or GND	5.5	-	±0.1	-	±1.0	-	±1.0	ì êÀ
I_{CC}	Quiescent supply current	V_{CC} or GND $I_O=0$	5.5	-	8.0	-	80	-	160	ì êÀ

AC ELECTRICAL CHARACTERISTICS (C$_L$=50 pF, t$_{LH}$ = t$_{HL}$ = 2.5 nc, V$_{IL}$=0B, V$_{IH}$=V$_{CC}$)

Symbol	Parameter	V$_{CC}$ V	Guaranteed Limit						Unit
			25°C		î ò -40°C to 85°C		î ò -40°C to 125°C		
			min	max	min	max	min	max	
t$_{PLH}$, t$_{PHL}$	Propagation delay, input A to output Y (Figures 1)	1.2 2.0 2.7 3.0 4.5	-	150 33 23 19 14	-	150 36 26 21 16	-	180 44 33 26 20	ns
t$_{PLH}$, t$_{PHL}$	Propagation delay , CS1 to output Y (Figures 2)	1.2 2.0 2.7 3.0 4.5	-	170 35 26 21 17	-	170 39 29 23 19	-	200 49 36 29 24	ns
t$_{PLH}$, t$_{PHL}$	Output transition time, CS2 or CS3 to output Y (Figures 3)		-	170 35 26 21 17	-	170 39 29 23 19	-	200 49 36 29 24	ns
C$_{IN}$	Input capacitance	5.0 Ò=+25$^{\text{î}}$Ñ		7.0					pF

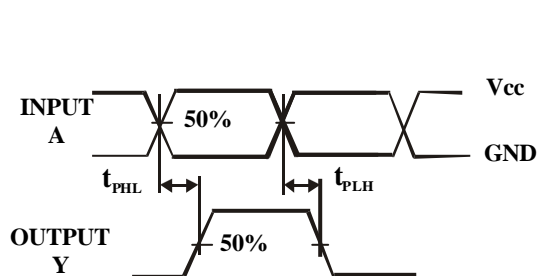|			
	Power dissipation capacitance (per enabled output)	Typical @25°C,V$_{CC}$=5.5 V	
C$_{PD}$	Used to determine the no-load dynamic power consumption: P$_D$=C$_{PD}$V$_{CC}$^{2}f+I$_{CC}$V$_{CC}$	90	pF

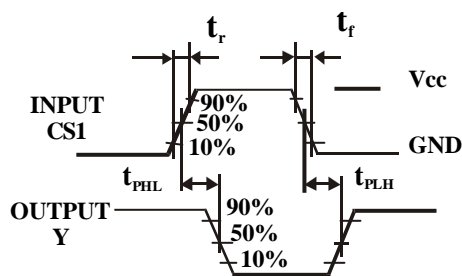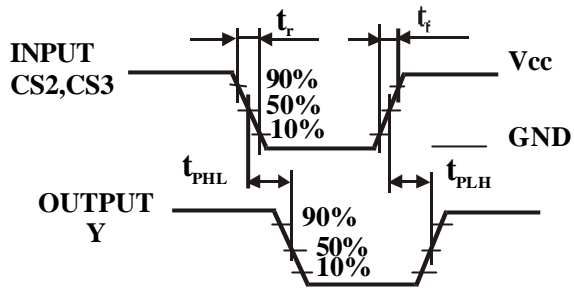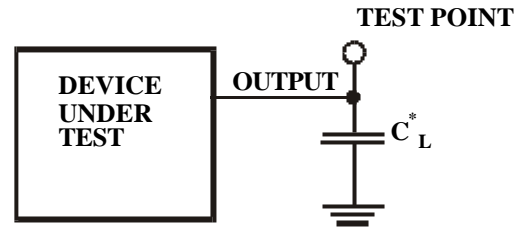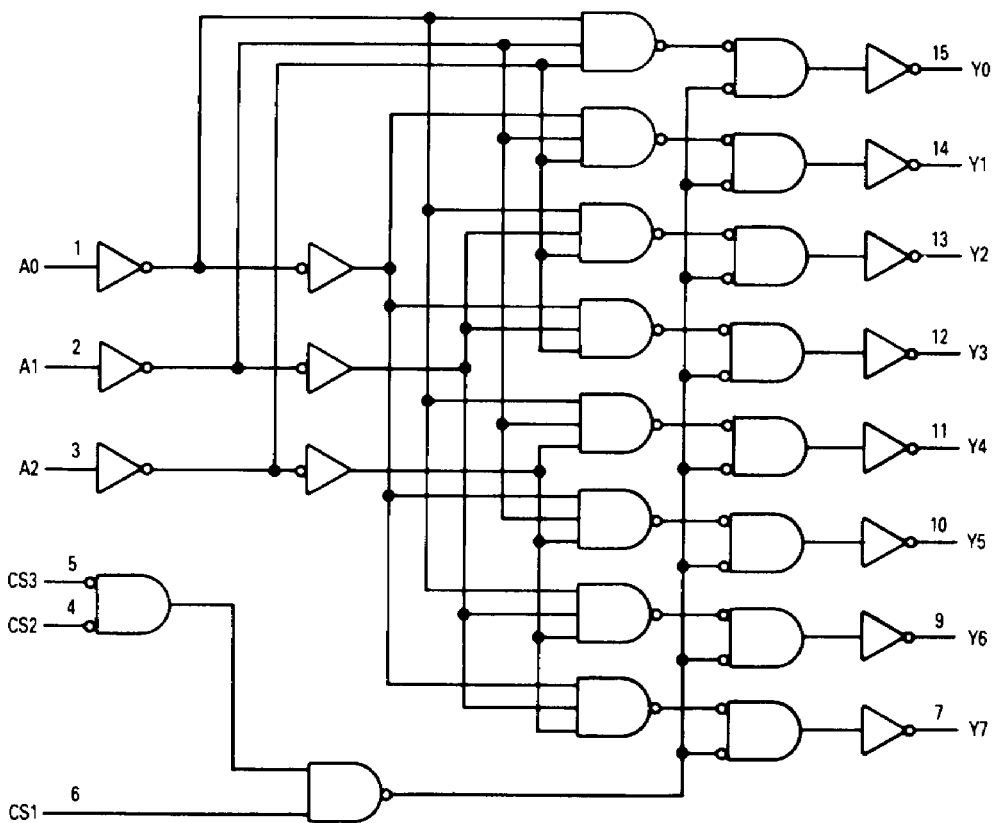**Figure 1. Switching Waveforms**   **Figure 2. Switching Waveforms**

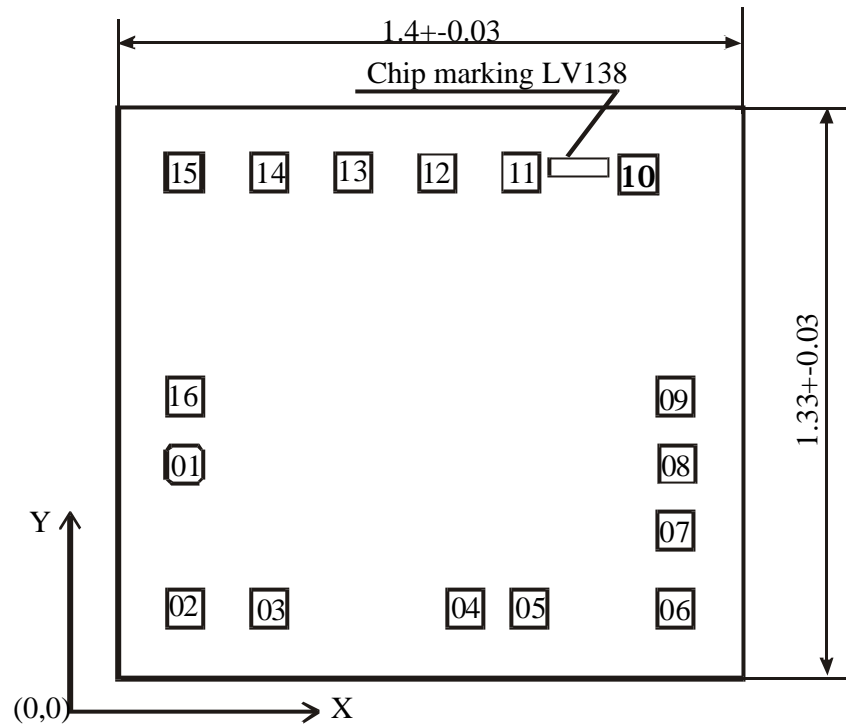Figure 3. Switching Waveforms

* Includes all prode and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM

CHIP PAD DIAGRAM

Location of marking (mm): left lower corner x = 0.950, y = 1.175;
Thickness of chip: 0.46 ± 0.02 mm

PAD   LOCATION

Pad No.	Pad Name	X	Y	Pad size (mm)
01	AO	0.118	0.429	0.100 x 0.100
02	A1	0.118	0.115	0.100 x 0.100
03	A2	0.395	0.115	0.100 x 0.100
04	CS2	0.709	0.115	0.100 x 0.100
05	CS3	0.877	0.115	0.100 x 0.100
06	CS1	1.191	0.115	0.100 x 0.100
07	Y7	1.191	0.283	0.100 x 0.100
08	GND	1.191	0.441	0.100 x 0.100
09	Y6	1.191	0.599	0.100 x 0.100
10	Y5	1.084	1.111	0.100 x 0.100
11	Y4	0.798	1.111	0.100 x 0.100
12	Y3	0.640	1.111	0.100 x 0.100
13	Y2	0472	1.111	0.100 x 0.100
14	Y1	0.314	1.111	0.100 x 0.100
15	Y0	0.131	1.111	0.100 x 0.100
16	Vcc	0.118	0.597	0.100 x 0.100

∗ Note: Pad location is given as per passivation layer

INTEGRAL