

IN74LV139

Dual 2-to-4 line decoder/demultiplexer; inverting

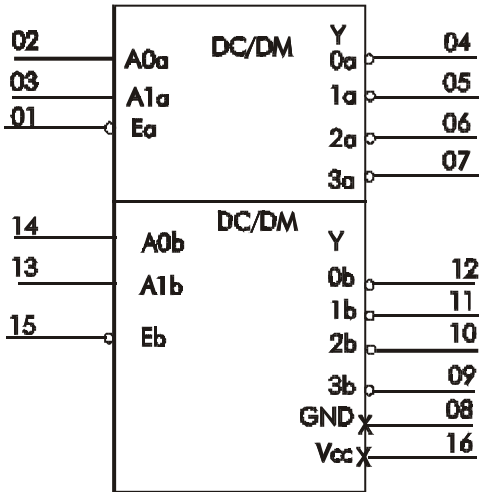
The IN74LV139 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HCT139.

The IN74LV139 is dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A0a,A0b and A1a,A1b) and providing four mutually exclusive active LOW outputs (nY0 to nY3). Each decoder has an active LOW enable input (nE)

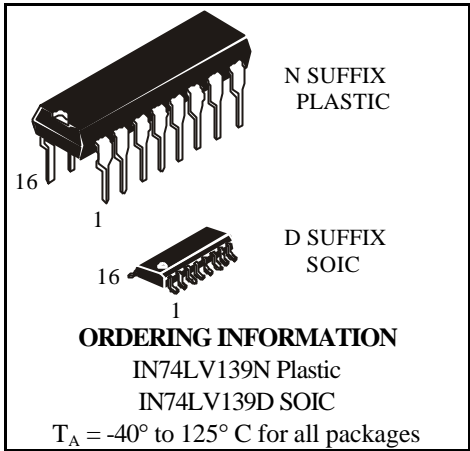
When nE is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

- Optimized for Low Voltage applications: 1.2 to 3.6 V
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output capability: standard

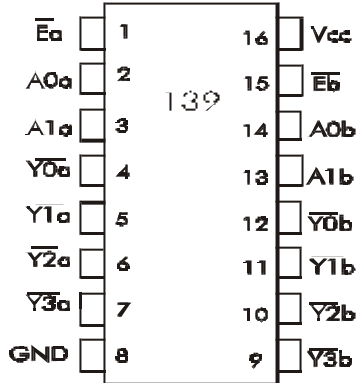
LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND



PIN ASSIGNMENT



FUNCTION TABLE

Inputs			Outputs			
E	A1	A0	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level (steady state)
L = low level (steady state)
X = don't care

MAXIMUM RATINGS *

Symbol	Parameter	Value	Conditions	Unit
V _{CC}	DC supply voltage	-0.5 to +7.0		V
I _{IK}	DC input diode current	±20	V _I < - 0.5 or V _I > V _{CC} +0.5V	mA
I _{OK}	DC output diode current	±50	V _O < - 0.5 or V _O > V _{CC} +0.5V	mA
I _O	DC output source or sink current	±25	-0.5V < V _O < V _{CC} +0.5V	mA
I _{CC}	DC V _{CC} or GND current for types with standard outputs	±50		mA
T _{stg}	Storage Temperature	-65 to +150		°C
P _D	Power Dissipation per package Plastic DIP+ SOIC Package+	750 500		mW
T _L	Lead temperature, 1.5 mm from Case for 4 seconds (Plastic DIP), 0.3 mm (SOIC Package)	260		°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
 +Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
 SOIC Package: - 8 mW/°C from 70° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC supply voltage	1.2	5.5	V
V _I	DC input voltage,	0	V _{CC}	V
V _O	DC output voltage	0	V _{CC}	V
T _A	Operating ambient temperature range in free air	-40	+125	°C
t _r , t _f	Input rise and fall times except for Schmitt-trigger inputs	V _{CC} = 1.0 ? 2.0V 0 0 0	500 200 100 50	ns/B

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} , Â	Guaranteed Limit						Unit
				25°C		î ð -40°C to 85°C		î ð -40°C to 125°C		
				min	max	min	max	min	max	
V _{IH}	High-level input voltage		1.2	0.9	-	0.9	-	0.9	-	Â
			2.0	1.4	-	1.4	-	1.4	-	
			2.7 to 3.6	2.0	-	2.0	-	2.0	-	
			4.5 to 5.5	0.7 V _{CC}	-	0.7 V _{CC}	-	0.7 V _{CC}	-	
V _{IL}	Low-level input voltage		1.2	-	0.3	-	0.3	-	0.3	Â
			2.0	-	0.6	-	0.6	-	0.6	
			2.7 to 3.6	-	0.8	-	0.8	-	0.8	
			4.5 to 5.5	-	0.3 V _{CC}	-	0.3 V _{CC}	-	0.3 V _{CC}	
V _{OH}	High-level output voltage	-I _O =100µA V _{IH} or V _{IL}	1.2	-	-	-	-	-	-	Â
			2.0	1.85	-	1.8	-	1.8	-	
			2.7	2.55	-	2.5	-	2.5	-	
			3.0	2.85	-	2.8	-	2.8	-	
			3.6	3.45	-	3.4	-	3.4	-	
			4.5	4.35	-	4.3	-	4.3	-	
	V _{IH} or V _{IL} -I _O =6.0 mA -I _O =12.0 mA	3.0	2.48	-	2.40	-	2.20	-	B	
		4.5	3.70	-	3.60	-	3.50	-		
V _{OL}	Low-level output voltage	V _{IH} or V _{IL} I _O =100µA	1.2	-	0.15	-	0.2	-	0.2	B
			2.0	-	0.15	-	0.2	-	0.2	
			3.0	-	0.15	-	0.2	-	0.2	
			-	-	-	-	-	-	-	
V _{IH} or V _{IL} I _O =6.0 mA I _O =12.0 mA	3.0	-	0.33	-	0.40	-	0.50	B		
	4.5	-	0.40	-	0.55	-	0.65			
I _I	Input leakage current	V _{CC} or GND	5.5	-	±0.1	-	±1.0	-	±1.0	î êÀ
I _{CC}	Quiescent supply current	V _{CC} or GND I _O =0	5.5	-	8.0	-	80	-	160	î êÀ

AC ELECTRICAL CHARACTERISTICS ($C_L=50$ pF, $t_{LH} = t_{HL} = 2.5$ ns, $V_{IL}=0B$, $V_{IH}=V_{CC}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit						Unit
			25°C		-40°C to 85°C		-40°C to 125°C		
			min	max	min	max	min	max	
t _{PLH} , t _{PHL}	Propagation delay, input A to output Y (Figures 1)	1.2	-	140	-	140	-	140	ns
		2.0		27		31		39	
		2.7		20		23		29	
		3.0		16		18		23	
		4.5		13		15		19	
t _{PLH} , t _{PHL}	Propagation delay, E to output Y (Figures 2)	1.2	-	120	-	120	-	120	ns
		2.0		22		27		34	
		2.7		16		20		25	
		3.0		13		16		20	
		4.5		10		13		16	
C _I	Input capacitance	5.0 @+25°C		7.0					pF

C _{PD}	Power dissipation capacitance (per enabled output)	Typical @25°C, V _{CC} =5.5 V		pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	84*		

* - Power dissipation capacitance per multiplexer

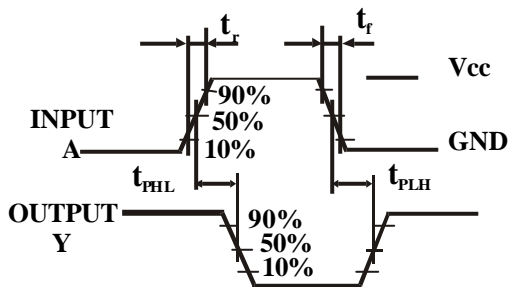


Figure 1. Switching Waveforms

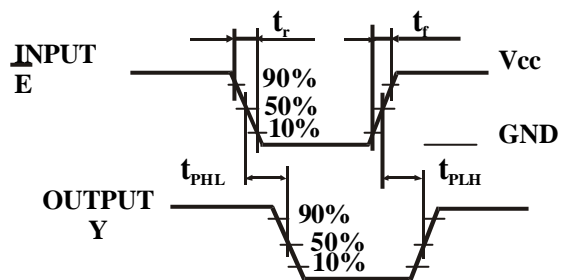


Figure 2. Switching Waveforms

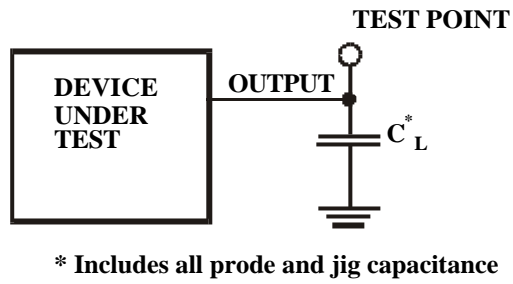
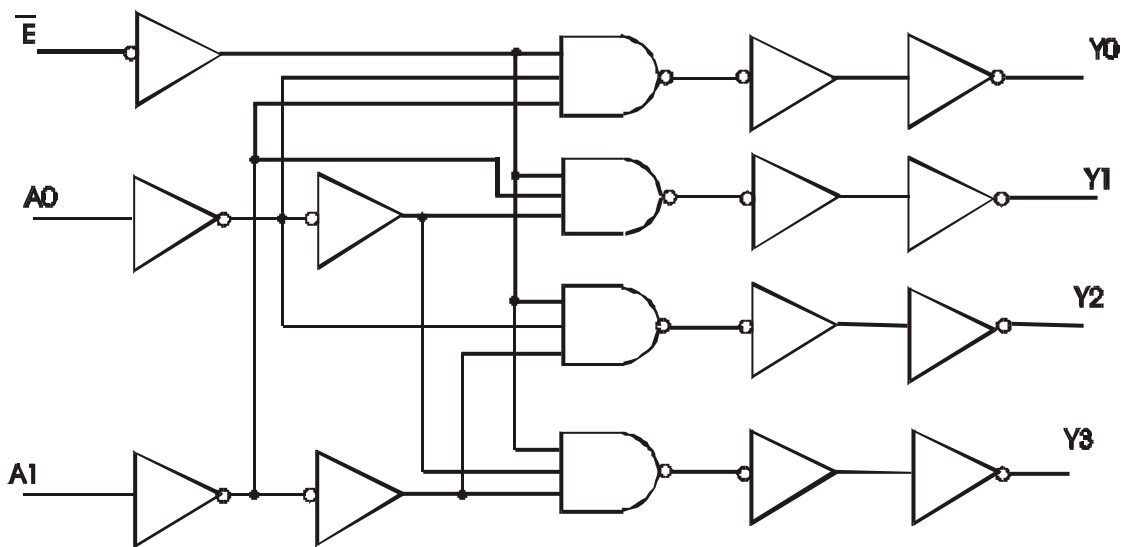


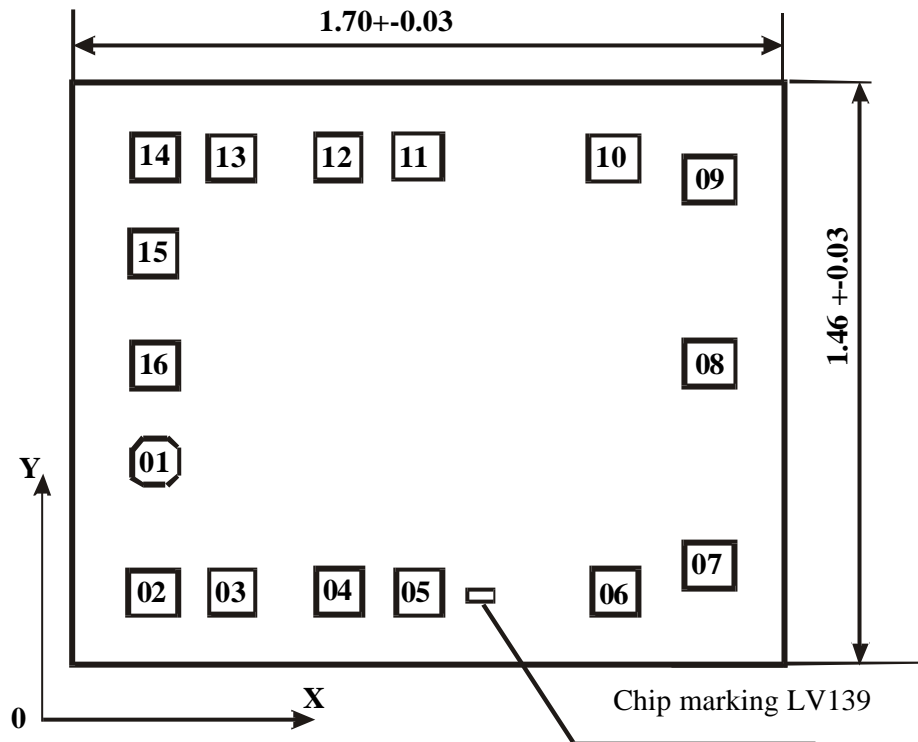
Figure 3. Test Circuit

EXPANDED LOGIC DIAGRAM

(1/2 of Device)



CHIP PAD DIAGRAM



Location of marking (mm): left lower corner $x = 0.950$, $y = 0.130$;

Thickness of chip: 0.46 ± 0.02 mm

PAD LOCATION

Pad No.	Pad Name	X	Y	Pad size (mm)
01	$\bar{E}a$	0.1245	0.4625	0.100 x 0.100
02	A0a	0.1245	0.1290	0.100 x 0.100
03	A1a	0.2920	0.1290	0.100 x 0.100
04	Y0a	0.5480	0.1290	0.100 x 0.100
05	Y1a	0.7520	0.1290	0.100 x 0.100
06	Y2a	1.2830	0.1290	0.100 x 0.100
07	Y3a	1.4845	0.1845	0.100 x 0.100
08	<u>GND</u>	1.4840	0.6770	0.100 x 0.100
09	Y3b	1.4845	1.1720	0.100 x 0.100
10	Y2b	1.2830	1.2265	0.100 x 0.100
11	Y1b	0.7520	1.2265	0.100 x 0.100
12	Y0b	0.5480	1.2265	0.100 x 0.100
13	A1b	0.2920	1.2265	0.100 x 0.100
14	A0b	0.1245	1.2265	0.100 x 0.100
15	Eb	0.1245	0.8930	0.100 x 0.100
16	Vcc	0.1245	0.6650	0.100 x 0.100

* Note: Pad location is given as per passivation layer