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ISD-300A1
High Speed USB to ATA ASIC

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Document Revision History

Title	ISD-300A1 ASIC Datasheet
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Initial Revision #	0.8
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Revision	Date	Comments
0.8	January 16, 2001	Initial revision
0.82	March 28, 2001	Grammar edits.
0.83	April 18, 2001	Identified I²C limitations
0.9	June 19, 2001	Rolled version to release draft
1.0	July 10, 2001	Minor corrections, rolled to final release draft.
1.01	Aug 1, 2001	Added text to Figure 5 noting 45Ω impedance on D+ and D- for High-speed operation.
1.02	October 19, 2001	Initial conversion to Cypress document

Table 1 –Document Revision History

Pin Information

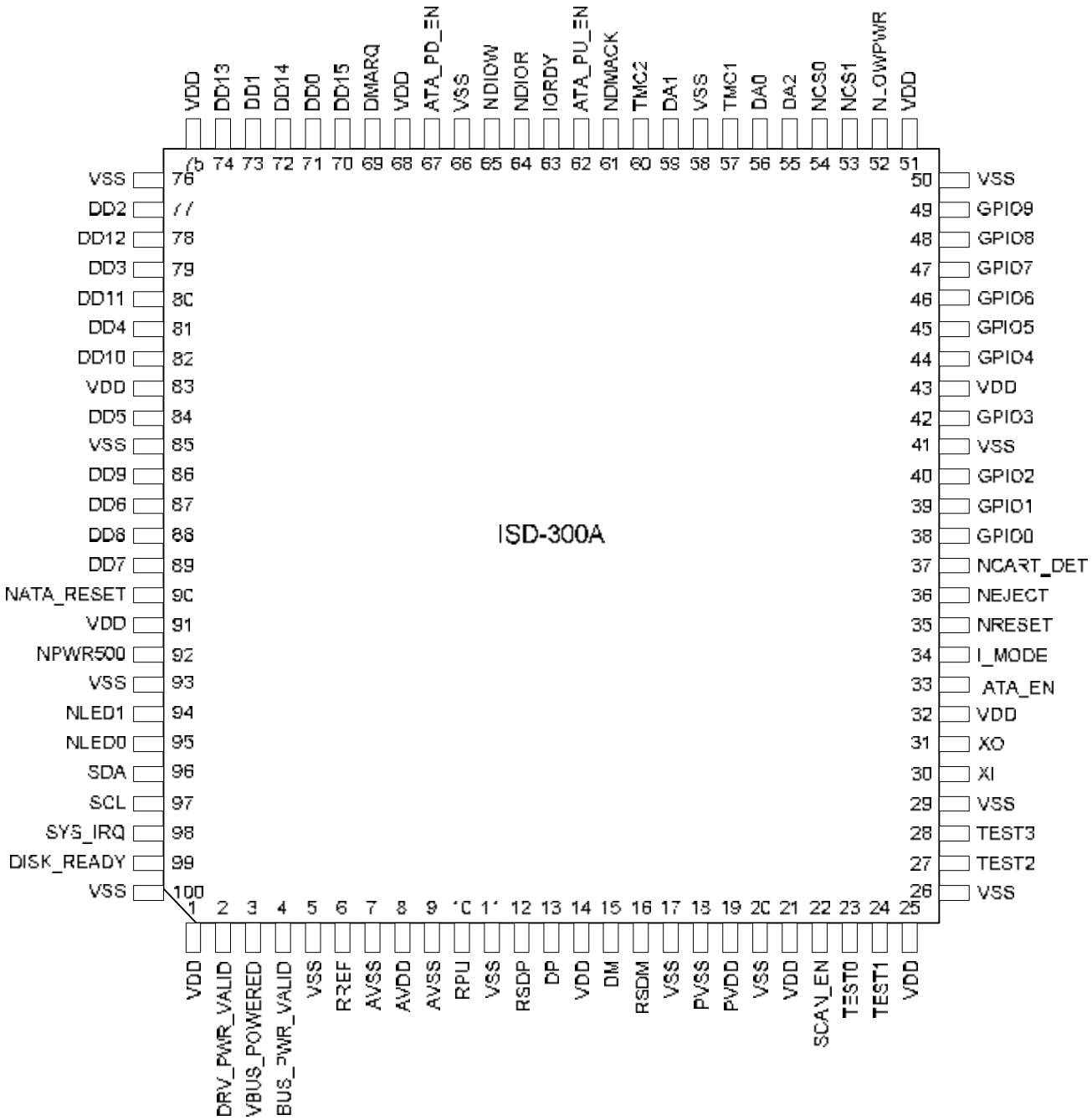


Figure 1 – Pin Layout

Pin Name	TQFP Pin #	Dir	Type	Description
NRESET	35	I	LVTTL, 5V tolerant, hysteresis	Active low. Asynchronous chip reset. To evoke reset, NRESET must be held asserted for a minimum of 1 ms after power is stable.
XI	30	I	OSC input	30 MHz crystal connection. 3.3V tolerant input.
XO	31	O	OSC output	30 MHz crystal connection.
TEST0 – TEST3	25, 24, 27, 28	I	LVTTL, 5V tolerant, internal pull-down resistor	Active high. ASIC fabrication and mfg. test mode select. The TEST pins must be no-connect or set to 0x0 during normal operation.
SCAN_EN	22	I	LVTTL, 5V tolerant, internal pull-down resistor	Active high. ASIC test – scan chain enable. SCAN_EN must be a no-connect or set to 0 during normal operation.
ATA_EN	33	I	LVTTL, 5V tolerant, hysteresis	Active high. ATA interface enable. Allows ATA bus sharing with other host devices. Setting ATA_EN=1 enables the ATA interface for normal operation. Disabling ATA_EN 3-states (high-Z) the ATA interface and halts the ATA interface state machine logic.
SYS_IRQ	98	I	LVTTL, 5V tolerant, internal pull down resistor, hysteresis	Active high. USB interrupt. SYS_IRQ controls ISD-300A1 responses to USB interrupt pipe requests. Setting SYS_IRQ = 1 enables the return of interrupt data to the host.
DISK_READY	99	I	LVTTL, 5V tolerant, hysteresis	Active high. Indicates device is powered and ready to begin accepting ATA / ATAPI commands.
NLOWPWR	52	O	12 mA LVTTL, 5V tolerant	Active low. Indicates when the ISD-300A1 is in a low power state of operation. Open drain during normal operation.
NPWR500	92	O	12 mA LVTTL, 5V tolerant	Active low. Indicates the USB host has enabled use of VBUS power (USB configuration set to 1) up to the requested amount in the USB descriptor *bMaxPower* entry. VBUS powered devices must condition power circuitry with the state of the VBUS_POWERED signal for correct operation. Open drain during normal operation.
VBUS_POWERED	3	I	LVTTL, 5V tolerant, hysteresis	Active high. Indicates the amount of VBUS current the system is capable of consuming (typically <= 100 mA OR <= 500 mA)
VBUS_PWR_VALID	4	I	LVTTL, 5V tolerant, hysteresis	Active high. Indicates that VBUS power is present.
DRV_PWR_VALID	2	I	LVTTL, 5V tolerant, hysteresis	Power / connection indication in hybrid power systems (VBUS ISD-300A1, brick device). Functionality and active polarity is controlled with configuration data. Set DRV_PWR_VALID = 0 if the functionality is not utilized.
GPIO0 – GPIO9	38, 39, 40, 42, 44, 45, 46, 47, 48, 49	IO	12 mA LVTTL, 5V tolerant, internal pull-down resistor	General purpose IO pins. Configuration data provides independent 3-state control for each GPIO pin. The GPIO pins may be left as no-connect if functionality is not utilized.
NCARD_DET	37	I	LVTTL, 5V tolerant, hysteresis	Active low. Media present indication. If remote wakeup is enabled by the USB host, a state change on this pin will cause the ISD-300A1 to perform a USB remote wakeup event. Filtered internally by ISD-300A1. Set NCARD_DET = 1 if the functionality is not utilized.

Pin Name	TQFP Pin #	Dir	Type	Description
MEJECT	38	I	LVTTL, 5V tolerant, hysteresis	Active low. Media eject requested. If remote wakeup is enabled by the USB host, a state change on this pin will cause the ISD-300A1 to perform a USB remote wakeup event. Filtered internally by ISD-300A1. Set MEJECT = 1 if the functionality is not utilized.
SCL	97	O	6 mA LVTTL, 5V tolerant	I^2C clock. Open drain during normal operation. This pin may be left as a no-connect pin if the I^2C interface is not utilized.
SDA	96	IO	6 mA LVTTL, 5V tolerant	I^2C address/data. Open drain during normal operation. An external pull-up resistor is required for correct operation in all ISD-300A1 modes of operation.
DMARQ	69	I	LVTTL, 5V Fail Safe	ATA control.
NDMACK	61	O	6 mA LVTTL, 5V Fail Safe	ATA control.
DA0 – DA2	56, 59, 55	O	6 mA LVTTL, 5V Fail Safe	ATA Address.
DD0 – DD15	71, 73, 77, 79, 81, 84, 87, 89, 88, 86, 82, 80, 78, 74, 72, 70	IO	6 mA LVTTL, 5V Fail Safe	ATA Data.
NIOOR	64	O	6 mA LVTTL, 5V Fail Safe	ATA control.
NIOW	65	O	6 mA LVTTL, 5V Fail Safe	ATA control.
NCS0, NCS1	54, 53	O	6 mA LVTTL, 5V Fail Safe	ATA Chip Selects.
IORDY	63	I	LVTTL, 5V Fail Safe	ATA control.
ATA_PU_EN	62	O	6 mA LVTTL, 5V Fail Safe	Active high. ATA IORDY pull-up connection. Driven low during USB suspend, 3-stated (hi-Z) when ATA_EN=0.
ATA_PD_EN	67	O	6 mA LVTTL, 5V Fail Safe	Active low. ATA DMARQ pull-down connection. 3-state (hi-Z) when ATA_EN=0.
NATA_RESET	90	O	6 mA LVTTL, 5V Fail Safe	Active low. ATA reset.
NLED0	95	O	12 mA LVTTL	Active low. LED drive to indicate USB bus speed. Active when utilizing HS, inactive during FS or USB suspend or other low power modes of operation. Open drain during normal operation. Leave as a no-connect pin if functionality is not utilized.
NLED1	9	O	12 mA LVTTL	Active low. LED drive to indicate status of device initialization. Flashing when initializing is in progress, solid when the device is initialized, and inactive during USB suspend or other low power modes of operation. Open drain during normal modes of operation. Leave as a no-connect pin if functionality is not utilized.
I_MODE	34	I	LVTTL, 5V Tolerant	Active high. Indicates ISD-300A1 configuration / USB descriptor information is obtained using the ATA vendor specific Identify command (F8h)
RSDM	16	O	USB IO	USB full speed output buffer (D-). RSDM also functions as a current sink for termination during HS operation.

Pin Name	TQFP Pin #	Dir	Type	Description
DM	15	IO	USB IO	USB high speed IO buffer (D-).
DP	13	IO	USB IO	USB high speed IO buffer (D+).
RSDP	12	O	USB IO	USB full speed output buffer (D+). RSDP also functions as a current sink for termination during HS operation.
RPU	10	O	USB output	RPU sources power for the 1.5K ohm resistor attached to D+ during full speed operation.
RREF	6		Analog	PLL voltage reference. Current source for 9.1K ohm resistor (1%) connected to AVSS.
TMC1	57	I	ASIC test	Fabrication only. Connect to VSS.
TMC2	60	I	ASIC test	Fabrication only. Connect to VSS.
PVDD	19			Analog 3.3V supply (PLL)
PVSS	18			Analog 3.3V ground (PLL)
AVDD	8			Analog 3.3V supply
AVSS	7, 9			Analog ground
VDD	1, 14, 21, 25, 32, 43, 51, 68, 75, 83, 91			3.3V digital supply
VSS	5, 11, 17, 20, 26, 29, 41, 50, 58, 66, 76, 85, 93, 100			Digital ground

Table 2 – Pin Descriptions

Overview

- Compact 100 pin TQFP package – No Requirement For Additional External ROM Or RAM
- USB Mass Storage Class Bulk-Only Specification Compliant (Version 1.0)
- 5V Tolerant Inputs, 3.3V Output Drive, Single 3.3V Supply Voltage Requirement Simplifies System Integration
- Command Queuing Hooks In Hardware Allow Near Theoretical USB Data Transfer Rates
- USB Version 2.0 Compliant
  - Integrated USB Transceiver
  - High Speed (480 Mbit) And Full Speed (12 Mbit) Support
  - USB Suspend / Resume, Remote Wakeup Support
- Two Power Modes Of Operation
  - USB Bus Powered
  - Self Powered
- Flexible USB Descriptor And Configuration Retrieval Source
  - I^2C Serial ROM Interface
  - ATA Interface Using Vendor Specific ATA Command (FBh) Implemented On ATAPI Or ATA Device
  - Default On-Chip ROM Contents For Manufacturing / Development
- Large 8 Kbyte Data Buffer Maximizes ATA / ATAPI Data Transfer Rate
- ATA Interface Supports ATA PIO Modes 0–4, UDMA Modes 0–4 Of Operation (Multi-word DMA Not Supported). ATA Interface Operation Mode Is Automatically Selected During Device Initialization Or Manually Programmed With Configuration Data
- Automatic Detection Of Either Master or Slave ATA/ATAPI Devices
- Event Notification Via Vendor Specific ATA Command
  - Configurable ATA Command
  - Input Pins For Media Cartridge Detection And Ejection Request
  - USB Bus State Indications (Reset, FS/HS Mode Of Operation, Suspend/Resume)
- Multiple LUN support
- ATA Translation Provides Seamless ATA Support with Standard MSC Drivers
  - Additional ATA Command Support Provided By Vendor Specific ATACBs (ATA Command Blocks Utilizing the MSC Command Block Wrapper)
- Provisions To Share ATA Bus With Other Hosts
- Manufacturing Interconnect Test Support Provided With Vendor Specific USB Commands
  - Read / Write Access To Relevant ASIC Pins
- Utilizes Inexpensive 30Mhz Crystal For Clock Source

Introduction

The ISD-300A1 implements a bridge between one USB port and one ATA or ATAPI based mass storage device port. This bridge adheres to the *Mass Storage Class Bulk-Only Transport* specification. Hardware design allows CBW command queuing, which with vendor specific drivers allows data transfer rates of up to the USB theoretical maximum.

The USB port of the ISD-300A1 is connected to a host computer directly or via the downstream port of a USB hub. Host software issues commands and data to the ISD-300A1 and receives status and data from the ISD-300A1 using standard USB protocol.

The ATA/ATAPI port of the ISD-300A1 is connected to a mass storage device. A large 8 Kbyte buffer maximizes ATA/ATAPI data transfer rates by minimizing losses due to device seek times. The ATA interface supports ATA PIO modes 0-4, and Ultra Mode DMA modes 0-4.

The device initialization process is configurable, enabling the ISD-300A1 to initialize most ATA/ATAPI devices without software intervention. The ISD-300A1 can also be configured to allow software initialization of a device if initialization requirements are not supported by ISD-300A1 algorithms.

ISD-300A1 Configuration

Certain timing parameters and operational modes are configurable by external configuration data. USB descriptor information is also retrieved externally. ISD-300A1 configuration data should not be confused with the USB Configuration Descriptor data.

ISD-300A1 Configuration and USB Descriptor Sources

ISD-300A1 configuration and USB descriptor data can be retrieved from three sources. **Table 3** indicates the method of determining which data source is used.

ISD-300A1 configuration and USB descriptor data can be supplied from an I^2C serial memory device. The ISD-300A1 can address 2 Kbytes of I^2C data, but ISD-300A1 configuration and USB descriptor information are limited to 512 bytes maximum. Unused register space in the I^2C serial memory device may be used for product specific data storage. Note that no descriptor is allowed to span multiple pages within the I^2C serial memory device. The ISD-300A1 provides support for the 24LC01-16 EEPROM family.

Alternatively, configuration and descriptor data can be supplied by an attached mass storage device through a vendor-specific Identify (FBh) ATA command. The ISD-300A1 provides 256 bytes of internal RAM for FBh data storage.

The ISD-300A1 also contains an internal set of ISD-300A1 configuration and USB descriptors. Retrieval of internal ROM data will occur under the specific circumstances outlined in **Table 3**. The internal descriptors may only be used during manufacturing, as the internal ROM values disable some features required for normal operation to aid use in a manufacturing environment. *NOTE: The internal descriptors do not provide a unique serial number (required for USB Mass Storage Class compliance), and therefore cannot be used for shipping products. An external I^2C memory device or utilization of the vendor specific FBh identify command is required to correctly configure the ISD-300A1 for operation and provide a unique serial number for MSC compliance.*

Table 3 describes how the ISD-300A1 determines USB descriptor / configuration sources.

I_MODE Pin Active	I^2C Memory Device present	Signature Check Passes	ISD-300A1 Configuration and USB Descriptor Retrieval
No	No	X	In this mode, the ISD-300A1 uses internal ROM contents for USB descriptor information and configuration register values. *This mode is for debug / manufacturing operation only. Not for shipping products.*
Yes	X	No	In this mode, the ISD-300A1 uses internal ROM contents for USB descriptor information. Configuration register values are loaded from internal ROM. *This is not a valid mode of operation.*
Yes	X	Yes	The ISD-300A1 retrieves all Descriptor and Configuration values from the vendor-specific Identify (FBh) data. The ISD-300A1 is configured using internal ROM values until FBh data becomes available.
No	Yes	No	The ISD-300A1 uses internal ROM contents for USB descriptor information. Configuration register values are loaded from internal ROM. In this mode of operation, any ISD-300A1 vendor specific configuration access causes the ISD-300A1 to recheck the signature field. Once the signature check passes, SROM data is returned for USB descriptors requests. *This is not a valid mode of operation.*
No	Yes	Yes	The ISD-300A1 retrieves all Descriptor and Configuration values from the I^2C memory device. The ISD-300A1 is configured using values present in the I^2C memory device data.

Table 3 – ISD-300A1 Configuration and Descriptor Sources

Internal ROM Contents

Internal on-board ROM addresses and the contents of those locations are shown in the **ISD-300A1 Configuration/USB Descriptor Data Formatting** section on page 9 of this document.
Internal ROM is necessary for manufacturing activities. Internal ROM contents allow the host to enumerate the ISD-300A1 when an un-programmed I^2C memory device is connected.

I^2C Memory Device Interface

The ISD-300A1 supports a subset of the "slow mode" specification (100 KHz) required for 24LC01-16 EEPROM family device support. Features such as "Multi-Master", "Clock Synchronization" (the SCL pin is output only), "10-bit addressing", and "CBUS device support", are NOT supported. Vendor specific USB commands allow the ISD-300A1 to address up to 2 K bytes of data (although configuration / descriptor information is limited to 512 bytes of register space).

Following release of NRESET, the ISD-300A1 waits 50ms, then checks for I^2C device presence. If an I^2C device is present but does not pass signature check (first two data bytes must equal 0x1D51), the ISD-300A1 re-tests the signature with each vendor specific USB load or read access of configuration bytes 0 and 1. Once the signature check passes, I^2C data is returned for USB descriptor requests. If an I^2C device is detected initially, it is always assumed present until the next reset cycle (NRESET). If an I^2C device is present, a lack of an ACK response when required causes the ISD-300A1 to stall that USB request. The ISD-300A1 will attempt the access again with the next USB request.

Programming of the I^2C memory device can be accomplished using an external device programmer, ISD-300A1 supported vendor specific USB commands, or using a "bed of nails". An example of I^2C memory device data formatting is shown in **Appendix A – Example EEPROM or FBh Identify Data Contents**.

Vendor-Specific Identify Data (FBh)
If an I^2C memory device is not utilized, the ISD-300A1 must be configured to accept descriptor and configuration data from an attached device using a vendor-specific identify command. (See **I_MODE Pin** on page 41)

For vendor specific identify data (FBh) to be deemed valid, it must pass the signature check (first two data bytes must equal 0x4D51). In the event of a failed signature check, the ISD-300A1 will respond to all USB GET_DESCRIPTOR or GET_CONFIGURATION commands by returning defaults contained in internal ROM.

An example of vendor specific identify data (FBh) formatting is shown in **Appendix A – Example EEPROM or FBh Identify Data Contents** on page 51.

ISD-300A1 Configuration/USB Descriptor Data Formatting

Data formatting for all ISD-300A1 configuration data and USB descriptor data is identical for internal ROM, I^2C memory device data, and vendor specific identify data (FBh). The following sections show how the ISD-300A1 configuration data is mapped into address space. The **USB Interface** section on page 14 explains formatting of USB descriptor data.

ISD-300A1 Configuration Data
The ISD-300A1 Configuration Data is located at addresses 0x0 to 0xF of the Descriptor/Configuration data contents. Configuration Data determine certain parameters and operational modes used by the ISD-300A1. Any vendor specific USB command write operation to I^2C memory device configuration space will simultaneously update internal configuration register values as well. If the I^2C memory device is programmed without vendor specific USB commands, the ISD-300A1 must be asynchronously reset (NRESET) before configuration data is reloaded.

Formatting is identical for the internal ROM, the I^2C memory device, and FBh data. ISD-300A1 configuration data is loaded into internal registers, regardless of the original data source.

Address	Field Name	Description	On-board ROM Defaults
0x0	I^2C memory device Signature (LSB)	LSB I^2C memory device signature byte. Register does not exist in HW	0x51
0x1	I^2C memory device Signature (MSB)	MSB I^2C memory device signature byte. Register does not exist in HW	0x4D
0x2	Event Notification	ATAPI event notification command. Setting this field to 0x00 disables this feature.	0x00
0x3	APM Value	ATA Device Automatic Power Management Value. If an attached ATA device supports APM and this field contains other than 0x00, the Initialization state machines will issue a SET FEATURES command to enable APM with the register value during the drive initialization process. Setting APM Value to 0x00 disables this functionality. This register value is ignored with ATAPI devices.	0x00
0x4	ATA Initialization Timeout	Time in 128 millisecond granularity before the ISD-300A1 stops polling the ALT STAT register for reset complete and restarts the reset process (0x80 = 16.4 seconds).	0x80

Address	Field Name	Description	On-board ROM Defaults
0x5	USB Bus Mode	Bit (7) – read only. USB bus mode of operation 0 USB bus is operating in full speed mode (12 Mbit/sec). 1 USB bus is operating in high speed mode (480 Mbit/sec).	0x00
	ATAPI Command Block Size	Bit (6) CBW Command Block Size 0 12 byte ATAPI CB 1 16 byte ATAPI CB	
	Master/Slave Selection	Bit (5) Device number selection. This bit is valid only when "Skip ATA/ATAPI Device Initialization" is active. Under ISD-300A1 control ("Skip ATA/ATAPI Device Initialization" = '0'), the value is ignored. 0 Drive 0 (master) 1 Drive 1 (slave)	
	ATAPI Reset	Bit (4) ATAPI reset during drive initialization. Setting this bit enables the ATAPI reset algorithm in the drive initialization state machines	
	ATA /ATAPI	Bit (3) – read only. Indicates if an ATA or ATAPI device is detected 0 ATAPI device 1 ATA device or possible device initialization failure.	
	Force USB FS	Bit(2) Force USB full speed only operation. Setting this bit prevents the ISD-300A1 from negotiating HS operation during USB reset events 0 Normal operation – allow HS negotiation during USB reset 1 USB FS only – do not allow HS negotiation during USB reset	
	VS / MSC SOFT_RESET	Bit(1) Vendor Specific / MSC SOFT RESET control 0 Vendor Specific USB command utilized for SOFT_RESET 1 Mass Storage Class USB command utilized for SOFT_RESET	
	DISK_READY Polarity	Bit (0) DISK_READY active polarity. DISK_READY Polarity is ignored if I_MODE is set to 1. During I_MODE operation DISK_READY polarity is active high. 0 Active high polarity 1 Active low polarity	
0x6	ATA Command Designator (Byte 0, LSB)	Value in CBW CB field that designates if the CB is decoded as vendor specific ATA commands instead of the ATAPI command block.	0x21
0x7	ATA Command Designator (Byte 1, MSB)	Value in CBW CB field that designates if the CB is decoded as vendor specific ATA commands instead of the ATAPI command block.	0x21

Address	Field Name	Description	On-board ROM Defaults
0x8	Initialization Status	Bit (7) – read only Drive Initialization Status If set, indicates the drive initialization sequence state machine is active	0x00
	Force ATA Device	Bit (6) Allows software to manually enable ATA Translation with devices that do not support ISD-300A1 device initialization algorithms. *Note: Force ATA Device must be set '1' in conjunction with Skip ATA/ATAPI Device Initialization and ATA Translation Enable.* Software must issue an INQUIRY command followed with a MSC reset to allow the ISD-300A1 to parse drive information and optimize system performance and operation. Force ATA Device should be set '0' for devices that support ISD-300A1 device initialization algorithms.	
	Skip ATA / ATAPI Device Initialization	Bit (5) Skip_Init – This bit should be cleared for LUNONE operation. The host driver must initialize the attached device (if required) when this bit is set. *Note: For ATAPI devices, if Skip_Init is set the host driver must issue an IDENTIFY command utilizing ATACBs to allow the ISD-300A1 to parse drive information and optimize system performance and operation. Refer to InATACBActionStatus in the* ATA Command Block - Field Descriptions *section on page 30 for further information.* 0 normal operation 1 only reset the device and write the device control register prior to processing commands.	
	Obsolete	Bit (4:3) – Shall be set to '0'	
	Last LUN Identifier	Bits (2:0) Maximum number of LUNs device supports.	
0x9	ATA_EN	Bit (7) – read only. Current logic state of the ATA_EN pin	0x01
	Obsolete	Bit (6:1) – Shall be set to 0	
	SRST Enable	Bit (0) SRST reset during drive initialization. Setting this bit enables the SRST reset algorithm in the drive initialization state machines.	
0xA	ATA Data Assert	Bits (7:4) Standard values for ATA compliant devices and a 30.0 MHz system clock (in binary). *Note: These values are only valid when the Override PIO Timing configuration bit is set.* mode 0 0101 (5−1)*33.33 = 200 ns mode 1 0011 (3−1)*33.33 = 133 ns mode 2 0011 (3−1)*33.33 = 133 ns mode 3 0010 (2−1)*33.33 = 100 ns mode 4 0010 (2−1)*33.33 = 100 ns	0x5C
	ATA Data Recover	Bits (3:0) ATA cycle times are calculated using Data Assert and Data Recover values. Standard recover values and cycle times for ATA compliant devices and a 30.0 MHz system clock (in binary). *Note: These values are only valid when the Override PIO Timing configuration bit is set.* mode 0 1100 (4−1)+(12−1)*33.33 = 600 ns mode 1 0111 (2−1)+(7−1)*33.33 = 400 ns mode 2 0011 (2−1)+(3−1)*33.33 = 233 ns mode 3 0010 (2−1)+(2−1)*33.33 = 200 ns mode 4 0000 (2−1)+(0−1)*33.33 = 133 ns	

Address	Field Name	Description	On-board ROM Defaults
0xB	ATA Data Setup	Bits (7:5) Setup time is only incurred on the first data cycle of a burst. Standard values for ATA compliant devices and a 30.0 MHz system clock are (in binary): *Note: These values are only valid when the Override PIO Timing configuration bit is set.* mode 0 010 (2+1)*33.33 = 133 ns mode 1 001 (1+1)*33.33 = 66 ns mode 2 001 (1+1)*33.33 = 66 ns mode 3 001 (1+1)*33.33 = 66 ns mode 4 000 (0+1)*33.33 = 33 ns	0x40
	Drive Power Valid Polarity	Bit (4) Controls the polarity of DRV_PWR_VALID pin 0 Active low ("connected ground" indication) 1 Active high (power indication from device)	
	Override PIO Timing	Bit (3) This field is used in conjunction with ATA Data Setup, ATA Data Assertion, ATA Data Recover, and PIO Mode Selection fields. 0 Use timing information acquired from the Drive 1 Override device timing information with configuration values	
	Drive Power Valid Enable	Bit (2) Enable for the DRV_PWR_VALID pin. Drive Power Valid should only be enabled in cable applications where the ISD-300A1 is VBUS powered. 0 pin disabled (most systems) 1 pin enabled	
	ATA Read Kludge	Bit (1) PIO data read 3-state control. Enabling this will 3-state (hi-Z) the ATA data bus during PIO read operations while addressing the data register. In most applications this bit is set to '0'. This functionality is provided as a solution for devices that erroneously drive the ATA data bus continuously during PIO data register reads. 0 Normal operation as per ATA/ATAPI interface specification. 1 3-state (hi-Z) DD[15:0] during PIO data register reads.	
	I_MODE	Bit (0) read only This bit reflects the current state of the I_MODE input pin.	

Address	Field Name	Description	On-board ROM Defaults
0xC	SYS_IRQ	Bits(7) – read only This bit reflects the current logic state of the SYS_IRQ input.	0x60
	DISK_READY	Bit(6) – read only This bit reflects the current logic state of the DISK_READY input.	
	ATA Translation Enable	Bit(5) Enable ATAPI to ATA protocol translation enable. If enabled, AND if an ATA device is detected, ATA translation is enabled. *Note: If Reg ATA/ATAPI Device Initialization is set '1', Force ATA Device must also be set '1' in order to utilize ATA translation. Software manufacturer must do HOST-SET command followed with an MSC reset to enable ATA translation operation.* 0 ATA Translation Disabled 1 ATA Translation Enable	
	ATA UDMA Enable	Bit(4) Enable Ultra Mode data transfer support for ATA devices. If enabled, AND the ATA device reports UDMA support, the ISD-300A1 will utilize UDMA data transfers. 0 Disable ATA device UDMA support 1 Enable ATA device UDMA support	
	ATAPI UDMA Enable	Bit(3) Enable Ultra Mode data transfer support for ATAPI devices. If enabled, AND the ATAPI device reports UDMA support, the ISD-300A1 will utilize UDMA data transfers. 0 Disable ATAPI device UDMA support 1 Enable ATAPI device UDMA support	
	ROM UDMA Mode	Bits(2:0) ROM UDMA Mode indicates the highest UDMA mode supported by the product. The ISD-300A1 will utilize the lesser of ROM UDMA Mode or the highest mode supported by the device. *Note: UDMA read operation mode timing is controlled by the device.* mode 0 000 120.3 ns per 16-bit word write mode 1 001 100 ns per 16-bit word write mode 2 010 66.7 ns per 16-bit word write mode 3 011 66.7 ns per 16-bit word write mode 4 100 33.3 ns per 16-bit word write	

Address	Field Name	Description	On-board ROM Defaults
0xD	PIO Mode Selection	Bits (7:5) PIO Mode Selection. The PIO mode reported back to the device if the Override PIO Timing configuration bit is set. This field represents the PIO mode of operation configured by the ATA Data Setup, ATA Data Assertion, ATA Data Recover, and Override PIO Timing fields. mode 0 000 mode 1 001 mode 2 010 mode 3 011 mode 4 100	0x03
	Skip Pin Reset	Bit (4) Skip ATA_NRESET assertion. *Note: SRST Enable must be set in conjunction with Skip Pin Reset.* Setting this bit causes the Initialize algorithm to bypass ATA_NRESET assertion unless a DISK_READY 0->1 event occurred. All other reset events utilize SRST as the drive reset mechanism. 0 Allow ATA_NRESET assertion for all resets 1 Disable ATA_NRESET assertion except for drive power-on reset cycles	
	General Purpose IO	Bits (3:2) GPIO[0:8] input / output control Writing this register controls the output state of the GPIO pin (if the 3-state control is enabled) Reading this register returns the logic value from the GPIO pin	
	General Purpose IO 3-state control	Bits (1:0) GPIO[0:8] 3-state control 0 Output enabled (GPIO pin is an output) 1 3-state(hi-Z) (GPIO pin is an input)	
0xE	General Purpose IO	Bits[7:0] GPIO[7:0] input / output control Writing this register controls the output state of the GPIO pin (if the 3-state control is enabled) Reading this register returns the logic value from the GPIO pin	0x00
0xF	General Purpose IO 3-state control	Bits[7:0] GPIO[7:0] 3-state control 0 Output enabled (GPIO pin is an output) 1 3-state (hi-Z) (GPIO pin is an input)	0x0F

Table 4 – ISD-300A1 Configuration Bytes

USB Interface

The ISD-300A1 is electrically and logically compliant with the *Universal Serial Bus Specification Revision 2.0*.

Descriptors

Supported Descriptors

- *Device*
- *USB Device Qualifier*

  The ISD-300A1 requires only one Device Qualifier descriptor. The information returned is identical for full and high speed modes of operation.

- *Standard Configuration*

  The ISD-300A1 supports two configurations, depending on the mode of operation. See the **VBUS_POWERED** section on page 38 for more information.

  Configuration bus-powered. This configuration descriptor is reported if the VBUS_POWERED signal is set active, typically indicating more than 100 mA of current is sourced from VBUS.

  Configuration non-bus-powered. This configuration descriptor is reported if the VBUS_POWERED input is set inactive, indicating the system is sourcing 100 mA or less of current from VBUS (self powered system).

- *Other Speed Configuration*

  The ISD-300A1 supports two configurations, depending on the mode of operation. See the **VBUS_POWERED** section on page 38 for more information.

  Other Speed Configuration bus-powered. This configuration descriptor is reported if the VBUS_POWERED signal is active.

  Other Speed Configuration non-bus-powered. This configuration descriptor is reported if the VBUS_POWERED input is inactive.

- *Interface*

  The ISD-300A1 supports two interface descriptors, both FS (full speed) and HS (high speed), each with four possible endpoints.

  - *Endpoint*

    The ISD-300A1 supports the following endpoints:

    Default Control endpoint. Accessible as endpoint 0.

    Bulk Out endpoint. Accessible as endpoint 1.

    Bulk In endpoint. Accessible as endpoint 2.

    Interrupt endpoint. Accessible as endpoint 3.

- *String*

  The ISD-300A1 supports a set of class and vender-specific string descriptors. For more information on strings, refer to the **String Descriptors** section on page 19 of this document.

Descriptor Data Format

Device Descriptor

There is only one device descriptor for each USB device. This descriptor gives USB information about the ISD-300A1 device such as device class and device subclass, etc.

Address	Field Name	Description	On-board Defaults
0x10	bLength	Length of device descriptor in bytes.	0x12
0x11	bDescriptor Type	Descriptor type.	0x01
0x12	bcdUSB (LSB)	USB Specification release number in BCD.	0x00
0x13	bcdUSB (MSB)		0x02
0x14	bDeviceClass	Device class.	0xFF
0x15	bDeviceSubClass	Device subclass.	0x00
0x16	bDeviceProtocol	Device protocol.	0xFF
0x17	bMaxPacketSize0	USB packet size supported for default pipe.	0x40
0x18	idVendor (LSB)	Vendor ID.	0xAB
0x19	idVendor (MSB)		0x05
0x1A	idProduct (LSB)	Product ID.	0x6A
0x1B	idProduct (MSB)		0x00
0x1C	bcdDevice (LSB)	Device release number in BCD LSB (product release number)	0x00

Address	Field Name	Description	On-board Defaults
0x10	bcdDevice (MSB)	Device release number in BCD MSB (silicon release number). *NOTE: This field entry is always returned from internal ROM contents, regardless of the descriptor source.*	0x10 (rev A); 0x11 (rev B)
0x12	Manufacturer	Index to manufacturer string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x19
0x17	iProduct	Index to product string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x3A
0x20	SerialNumber	Index to serial number string. This entry must equal half of the address value where the string starts or 0 if the string does not exist. *The USB Mass Storage Class Bulk Only Transport Specification requires a unique serial number.*	0x00
0x21	bNumConfigurations	Number of configurations supported.	0x01

Table 5 – Device Descriptor

Device Qualifier Descriptor

The device qualifier descriptor describes information about a high-speed capable device that would change if the device were operating at the other speed. For the ISD-300A1, none of the descriptor information requires modification, thus only one Device Qualifier Descriptor is required. The ISD-300A1 returns the same descriptor while operating in either full speed or high speed mode.

Address	Field Name	Description	On-board Defaults
0x22	bLength	Length of device descriptor in bytes.	0x0A
0x23	bDescriptor Type	Descriptor type.	0x06
0x24	bcdUSB (LSB)	USB Specification release number in BCD.	0x00
0x25	bcdUSB (MSB)		0x02
0x26	bDeviceClass	Device class.	0xFF
0x27	bDeviceSubClass	Device subclass.	0x00
0x28	bDeviceProtocol	Device protocol.	0xFF
0x29	bMaxPacketSize0	USB packet size supported for default pipe.	0x40
0x2A	bNumConfigurations	Number of configurations supported	0x01
0x2B	bReserved	Reserved for future use, must be zero	0x00

Table 6 – Device Qualifier Descriptor

Standard Configuration Descriptor

The ISD-300A1 requires two configuration descriptors. The first configuration is returned when the VBUS_POWERED signal is active, the second configuration when the VBUS_POWERED signal is inactive (brick powered). The configuration descriptor contains information about the ISD-300A1 device configuration. Each configuration has one interface that supports four endpoints. See the **VBUS_POWERED** section on page 38 for more information.

Address (Config. Number)	Field Name	Description	On-board Defaults
0x2C(1) 0x80(2)	bLength	Length of configuration descriptor in bytes.	0x09
0x2D(1) 0x81(2)	bDescriptorType	Descriptor type.	0x02

Address (Config. Number)	Field Name	Description	On-board Defaults
0x2E(1) 0x82(2)	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27
0x2F(1) 0x83(2)	bTotalLength (MSB)		0x00
0x30(1) 0x84(2)	bNumInterfaces	Number of interfaces supported. The ISD-300A1 only supports one interface.	0x01
0x31(1) 0x85(2)	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. This value must be set to 0x02	0x02
0x32(1) 0x86(2)	iConfiguration	Index to the configuration string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x00
0x33(1) 0x87(2)	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On-board default 7 Reserved, set to 1. '1' 6 Self-powered. '0' for configuration 1, '1' for configuration 2 5 Remote wake-up. '0' 4-0 Reserved, set to 0. '0'	0x80 (1) 0xC0 (2)
0x34(1) 0x88(2)	bMaxPower	Maximum power consumption for this configuration. Units used are mA*2 (i.e. 0x31 = 98 mA, 0xF9 = 498 mA).	0xF9 (1) 0x31 (2)

Table 7 – Standard Configuration Descriptor(s)

Other Speed Configuration Descriptor

This descriptor describes a configuration of a high-speed capable device if it were operating at its other possible speed. Although two descriptors are not required to distinguish differences between full speed and high speed operation, the ISD-300A1 supports two other speed configuration descriptors to enumerate differences between VBUS powered and self powered operation. The first configuration is returned when the VBUS_POWERED signal is active, the second configuration when the VBUS_POWERED signal is inactive. Each configuration has one interface that supports four endpoints. See the **VBUS_POWERED** section on page 38 for more information.

Address (Config. Number)	Field Name	Description	On-board Defaults
0x35(1) 0x89(2)	bLength	Length of configuration descriptor in bytes.	0x09
0x36(1) 0x8A(2)	bDescriptorType	Descriptor type.	0x07
0x37(1) 0x8B(2)	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27
0x38(1) 0x8C(2)	bTotalLength (MSB)		0x00
0x39(1) 0x8D(2)	bNumInterfaces	Number of interfaces supported. The ISD-300A1 only supports one interface.	0x01
0x3A(1) 0x8E(2)	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. This value must be set to 0x02	0x02
0x3B(1) 0x8F(2)	iConfiguration	Index to configuration string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x00
0x3C(1) 0x90(2)	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On-board default 7 Reserved, set to 1. '1' 6 Self-powered. '0' for configuration 1, '1' for configuration 2 5 Remote wake-up. '0' 4-0 Reserved, set to 0. '0'	0x80 (1) 0xC0 (2)
0x3D(1) 0x91(2)	bMaxPower	Maximum power consumption for the second configuration. Units used are mA*2 (i.e. 0x31 = 98 mA, 0xF9 = 498 mA).	0xF9 (1) 0x31 (2)

Table 8 – Other Speed Configuration Descriptor(s)

Interface Descriptor

This descriptor specifies the interface within a configuration. There are two interface descriptors in the ISD-300A1, one for high speed, and one for full speed. Each interface contains four endpoint descriptors: Default Control (no descriptor), Bulk out, Bulk in, and Interrupt.

Interface and endpoint descriptors cannot be directly accessed using the Get Descriptor USB command. However, interface and endpoint descriptors are always returned as part of the configuration and other speed configuration descriptor. When the other speed configuration descriptor is requested, the interface descriptor returned is dependent upon the USB bus speed mode of operation. When operating in high speed, the full speed interface descriptor is returned with the other speed configuration descriptor. When operating in full speed, the high speed interface descriptor is returned with the other speed configuration descriptor.

Endpoint descriptors and addresses must be in the fixed order of the ISD-300A1 internal defaults: Bulk-out first, then Bulk-in, followed by Interrupt.

Address (HS or FS)	Field Name	Description	On-board Defaults
Interface Descriptor			
0x3E(HS) 0x5D(FS)	bLength	Length of interface descriptor in bytes.	0x09
0x3F(HS) 0x5E(FS)	bDescriptorType	Descriptor type.	0x04
0x40(HS) 0x5F(FS)	bInterfaceNumber	Interface number.	0x00
0x41(HS) 0x60(FS)	bAlternateSetting	Alternate settings	0x00
0x42(HS) 0x61(FS)	bNumEndpoints	Number of endpoints	0x03
0x43(HS) 0x62(FS)	bInterfaceClass	Interface class.	0x0F
0x44(HS) 0x63(FS)	bInterfaceSubClass	Interface subclass.	0x00
0x45(HS) 0x64(FS)	bInterfaceProtocol	Interface protocol.	0xFF
0x46(HS) 0x65(FS)	iInterface	Index to first interface string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x00
USB Bulk Out Endpoint			
0x47(HS) 0x66(FS)	bLength	Length of this descriptor in bytes.	0x07
0x48(HS) 0x67(FS)	bDescriptorType	Endpoint descriptor type	0x05
0x49(HS) 0x68(FS)	bEndpointAddress	This is an Out endpoint, endpoint number 1.	0x01
0x4A(HS) 0x69(FS)	bmAttributes	This is a bulk endpoint.	0x02
0x4B(HS) 0x6A(FS)	wMaxPacketSize (LSB)	Max data transfer size.	0x00 (HS) 0x40 (FS)
0x4C(HS) 0x6B(FS)	wMaxPacketSize (MSB)		0x02 (HS) 0x00 (FS)
0x4D(HS) 0x6C(FS)	bInterval	HS interval for polling (max NAK rate). Does not apply to FS bulk endpoints.	0x01 (HS) 0x00 (FS)
USB Bulk In Endpoint			
0x4E(HS) 0x6D(FS)	bLength	Length of this descriptor in bytes.	0x07

Address (HS or FS)	Field Name	Description	On-board Defaults
0x4B(HS) 0x8B(FS)	bDescriptorType	Endpoint descriptor type	0x05
0x4C(HS) 0x8C(FS)	bEndpointAddress	This is an In endpoint, endpoint number 2.	0x82
0x4D(HS) 0x8D(FS)	bmAttributes	This is a bulk endpoint.	0x02
0x4E(HS) 0x8E(FS)	wMaxPacketSize (LSB)	Max data transfer size.	0x00 (HS) 0x40 (FS)
0x4F(HS) 0x8F(FS)	wMaxPacketSize (MSB)		0x02 (HS) 0x00 (FS)
0x50(HS) 0x90(FS)	bInterval	HS interval for polling (max NAK rate). Does not apply to FS bulk endpoints.	0x01 (HS) 0x00 (FS)
USB Interrupt Endpoint			
0x51(HS) 0x91(FS)	bLength	Length of this descriptor in bytes.	0x07
0x52(HS) 0x92(FS)	bDescriptorType	Endpoint descriptor type	0x05
0x53(HS) 0x93(FS)	bEndpointAddress	This is an interrupt endpoint, endpoint number 3.	0x83
0x54(HS) 0x94(FS)	bmAttributes	This is an interrupt endpoint.	0x03
0x55(HS) 0x95(FS)	wMaxPacketSize (LSB)	Max data transfer size.	0x02
0x56(HS) 0x96(FS)	wMaxPacketSize (MSB)		0x00
0x57(HS) 0x97(FS)	bInterval	This is the polling interval.	0x05 (HS) 0x20 (FS)

Table 9 – HS and FS Interface Descriptor(s)

String Descriptors

The ISD-300A1 supports multiple string descriptors, such as a manufacturer name string indexed by the iManufacturer field in the Device Descriptor. The descriptor index is specified as the starting address values divided by 2 (i.e. Manufacturer string begins at address 0x92, but is specified in the iManufacturer field as 0x49).

String index 0 must contain the LANGID of exactly one language, as the ISD-300A1 supports only a single language. Microsoft defines the LANGID codes for Windows, as described in *Developing International Software for Windows 95 and Windows NT*, Nadine Kano, Microsoft Press, Redmond, Washington. Note the LANGID code for English is 0x0409.

The following table shows how the LANGID, manufacturer, and product strings are formatted in the on-board ROM contents, and this can be considered an example of how to format strings in the PC memory device or FBh Identify data. Each string character is comprised of an ASCII character appended to a NULL byte to meet the UNICODE encoding requirements as specified in *The Unicode Standard, Worldwide Character Encoding, Version 1.0, Volumes 1 and 2*.

Address	Field Name	Description	On-board Defaults
USB String Descriptor - Index 0 (LANGID)			
0x7C	bLength	LANGID string descriptor length in bytes.	0x04
0x7D	bDescriptorType	Descriptor type	0x03
0x7E	LANGID (LSB)	Language supported. Note: See LANGID table in Microsoft documentation (the code for English is 0x0409)	0x09
0x7F	LANGID (MSB)		0x04
USB String Descriptor - Manufacturer			

Address	Field Name	Description	On-board Defaults
0x92	bLength	String descriptor length in bytes	0x22
0x93	bDescriptorType	Descriptor type.	0x03
0x94	bString	ASCII character.	0x49 ("I")
0x95	bString	("NULL")	0x00
0x96	bString	ASCII character.	0x6E ("n")
0x97	bString	("NULL")	0x00
0x98	bString	ASCII character.	0x20 (" ")
0x99	bString	("NULL")	0x00
0x9A	bString	ASCII character.	0x53 ("S")
0x9B	bString	("NULL")	0x00
0x9C	bString	ASCII character.	0x79 ("y")
0x9D	bString	("NULL")	0x00
0x9E	bString	ASCII character.	0x73 ("s")
0x9F	bString	("NULL")	0x00
0xA0	bString	ASCII character.	0x74 ("t")
0xA1	bString	("NULL")	0x00
0xA2	bString	ASCII character.	0x65 ("e")
0xA3	bString	("NULL")	0x00
0xA4	bString	ASCII character.	0x6D ("m")
0xA5	bString	("NULL")	0x00
0xA6	bString	ASCII character.	0x20 (" ")
0xA7	bString	("NULL")	0x00
0xA8	bString	ASCII character.	0x44 ("D")
0xA9	bString	("NULL")	0x00
0xAA	bString	ASCII character.	0x65 ("e")
0xAB	bString	("NULL")	0x00
0xAC	bString	ASCII character.	0x73 ("s")
0xAD	bString	("NULL")	0x00
0xAE	bString	ASCII character.	0x69 ("i")
0xAF	bString	("NULL")	0x00
0xB0	bString	ASCII character.	0x67 ("g")
0xB1	bString	("NULL")	0x00
0xB2	bString	ASCII character.	0x6E ("n")
0xB3	bString	("NULL")	0x00
USB String Descriptor – Product			
0xB4	bLength	String descriptor length in bytes	0x28
0xB5	bDescriptorType	Descriptor type	0x03
0xB6	bString	ASCII character.	0x55 ("U")
0xB7	bString	("NULL")	0x00
0xB8	bString	ASCII character.	0x53 ("S")
0xB9	bString	("NULL")	0x00
0xBA	bString	ASCII character.	0x42 ("B")
0xBB	bString	("NULL")	0x00
0xBC	bString	ASCII character.	0x20 (" ")
0xBD	bString	("NULL")	0x00
0xBE	bString	ASCII character.	0x53 ("S")
0xBF	bString	("NULL")	0x00
0xC0	bString	ASCII character.	0x74 ("t")
0xC1	bString	("NULL")	0x00

Address	Field Name	Description	On-board Defaults
0x02	bString	ASCII character.	0x6F ("o")
0x03	bString	("NULL")	0x00
0x04	bString	ASCII character.	0x72 ("r")
0x05	bString	("NULL")	0x00
0x06	bString	ASCII character.	0x61 ("a")
0x07	bString	("NULL")	0x00
0x08	bString	ASCII character.	0x67 ("g")
0x09	bString	("NULL")	0x00
0x0A	bString	ASCII character.	0x65 ("e")
0x0B	bString	("NULL")	0x00
0x0C	bString	ASCII character.	0x20 (" ")
0x0D	bString	("NULL")	0x00
0x0E	bString	ASCII character.	0x41 ("A")
0x0F	bString	("NULL")	0x00
0x10	bString	ASCII character.	0x64 ("d")
0x11	bString	("NULL")	0x00
0x12	bString	ASCII character.	0x61 ("a")
0x13	bString	("NULL")	0x00
0x14	bString	ASCII character.	0x70 ("p")
0x15	bString	("NULL")	0x00
0x16	bString	ASCII character.	0x74 ("t")
0x17	bString	("NULL")	0x00
0x18	bString	ASCII character.	0x65 ("e")
0x19	bString	("NULL")	0x00
0x1A	bString	ASCI character.	0x72 ("r")
0x1B	bString	("NULL")	0x00
0x1C 0x8F	Unused ROM space		0x00

Table 10 – String Descriptors

Descriptor Requirements

Descriptors programmed into an I^2C memory device must observe the following constraints.

String Descriptor Indexes

An index of 0x00 indicates the string is absent. If the string descriptor is present, the index value is the beginning address location divided by 2. String descriptors must not cross I^2C memory device block boundaries, i.e., the starting address must be moved to the next I^2C memory device boundary.

Pipes

The ISD-300A1 provides four USB pipes: Default Control, Bulk Out, Bulk In, and Interrupt.

Default Control Pipe

The default pipe is used to transport standard, class and vendor-specific USB requests to the ISD-300A1.

Bulk Out Pipe

The Bulk Out pipe is used to send commands and data to an attached mass storage device. Maximum packet size is 64 bytes in FS operation, 512 bytes in HS operation.

Bulk In Pipe
The Bulk In pipe is used to receive status and read data from an attached mass storage device. Maximum packet size is 64 bytes in FS operation, 512 bytes in HS operation.

Interrupt Pipe
The Interrupt pipe implemented in the ISD-300A1 serves two purposes: 1) Some legacy software applications require the endpoint to exist for correct operation, and 2) to enable systems to request service by the host. For more information, see the **SYS_IRQ Pin** section on page 41 of this document.

Requests

The ISD-300A1 responds to three different types of request:

- Standard USB device requests
- Mass Storage Class Bulk-Only requests
- Vendor-specific requests

Standard Requests
The ISD-300A1 supports all USB standard device requests except the optional Set Descriptor request. These requests, which are described in Chapter 9, Device Framework, of the *USB Specification*, are:

- Clear Feature
- Get Configuration
- Get Descriptor (for information on String Descriptors, see **String Descriptors** on page 19)
- Get Interface
- Get Status
- Set Address
- Set Configuration
- Set Interface
- Set Feature

Mass Storage Class Bulk-Only Requests
Mass Storage Class Bulk-Only requests supported by the ISD-300A1 are listed in **Table 11**.

Label	bmRequestType	bRequest	wValue	wIndex	wLength	Data
RESET	0x21	0xFF	0x0000	Interface	0x0000	[None]
GET_MAX_LUN	0xA1	0xFE	0x0000	Interface	0x0001	1 byte

Table 11 – Mass Storage Class Bulk-Only Requests

RESET
This request flushes all buffers and resets the pipes to their default states, resets all hardware registers to their default state, and basically causes the ISD-300A1 to enter a power-up reset state. Any STALL conditions or bulk data toggle bits remain unchanged.

GET_MAX_LUN
The ISD-300A1 returns one byte of data that contains the maximum LUNs supported by the device. This information is derived from the Last LUN Identifier configuration setting, bits (2:0) of configuration data located at address offset 0x8. For example, if the device supports four LUNs then the LUNs would be

numbered from 0 to 3, and the Last LUN Identifier configuration data bit field should be set to 0x3. If no LUN is associated with the device, the Last LUN Identifier shall be set to 0x0.

Vendor-Specific Requests

Vendor specific requests supported by the ISD-300A1 are listed in **Table 12**. The ISD-300A1 will STALL any vendor specific request if not configured by the USB host (USB configuration is 0).

Label	bmRequestType	bRequest	wValue	wIndex	wLength	Data
LOAD_CONFIG_DATA	0x40	0x01	Data Source	Starting Address	Data Length	Configuration Data
READ_CONFIG_DATA	0xC0	0x02	Data Source	Starting Address	Data Length	Configuration Data
SOFT_RESET	0x40	0x03	0x0000	0x0000	0x0000	[None]
CMD_QUEUING_CONTROL	0x40	0x04	Queuing Control	0x0000	0x0000	[None]
BOGUS_READ	0xC0	0x01	0xXXXX	0xXXXX	0xXXXX	Null byte data
LOAD_MFG_DATA	0x40	0x05	Disable / Enable	0x0000 (starting address)	Data Length	Mfg. test data
READ_MFG_DATA	0xC0	0x06	0x0000	0x0000	Data Length	Mfg. test data

Table 12 – Vendor-Specific Requests

LOAD_CONFIG_DATA

This request enables configuration data writes to the data source specified by the wValue field. The wIndex field specifies the starting address and the wLength field denotes the data length in bytes.

Legal values for wValue are as follows:

0x0000	Configuration bytes, address range 0x2 – 0x1F
0x0002	External I^2C memory device

Configuration byte writes must be constrained to addresses 0x2 through 0x1F, as shown in **Table 4 – ISD-300A1 Configuration Bytes** on page 14. Attempts to write outside this address space will result in a STALL condition. Configuration byte writes only overwrite ISD-300A1 Configuration Byte registers, the original data source remains unchanged (I^2C memory device, TDB identify data, or internal ROM).

Writes to I^2C memory devices shall only start on eight-byte boundaries, meaning that the address value must be evenly divisible by eight.

Writes to I^2C memory devices must not cross 256 byte page boundaries, i.e. start and finish write addresses must have equal modulo 256 values. Write operations with beginning and end addresses that do not fall in the same 256 byte page will result in a STALL condition.

Illegal values for wValue as well as attempts to write to an I^2C memory device when none is connected will result in a STALL condition.

READ_CONFIG_DATA

This USB request allows data retrieval from the data source specified by the wValue field. Data is retrieved beginning at the address specified by the wIndex field. The wLength field denotes the length in bytes of data requested from the data source.

Legal values for wValue are as follows:

0x0000	Configuration bytes, addresses 0x0 – 0xF only
0x0001	Internal ROM
0x0002	External I^2C memory device
0x0003	Vendor-specific identify (FBh) data

Illegal values for wValue will result in a STALL condition on the USB port. Attempted reads from an I^2C memory device when none is connected or attempted reads from FBh data when not in I_MODE will result in a STALL condition. Attempts to read configuration bytes with starting addresses greater than 0xF will also result in a STALL condition.

SOFT_RESET

This request resets the ISD-300A1's data path control state machines, buffer RAM and command queue. The attached device is not reset. This USB request is required for error recovery while complex command queuing is enabled.

Issuing a SOFT_RESET when complex command queuing is not enabled will result in a STALL condition.

CMD_QUEUING_CONTROL

This request sets the type of command queuing used by the ISD-300A1. Command queuing is a vendor specific feature of the ISD-300A1 that allows the CBW (refer to the USB Mass Storage Class Bulk Only Transport Specification) and possibly data for a new command to be transferred before the CSW for the previous command has been sent. Queuing commands can hide delays between the CBW, data, and CSW of a command and between commands, and thus improve overall system performance. The ISD-300A1 supports two types of command queuing: simple and complex.

Simple Command Queuing

In simple command queuing the ISD-300A1 stops when there is a phase error and does not process a queued CBW. But when there is a device error the ISD-300A1 continues and processes the queued command. It is up to the host to notice the "command failed" status in the CSW for the first command and recover from the error even though the subsequent queued command might have changed the state of the attached device after the error occurred.

Complex Command Queuing

In complex command queuing the ISD-300A1 stops processing commands in the event of a device error just as it does for a phase error. This preserves the state of the attached device. The SOFT_RESET command is available when complex command queuing is enabled to allow the host to reset the ISD-300A1 and discard any queued commands or data without resetting the attached device. After the SOFT_RESET the host can send another CBW to query the device for more information about the error or re-issue the failed command.

Legal values for wValue are as follows:

0x0000	Simple Command Queuing (**Power-on reset default**)
0x0001	Complex Command Queuing

BOGUS_READ

This USB request is present for legacy software reasons – some USB drivers require this command to exist for proper operation. The ISD-300A1 will return the requested amount of zero filled data packets.

LOAD_MFG_DATA

This USB request is used to enable and control Manufacturing Test Mode operation. Manufacturing Test Mode is provided as a means to implement board/system level interconnect tests. During Manufacturing Test Mode operation, all outputs not associated directly with USB operation are controllable. Normal state machine and register control of output pins are disabled. Control of the select ISD-300A1 IO pins and their 3-state controls are mapped to the USB data packet associated with this request. (See **Table 13 – LOAD_MFG_DATA Data Block Bit Map** for explanation of the required LOAD_MFG_DATA data packet format.)

The wValue field enables/disables Manufacturing Test Mode operation. All Manufacturing Test Mode operation requests must contain a complete data packet (wLength field set to 0x0007) and start from the beginning of the register chain (wIndex field set to 0x0000).

Legal values for wValue are as follows:

0x0000	Normal operation mode – writing this wValue returns the ISD-300A1 to normal operation regardless of previous command data sets (power-on reset default).
0x0001	Manufacturing Test Mode – manufacturing test registers control specific outputs cells of the ISD-300A1 to enable board level testing in the manufacturing environment.

Legal values for wLength are as follows:

0x0000	Valid only when wValue = 0x0000; when disabling Manufacturing Test Mode of operation.
0x0007	Valid only when wValue = 0x0001. For proper Manufacturing Test Mode operation, wLength must equal 0x0007. Any data packet lengths greater than 7 will result in a STALL condition.

Table 13 shows the bit-wise test control register mapping of the data packet associated with the LOAD_MICC_DATA vendor specific USB command.

Byte	Bit(s)	Test / 3-State Control Register Name
0	1:0	NLED[1:0]
0	2	NPWR500
0	3	NATA_RESET
0	4	NDIOW
0	5	NDIOR
0	6	NDMACK
0	7	ATA_PU_EN
1	0	ATA_PD_EN
1	2:1	NCS[1:0]
1	5:3	DA[2.0]
1	6	NLOWPWR
1	7	DD[15:0] 3-State Active h 3-state buffer enable for ATA data bus.
2	7:0	DD[7:0]
3	7:0	DD[15:8]
4	7:0	GPIO[7:0]
5	1:0	GPIO[9:8]
5	7:2	GPIO[5:0] 3-State Enable Active h 3-state buffer enable for each GPIO pin
6	3:0	GPIO[9:6] 3-State Enable Active h 3-state buffer enable for each GPIO pin
6	7:4	Reserved, software must write 0000b

Table 13 – LOAD_MICC_DATA Data Block Bit Map

READ_MFG_DATA

This USB request returns a "snapshot in time" of select ISD-300A1 input pins. The input pin states are bit-wise mapped to the USB data packet associated with this request. ISD-300A1 input pins not associated directly with USB operation can be sampled at any time during normal or Manufacturing Test Mode operation. This request is independent of normal ISD-300A1 state machine control or Manufacturing Test Mode write operations. See **Table 14 – READ_MFG_DATA Data Block Bit Map** for an explanation of the READ_MFG_DATA data packet format.

Legal values for wValue are as follows:

0x0000 wValue must be set to 0x0000.

Legal values for wLength are as follows:

0x0001 –
0x0008 Any data packet lengths greater than 0x0008 will result in a STALL condition.

Table 14 shows the bit-wise input pin mapping of the data packet associated with the READ_MFG_DATA vendor specific USB command. All input and bi-directional pin values are taken from the pin.

Byte	Bit(s)	Pin Name
0	0	DRV_PWR_VALID
0	1	VBUS_PWR_VALID
0	2	VBUS_POWERED
0	3	DISK_READY
0	4	SYS_IRQ
0	5	IORDY
0	6	DMARQ
0	7	I_MODE
1	0	NCART_DET
1	1	N_EJECT
1	3:2	NLED[1:0]
1	4	NPRW500 (output register value only)
1	5	ATA_RESET (output register value only)
1	6	NDIOW (output register value only)
1	7	NDIOR (output register value only)
2	0	NDMACK (output register value only)
2	1	ATA_PU_EN (output register value only)
2	2	ATA_PD_EN (output register value only)
2	4:3	NCS[1:0] (output register value only)
2	7:5	DA[2:0] (output register value only)
3	7:0	DD[7:0]
4	7:0	DD[15:8]
5	7:0	GPIO[7:0]
6	1:0	GPIO[9:8]
6	2	DD[15:0] 3-State Control (internal register)
6	7:3	GPIO[4:0] 3-State Control (internal register)
7	4:0	GPIO[9:5] 3-State Control (internal register)
7	5	MFG_SEL (manufacturing test mode enable)
7	6	NLOWPWR (output register value only)
7	7	ATA_EN

Table 14 – READ_MFG_DATA Data Block Bit Map

ATA/ATAPI Interface

The ATA/ATAPI port on the ISD-300A1 is compliant with the *Information Technology – AT Attachment with Packet Interface – 5 (ATA/ATAPI-5) Specification, T13-1321D Rev 3.* The ISD-300A1 supports both ATAPI packet commands as well as ATA commands (by use of ATA Command Blocks). Additionally, the ISD-300A1 translates ATAPI SFF-8070i commands to ATA commands for seamless integration of ATA devices with generic Mass Storage Class BOT drivers. The ISD-300A1 also provides a vendor-specific "event notify" ATA command to automatically communicate certain USB and system events to the attached device.

Protocol

The ISD-300A1 supports command protocol flows as defined in the *ATA/ATAPI-5 Specification.* Commands are grouped into different classes, based on the protocol followed for command execution.

The ATA/ATAPI interface supports the following clarifications:

- Immediately after the reset recovery period, the ISD-300A1 will write 0x00 to the Device Control register.
- Arbitrary byte count transfers are supported.
- 16-bit data reads and writes are supported.
- 8-bit data transfers are not supported.

Reset Mapping

The ATA/ATAPI interface responds to several resets: Power-on, USB, MSC, and Vendor-specific Soft reset.

In the case of a power-on reset, a full device initialization is performed. IDB data is retrieved and stored if the I_MODE pin is set active.

In the cases of USB reset and MSC reset, a partial initialization is performed which excludes all attempts to perform Identify Device commands.

In the case of a Vendor-specific Soft reset, only the internal ISD-300A1 state machines are reset.

Device Requirements

Attached mass storage devices must support the following:

ATA Reset, ATh, FBh
After deassertion of ATA -RESET, BSY and DRQ must be cleared by the device within the ATA Initialization Timeout configuration setting value.

ATA Polling Device
The device shall be capable of being a polling only device. The ATA signal **INTRQ** is not used by the ISD-300A1.

ATA Initialization Timeout

ISD-300A1 internal ROM has a default configuration value of 8.2 seconds for ATA Initialization Timeout. When I_MODE operation is utilized, the default ATA Initialization Timeout value is used to retrieve F3h data. Once the vendor specific Identify (F3h) command completes, the default value is overridden with the F3h data value.

If an I^2C memory device is utilized for ISD-300A1 configuration and USB descriptor data, the ATA Initialization Timeout value is loaded from the I^2C memory device prior to any ATA interface activity.

Reset Recovery is 5 ms. **Figure 2** graphically defines "Initialization Timeout" and "Reset Recovery".

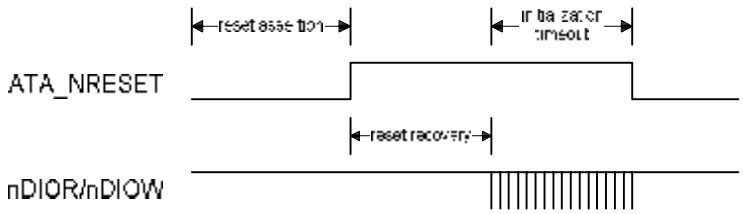


Figure 2 – ATA Reset Protocol

ATA Command Block

ATA commands for the ISD-300A1 are supported by command encoding in the command block portion of the *ASC* Command Block Wrapper *(CBW)*. Refer to the *USB Mass Storage Class (ASC) Bulk Only Transport Specification* for information on CBW formatting.

The ATA Command Block *(ATACB)* provides a means of passing ATA commands and ATA register accesses for execution. The *ATACB* resides in the *CBWCB* portion of the *CBW*. The *ATACB* is distinguished from other command blocks by the first two bytes of the command block matching the *wATACBSignature*. Only command blocks that have a valid *wATACBSignature* are interpreted as ATA Command Blocks. All other fields of the *CBW* and restrictions on the *CBWCB* shall remain as defined in the *USB Mass Storage Class Bulk Only Transport Specification*. The *ATACB* shall be 16 bytes in length. The following table and text defines the fields of the *ATACB*.

Byte	7	6	5	4	3	2	1	0
0-1	*wATACBSignature*							
2	*bmATACBActionSelect*							
3	*bmATACBRegisterSelect*							
4	*bATACBTransferBlockCount*							
5-12	*bATACBTaskFileWriteData*							
13-15	Reserved (0)							

Table 15 – ATA Command Block Formatting

Field Descriptions

wATACBSignature –

This signature indicates that the *CBWCB* contains an *ATACB*. The signature field shall contain the ATA Command Designator value obtained from ISD-300A1 configuration space to indicate an *ATACB* (the default value is 0x2424). Devices capable of accepting only ATA Command Blocks shall return a command failed status if the *wATACBSignature* is not correct.

bmATACBActionSelect –

The bit fields of this register shall control the execution of the *ATACB*. Refer to **Figure 3– ATA Command Block Flow Diagram** for further clarification. The bitmap of the *bmATACBActionSelect* shall be defined as follows:

Bit 7 *IdentifyPacketDevice* – ATA/ATAPI Identify Packet Device Command. Setting *IdentifyPacketDevice* indicates the data phase will contain ATAPI (A1h) or ATA (ECh) IDENTIFY device data. Setting *IdentifyPacketDevice* when the data phase is not IDENTIFY data will cause undetermined device behavior.
0 – Normal operation.
1 – Data phase of command will contain ATAPI or ATA IDENTIFY data, allowing the device to parse data for required device information.

Bit 6 *UDMACommand* - Ultra DMA Data Transfer Enable (Multi-word DMA not supported). Setting *UDMA Command* with non-UDMA capable devices or using it with non-UDMA commands will cause undetermined behavior.
0 – Do not use DMA data transfers (PIO transfers only).
1 – Utilize Ultra DMA for data transfers (device must be capable).

Bit 5 *DEVOverride* – Use the DEV value specified in the *ATACB*.
0 – The DEV bit value will be determined from ISD-300A1 Configuration data (0x5 bit 5).
1 – The DEV bit value will be determined from the *ATACB* (0x3 bit 1).

Bits 4-3 *DFErrorOverride(1:0)* - Device and Phase Error Override. These bits shall not be set in conjunction with *bmATACBActionSelect TaskFileRead*. The order of precedence for error override shall be dependant on the amount of data left to transfer when the error is detected, as depicted in the *ATACB* Command Flow diagram.
00 – Data accesses are halted if a device or phase error is detected.
01 – Phase error conditions are not used to qualify the occurrence of data accesses.
10 – Device error conditions are not used to qualify the occurrence of data accesses.
11 – Neither device error or phase error conditions are used to qualify the occurrence of data accesses.

Bit 2 *PollAltStatOverride* - Poll ALTSTAT Override.
0 – The Alternate Status registered shall be polled until BSY=0 before proceeding with the *ATACB* operation.
1 – Execution of the *ATACB* shall proceed with the data transfer without polling the Alternate Status register until BSY=0.

Bit 1 *DeviceSelectionOverride* - Device Selection Override. This bit shall not be set in conjunction with *bmATACBActionSelect TaskFileRead*.
0 – Device selection shall be performed prior to command register write accesses.
1 – Device selection shall not be performed prior to command register write accesses.

Bit 0 *TaskFileRead* - Read and return the task file register data selected in *bmATACBRegisterSelect*. If *TaskFileRead* is set, the *dCBWDataTransferLength* field must be set to 8.
0 – Execute *ATACB* command and data transfer (if any).
1 – Only task file registers selected in *bmATACBRegisterSelect* shall be read. Task file registers not selected in *bmATACBRegisterSelect* shall not be accessed and 00h shall be returned for the unselected register data.

bmATACBRegisterSelect –
Setting the appropriate bit fields shall cause the taskfile read or write register access to occur. Taskfile read data shall always be 8 bytes in length. Unselected taskfile register data shall be returned as 00h. Taskfile register accesses shall occur in sequential order as shown (Bit 0 first, Bit 7 last). The *bmATACBRegisterSelect* bitmap shall be as defined below.

Bit 0	(3F6h)	Device Control / Alternate Status
Bit 1	(1F1h)	Features / Error
Bit 2	(1F2h)	Sector Count
Bit 3	(1F3h)	Sector Number
Bit 4	(1F4h)	Cylinder Low
Bit 5	(1F5h)	Cylinder High
Bit 6	(1F6h)	Device / Head
Bit 7	(1F7h)	Command / Status

bATACBTransferBlockCount –
This value shall denote the maximum requested block size in 512 byte blocks. This variable shall be set to the value last used for "Sectors per Block" in the SET_MULTIPLE_MODE command. Valid values are 0, 1, 2, 4, 8, 16, 32, 64, and 128 (0 indicates 256 sectors per block). Command failed status shall be returned if an invalid value is detected in the *ATACB*. Non-multiple commands shall set this value to 1 (block size of 512 bytes).

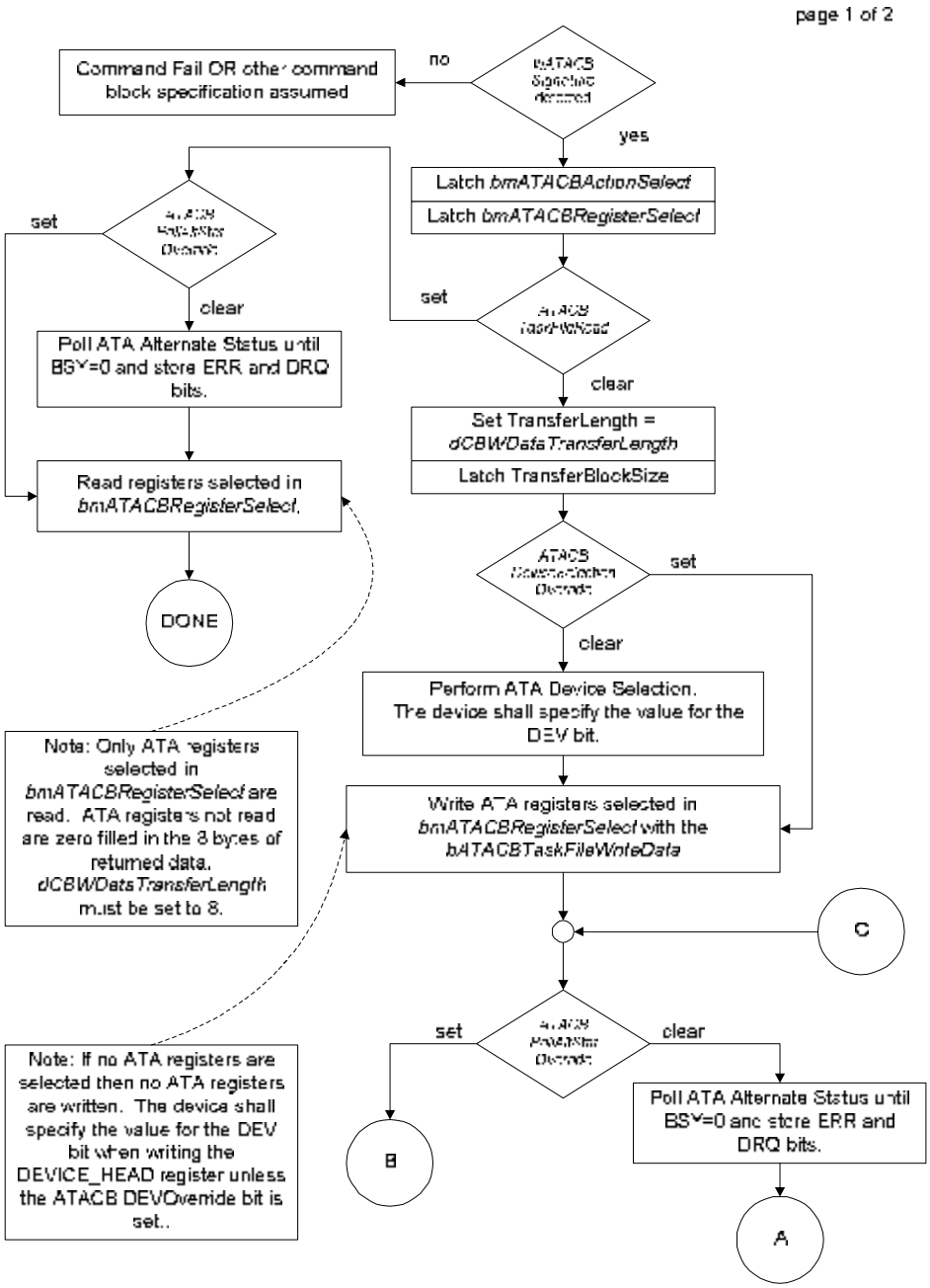
bATACBTaskFileWrtkData –

ATA register data used on ATA command or PIO write operations. Only data entries that have the associated *bmATACBRegisterSelect* bit set shall be required to have valid data.

ATACD Address offset 5h	(3F6h)	Device Control
ATACD Address offset 6h	(1F1h)	Features
ATACD Address offset 7h	(1F2h)	Sector Count
ATACD Address offset 8h	(1F3h)	Sector Number
ATACD Address offset 9h	(1F4h)	Cylinder Low
ATACD Address offset Ah	(1F5h)	Cylinder High
ATACD Address offset Bh	(1F6h)	Device
ATACD Address offset Ch	(1F7h)	Command

ATA Command Flow

Figure 3 shows the flow of ATA commands, specifically the actions taken by the ISD-300A1 based upon how the ATA Command Block is configured.



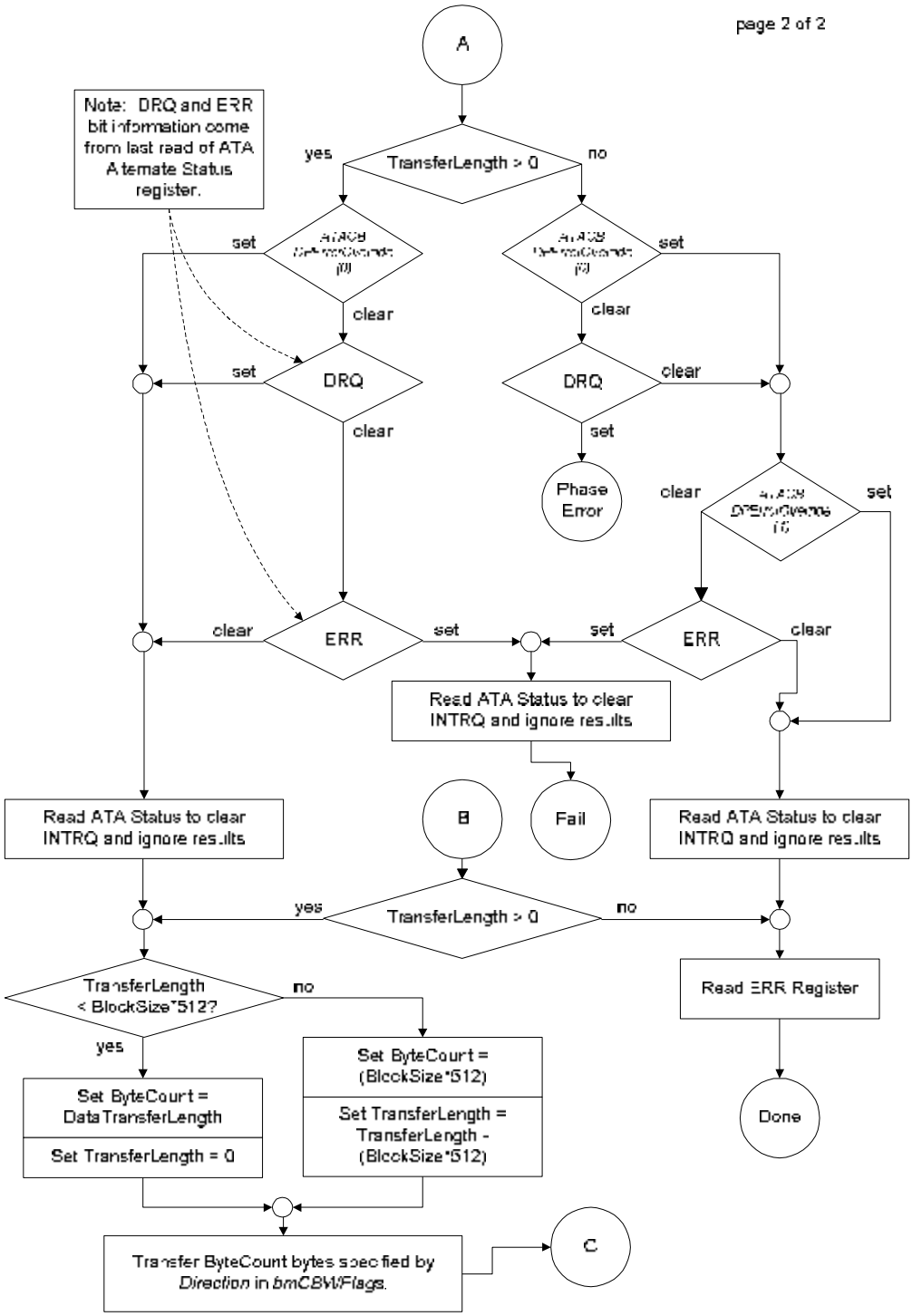


Figure 3– ATA Command Block Flow Diagram

Vendor-Specific ATA Commands

There are two vendor-specific ATA commands implemented in the ISD-300A1. These commands are shown in **Table 16**.

Label	Command Code	Description
IDENTIFY	FBh	This command is used to read ISD-300A1 configuration data and USB descriptor data from an attached mass storage device.
EVENT_NOTIFY	Specified in Configuration Data	This command communicates certain events to the device and is executed as the events occur.

Table 16 – Vendor-Specific ATA Commands

IDENTIFY

The vendor-specific Identify (FBh) command enables the ISD-300A1 to request configuration and USB descriptor information from an attached mass storage device.

Command Code

FBh

Protocol

PIO data-in (refer to *ATA/ATAPI-5 Specification*, section 9.7).

Identification Register Writes

Register	7	6	5	4	3	2	1	0
Feature	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	obs	N/A	obs	DEV	0	0	0	1
Command	FBh							

Table 17 - Identification Register Writes

Device/Head register –

The DEV bit indicates the selected device.

Identification Register Reads

Register	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	N/A							
Cylinder High	N/A							
Device/Head	obs	N/A	obs	DEV	N/A	N/A	N/A	N/A
Status	BSY	N/A	N/A	N/A	DRQ	N/A	N/A	ERR

Table 18 - Identification Register Reads

Device/Head register –
The DEV bit indicates the selected device.

Status register –
BSY shall be cleared to zero upon command completion.
DRDY shall be set to one.
DF (Device Fault) shall be cleared to zero.
DRQ shall be cleared to zero.
ERR shall be cleared to zero.

Device Error Indication
If the device does not support this command, the device shall return command aborted. Otherwise, the device shall not report an error.

Description
When the command is issued, the device sets the BSY bit to one, and prepares to transfer 512 bytes of configuration/descriptor data to the ISD-300A1. *Note: Configuration and descriptor information is limited to 256 bytes in length. Data beyond 256 bytes (bytes 256-511) is read by the ISD-300A1 but ignored.* The device then sets DRQ to one and clears BSY to zero.

The arrangement and meaning of the FDh data bytes are specified in **Table 3**, **Table 7**, **Table 8**, **Table 9**, **Table 10**, and **Table 11**. An example of FDh programming is shown in **Appendix A**.

EVENT_NOTIFY
The vendor-specific Event-notify command enables the ISD-300A1 to communicate the occurrence of certain USB and system events to the attached device.

Command Code
Specified in the ISD-300A1 Configuration Bytes, address 0x2. Programming the command code to 0x00 disables the event-notify feature.

Protocol
Non-data (refer to *ATA/ATAPI-5 Specification*, section 9.9).

Notification Register Writes

Register	7	6	5	4	3	2	1	0
Features	USB Reset	Class Specific Reset	USB Suspend	USB Resume	Cartridge Insert	Cartridge Release	Eject Button Press	Eject Button Release
Sector Count	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	USB High Speed	USB Full Speed
Sector Number	N/A							
Cylinder Low	STATE0							
Cylinder High	STATE1							
Device/Head	N/A							
Command	Specified in the ISD-300A1 Configuration Bytes							

Table 19 – Event Notify ATA Command

Features register –
The USB Reset bit indicates that a USB Reset event has occurred.
The Class Specific Reset bit indicates that an MSC Reset was issued by the host.
The USB Suspend bit indicates that the USB bus has gone into suspend.

The USB Resume bit denotes that the USB bus is no longer in suspend.
The Cartridge Insert bit is set when the device media is inserted.
The Cartridge Release bit is set when the device media is ejected.
The Eject Button Press bit is set when the eject button on the device is pressed.
The Eject Button Release bit is set when the eject button on the device is released.

Sector Count –
The USB Full Speed bit indicates the USB bus is now operating in full speed mode (12 Mbit).
The USB High Speed bit indicates the USB bus is now operating in high speed mode (480 Mbit).

Cylinder Low – STATE0
STATE0 is written with the value of NSTATE0 obtained from the previously completed event notification command. Assertion of NRESET resets STATE0 to 0x00.

Cylinder High – STATE1
STATE1 is written with the value of NSTATE1 obtained from the previously completed event notification command. Assertion of NRESET resets STATE1 to 0x00.

Notification Register Reads

Register	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number	N/A							
Cylinder Low	NSTATE0							
Cylinder High	NSTATE1							
Device/Head	N/A							
Status	BSY	N/A	N/A	N/A	DRQ	N/A	N/A	N/A

Table 20 - Event Notify Drive Status

Cylinder Low – NSTATE0
NSTATE0 is read from the device and stored for use as STATE0 during the next execution of the event notification command. NSTATE0 provides temporary non-volatile storage for devices whose power is controlled by NPWR500 (typically VBUS powered systems). This allows the device to store information prior to entering a USB suspend state for retrieval after resuming from the USB low power state.

Cylinder High – NSTATE1
NSTATE1 is read from the device and stored for use as STATE0 during the next execution of the event notification command. NSTATE0 provides temporary non-volatile storage for devices whose power is controlled by NPWR500 (typically VBUS powered systems). This allows the device to store information prior to entering a USB suspend state for retrieval after resuming from the USB low power state.

Note that a USB reset from the host may interrupt the collection of data. The device must accommodate the potential for this occurrence.

Status register –
BSY shall be cleared to zero upon command completion.
DRQ shall be cleared to zero.

Error Outputs
If the device does not support this command, the device shall return command aborted. Otherwise, the device shall not report an error.

Description
When the event notification command is issued, the ISD-300A1 waits until the device clears BSY and DRQ to zero before beginning register writes. After writing the input registers, the ISD-300A1 waits for BSY and DRQ cleared to zero and then reads the next state information (NSTATE).

The event notification command is issued following every reset of the device and following the power-on reset device initialization sequence. The event notification command is also issued after any of the events reported in the event notification data take place.

If any combination of mating events (mating events are defined as USB HST'S, suspend/resume, cartridge insert/release, eject press/release, and USB/class reset) take place before the ISD-300A1 can issue the event notification command to the device, the following will occur:

1. Send an event notification command showing all events.
2. Send a subsequent event notification command showing only the most recent of any marked events.

If an event notification command does not complete for any reason (such as an incoming reset), the ISD-300A1 will re-issue the command (with any new event data) until it completes successfully. Success of the command does NOT depend upon the ERR bit. If the DRQ bit is set in response to an event notification, the ISD-300A1 will continue to poll (this debug feature makes device incompatibility obvious).

Power Management

The ISD-300A1 is capable of offering two types of system power configurations.

- Self-Powered – VBUS current is limited to 100 mA or less.
- Bus-Powered – VBUS current is limited to 500 mA or less.

The ISD-300A1 dynamically operates in a self or bus powered system depending upon the state of the VBUS_POWERED input.

Control Pins

VBUS_POWERED Pin
The VBUS_POWERED input pin indicates the amount of system current drawn from VBUS. The VBUS powered input is used to qualify:

- The response for a GET_STATUS USB request.
- An ISD-300A1 asynchronous reset in the following cases:
  - If VBUS_POWERED is asserted high and the host has set the USB configuration for self powered operation.
  - If VBUS_POWERED is detected changing state when USB configuration is set to 0.
- Which USB descriptors are presented to the host. If asserted, the first descriptor set is returned. If de-asserted, the second descriptor set is returned.

Setting VBUS_POWERED inactive dictates the system is self powered, drawing up to the value of current returned in the bMaxPower field (100 mA maximum) or less from VBUS. Setting VBUS_POWERED active indicates the system is capable of drawing up to the amount present in the bMaxPower USB descriptor field (500 mA maximum).

DRV_PWR_VALID Pin

The DRV_PWR_VALID input pin is typically enabled only in Hybrid powered systems, or systems in which the ISD-300A1 receives power from VBUS, and the device receives power from another source. In VBUS or self powered systems DRV_PWR_VALID is typically not utilized. In Hybrid powered systems, DRV_PWR_VALID indicates if the device is powered or at least attached and qualifies device operation. DRV_PWR_VALID active polarity and enabling is controlled during ISD-300A1 configuration. It is active high in systems that can supply a power indication from the drive. It is active low in systems that utilize a "grounding scheme" to indicate when the cable is connected to the device. If enabled, and DRV_PWR_VALID is not determined active after the ISD-300A1 configuration data is loaded, the ISD-300A1 enters a low power mode of operation (similar to USB suspend state when in VBUS powered operation. See **Table 21 – ATA Interface Line States** on page 40 for more information). Asserting DRV_PWR_VALID enables resume from the low power operation state.
This signal may also be used in conjunction with ATA_EN to force the ISD-300A1 to disable the USB interface and operate in a low power state when sharing the ATA interface.

VBUS_PWR_VALID Pin

This input pin indicates that VBUS power is present at the USB connector. VBUS_PWR_VALID qualifies driving the system's 1.5K ohm pull-up resistor on D+ when the system is externally powered (the USB specification only allows the device to source power to D+ when the host is powered). After the ISD-300A1 configuration data is loaded, if VBUS_PWR_VALID is inactive the ISD-300A1 enters a low power mode of operation. Asserting VBUS_PWR_VALID resumes operation from the low power state.

DISK_READY Pin

This input pin indicates the attached device is powered and ready to begin communication with the ISD-300A1. DISK_READY qualifies the start of the ISD-300A1's initialization sequence. A state change from 0 to 1 on DISK_READY will cause the ISD-300A1 to wait for 25 ms before asserting NATA_RESET and re-initialize the device. The ATA interface state machines remain inactive and all of the ATA interface signals are driven logic '0' if DISK_READY is not asserted (assuming ATA_EN = '1'). This input is not used in conjunction with DRV_PWR_VALID, and should be tied to logic '1' in hybrid powered systems. DISK_READY is filtered for 25 ms on the rising edge and cleared asynchronously on the falling edge.

NLOWPWR Pin

When active, the NLOWPWR pin indicates the ISD-300A1 is operating in a low power state.

NPWR500 Pin

The NPWR500 output pin indicates the USB host has configured the ISD-300A1 USB interface for VBUS powered operation (VBUS_POWERED pin active), granting the requested amount of power for the peripheral (the bMaxPower entry from descriptor set 1). In the case of a USB suspend condition, NPWR500 is de-asserted and the ISD-300A1 enters a low power state of operation. Upon a resume condition, the ISD-300A1 will resume normal operation and restore NPWR500 accordingly. *Note: ISD-300A1 power sources should not be controlled at any time by using the NPWR500 pin*

ATA Interface Line States

The following table depicts the ATA interface line state dependency with the various controlling input pins.

Control Signals				ATA Interface / Power Management
				VBUS_SUSPEND: DD[15:0], NCS[1:0], DA[2:0], ATA_PD_EN, ATA_PU_EN, NDIOR, NDIOW, NDMACK, NATA_RESET = '0' OPERATIONAL: ATA_PD_EN = '0' ATA_PU_EN = '1' (NCS[1:0], DA[2:0], NDIOR, NDIOW, NDMACK, NATA_RESET = 'Z' when the ATA interface is idle) ATA_HIZ: ATA_PD_EN, ATA_PU_EN, and all other ATA interface signals = 'Z'
NRESET	ATA_EN	DRV_PWR_VALID (1)	DISK_READY	
0	1	X	X	VBUS_SUSPEND state for the ATA interface.
X	0	X	X	ATA_HIZ. All ATA interface signals are 3-stated (hi-Z).
1	1	0	X (=0)	VBUS_SUSPEND state for ATA interface. This is a Hybrid powered application (VBUS powered ISD-300A1, brick powered ATA/ATAPI device)
1	1	1	0	VBUS_SUSPEND state for the ATA interface.
1	1	1	1	OPERATIONAL. VBUS / Brick powered normal operation mode

Notes: (1) DRV_PWR_VALID is active (polarity is correct) OR is disabled by configuration data.

Table 21 – ATA Interface Line States

Operation Control

EJECT, NCART_DET Pins – USB Remote Wakeup and Event Notification

These pins are used to trigger USB remote-wakeup as well as ATA Event Notification. When asserted low EJECT indicates that a media eject request occurred. When asserted low NCART_DET indicates that a media cartridge is present. For EJECT, the pin value must remain static for 10 ms before any state change is detected by internal state machine logic. For NCART_DET, any asynchronous change in state after the signal retains a static value for more than 10 ms is detected by internal state machine logic.

GPIO Pins – General Purpose IO

The GPIO pins enable general purpose IO for miscellaneous use. Each GPIO pin has independent 3-state control, with an internal pull down resistor (50K ohm typically). The GPIO pins input, output, and 3-state control span three bytes of configuration space. The chosen implementation methodology does not allow read and write operations between GPIO[9:8] and GPIO[7:0] to occur during the same clock period.

- During read operations GPIO[9:8] are sampled one clock period (33ns) prior to GPIO[7:0] (assuming the read operation spans all GPIO register space).
- During write operations GPIO[9:8] 3-state control and output values are latched one clock period (33ns) prior to GPIO[7:0] 3-state control and output values (assuming the write operation spans all GPIO register space).

I_MODE Pin – Vendor Specific Identify (FBh) ATA Command (I_MODE)

Asserting the I_MODE pin high enables ISD-300A1 configuration and USB Descriptor data retrieval from an attached device via a vendor specific ATA command (FBh) rather than an external I^2C memory device.

Unlike operation with an external I^2C memory device, I_MODE operation requires the attached device first be initialized and FBh data retrieved before the ISD-300A1 can allow USB enumeration. To meet USB specification requirements, I_MODE operation must be limited to systems that draw 100 mA or less from VBUS prior to USB enumeration.

SYS_IRQ Pin – USB Interrupt

The SYS_IRQ pin provides a way for systems to request service from host software by use of the USB Interrupt pipe. If the ISD-300A1 has no pending interrupt data to return, USB interrupt pipe data requests are NAK'd. If pending data is available, the ISD-300A1 returns 16-bits of data indicating the state of the GPIO[9:0] and DISK_READY pins. **Table 22** and **Figure 4** depicts the bit map and latching algorithm incorporated by the ISD-300A1.

USB Interrupt Data Byte 1 Bit Map								USB Interrupt Data Byte 0 Bit Map							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0	0	0	0	0	DISK_READY	GPIO[9]	GPIO[8]	GPIO[7]	GPIO[6]	GPIO[5]	GPIO[4]	GPIO[3]	GPIO[2]	GPIO[1]	GPIO[0]

Table 22 – USB Interrupt Pipe Data

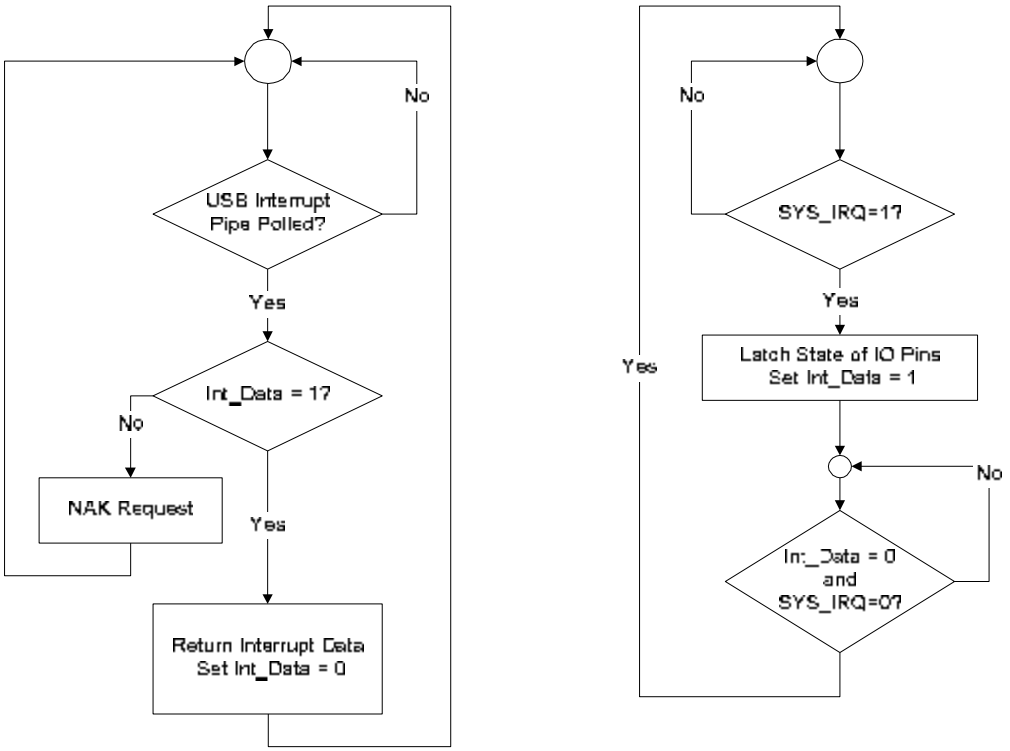


Figure 4 – SYS_IRQ – USB Interrupt Pipe

ATA_EN Pin – ATA Interface Disabled

The ATA_EN pin allows ATA bus sharing with other host devices. Asserting ATA_EN low causes the ISD-300A1 to 3-state all ATA bus interface pins hi-Z and suspend ATA state machine activity, otherwise leaving the ISD-300A1 operational (USB operation continues). Asserting ATA_EN high resumes normal operation.

To disable USB operation and the ATA interface, the DRIVE_PWR_VALID signal can be used in conjunction with ATA_EN to force the ISD-300A1 into a low power state until normal operation is resumed.

ATA_PU_EN Pin – ATA Interface Pull-up Resistor Source

This output provides control for the required host pull-up resisters on the ATA interface. ATA_PU_EN is 3-stated hi-Z when ATA_EN is low.

ATA_PD_EN Pin – ATA Interface Pull-down Resistor Sink

This output provides control for the required host pull-down resistors on the ATA interface. ATA_PD_EN is 3-stated hi-Z when ATA_EN is low.

TEST<3:0> Pins - Test Modes

TEST(3:0)	Mode Description
0000	**Normal Mode** - This is the default mode of operation, or run time mode. Pull-downs are on.
0001	**Normal Mode XCVR Muxout** – debug mode 1. See **XCVR Mux-out Mode** below.
0010	**Limbo** - Setting this mode disables most outputs. See **Limbo** Mode below.
0011	**Input NandTree** – Allows board level manufacturing tests. See **Input NandTree Mode** below.
0100	**Bi-di NandTree** – Allows board level manufacturing tests. See **Bi-di NandTree Mode** below.
0101	**SimTest** – HDL simulation only test mode. Specific GPIO pins are multiplexed in this mode of operation: Short Timers GPIO[2] Short SRAM GPIO[1] Skip identify GPIO[0]
0110	**Scan Mode** – Fab only test mode
0111	**Reserved**
1000	**Normal Mode XCVR Mux-out** – ASIC debug mode 2. See **XCVR Mux-out Mode**.
1001	**Normal Mode XCVR Mux-out** – ASIC debug mode 3. See **XCVR Mux-out Mode**.
1010	**Normal Mode XCVR Mux-out** – ASIC debug mode 4. See **XCVR Mux-out Mode**.
1011	**Test Bus** – SERDES Fab only test mode
1100	**Test Bus** – ROM Fab only test mode
1101	**Test Bus** – 256x8 SP SRAM. Fab only test mode
1110	**Test Bus** – 32x16 DP SRAM. Fab only test mode
1111	**Test Bus** - 4Kx16 DP SRAM. Fab only test mode

Table 23 – Test Modes

XCVR Mux-out Mode

These modes of operation are similar to the Normal Mode of operation with various internal transceiver logic signals brought out through the GPIO and LED pins. These modes are intended only for Cypress ASIC qualification. The table below shows the mux-out scheme for each mode of operation.

Pin #	ISD-300A1 Pin Name	Mode 1 – XCVR signal	Mode 2 – XCVR signal	Mode 3 – XCVR signal	Mode 4 – XCVR signal
38	GPIO0	RXERROR	IESDRVON	TXREADY	PUE
39	GPIO1	RXBUSAC	CDRCLKLN	TXVALID	CLRXVM
40	GPIO2	RXDOUT(0)	CLK_30	TXDIN(0)	CLRSVP
42	GPIO3	RXDOUT(1)	CLK_60	TXDIN(1)	CLRXISE0
44	GPIO4	RXDOUT(2)	LPBACK	TXDIN(2)	CLRSDATA
45	GPIO5	RXDOUT(3)	LPBACK0	TXDIN(3)	CNEN
46	GPIO6	RXDOUT(4)	LOCK	TXDIN(4)	CLRCVEN
47	GPIO7	RXDOUT(5)	IOST1	TXDIN(5)	CLTXOEN
48	GPIO8	RXDOUT(6)	IOST0	TXDIN(6)	CLTXOSE0
49	GPIO9	RXDOUT(7)	IISRCVEN	TXDIN(7)	CLTXDATA
94	NLED1	RXLSTBYT	0	RXACTIVE	CONTJ
95	NLED0	RXVALID	PWRDOWN_XCVR	TXBUSACT	CONTK

Limbo Mode

This mode of operation is provided to aid debug in manufacturing environments. The ISD-300A1 3-states (high Z) all output pins during Limbo mode operation with the exception of the XO pin. The XO pin output cell does not have 3-state control (always enabled), and thus must be disabled / disconnected by other means.

Input NandTree Mode

This mode tests the connectivity of all inputs and outputs. While in the Input NandTree Mode of operation, all bi-directional pins are wired as chain outputs. The results of the connectivity procedure will be seen on all bi-directional pins. The list below shows the connectivity order of the Input NandTree chain (beginning to end).

Chain inputs:
BUS_PWR_VALID,
VBUS_POWERED,
DRV_PWR_VALID,
DISK_READY,
SYS_IRQ,
DMARQ,
IORDY,
NCARD_DET,
NEJECT,
NRESET,
I_MODE,
ATA_EN

Chain outputs:
GPIO[9:0], DD[15:0], SDA

Bi-di NandTree Mode

This mode test the connectivity of all bi-directional inputs. While in the Bi-di NandTree Mode of operation, all bi-directional pins are wired as inputs and become part of the NandTree chain. The results of the connectivity procedure will be seen on all output only pins. The list below shows the connectivity order of the Bi-di NandTree chain (beginning to end).

Chain inputs:
GPIO[0:9]. Note: GPIO[0] first, GPIO[9] last
DD[15], DD[0], DD[14], DD[1], DD[13], DD[2], DD[12], DD[3], DD[11], DD[4], DD[10], DD[5], DD[9], DD[6], DD[8], DD[7].

Chain outputs:
NLED[1:0], NPWRSW, NATA_RESET, NDIOW, NDIOR, NDMACK, ATA_PU_EN, ATA_PD_EN, NCS[1:0], DA[2:0], NLOWPWR, SCL

Pin connectivity in both NandTree modes can be tested with the following procedure:

1. Set all inputs on the chain to '1'. Outputs will be '1'.
2. Set first input to '0'. Outputs will toggle
3. Set first input back to '1'. Outputs will toggle.
4. Set '0' on the NandTree chain inputs from second input to the end of the chain (in order). The outputs will toggle with each input toggle, testing pad / IO cell connectivity.

Manufacturing Test Mode

This mode of operation is provided for interconnect test in a manufacturing environment. During Manufacturing Test Mode operation, all outputs not associated directly with USB operation are controllable. Normal state machine and register control of output pins is disabled. ISD-300A1 input pins not associated directly with USB operation can be sampled at any time during normal or Manufacturing Test Mode operation.

Vendor specific USB commands are used to enable and control Manufacturing Test Mode operation and to sample input pin states. See **Vendor-Specific Requests** for more details on the LOAD_MFG_DATA and READ_MFG_DATA USB commands.

External Circuitry

USB, Crystal, and I²C Interface Connections

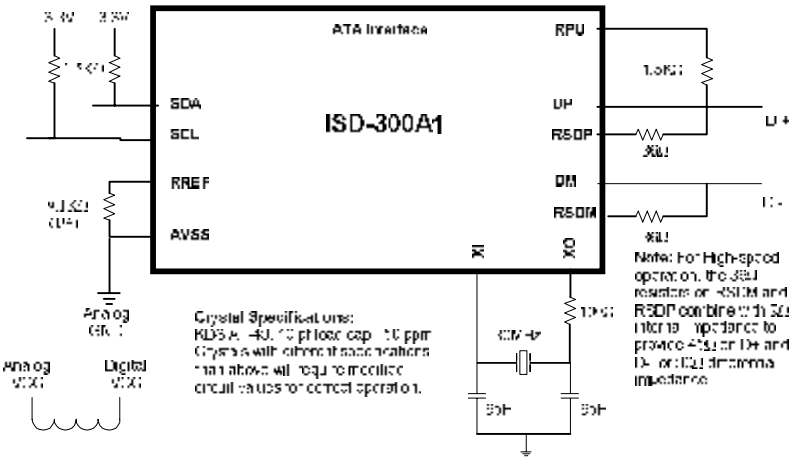


Figure 5 – External Components connection

ATA Interface Considerations

1K Ohm Pull-down Resistor On DD<7>

For "slave" devices, a 1K ohm pull-down resistor must be utilized on DD7 for ISD-300A1 based designs. This is required for proper operation of the ISD-300A1 master/slave device auto detection algorithm. If this modification is omitted, slave devices will take an excessive amount of time to initialize (around 30 seconds). In systems with only master devices this modification may be omitted.

ATA_PD_EN and ATA_PU_EN Usage In Self Powered Systems

These signals are controlled by ATA_EN, DRV_PWR_VALID, and DISK_READY. If these inputs are static, the ATA_Px_EN outputs can be left unconnected and the pull-up and pull-down resistors that normally connect to these outputs can be directly tied to the appropriate power rails.

ATA Interface Termination

Design practices as outlined in the *ATA/ATAPI-5 Specification* for signal integrity should be followed with systems that utilize a ribbon cable interconnect between the ISD-300A1 ATA interface and the device, especially if Ultra Mode DMA is utilized.

3.3V Power Regulation

In systems where the ATA/ATAPI device remains powered during ISD-300A1 low power operation (such as USB suspend state), the system design must insure the ISD-300A1 3.3V supply is not "back powered" through IO cell leakage current from the device's 5V ATA interface, raising the supply rail above safe operating limits. Typically this may be accomplished by utilizing a 1.5K ohm resistive current sink between the 3.3V supply and ground.

VBUS Powered System Considerations

GPIO Internal Pull Down Resistors

All ISD-300A1 GPIO IO cells incorporate an internal pull down resistor (50K ohm typical). The system must insure the GPIO interface is at logic '0' to eliminate current draw during the USB suspend state.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Symbol	Parameter	Min	Max	Units
VDD	3.3 V IO Supply	-0.5	1.0	Volts
Vin	Input Pin Voltage	-0.5	5.5	Volts
Ta	Ambient Operating Temperature Range	–40°	85°	Celsius
Tstrg	Storage Temperature	-65	150	Celsius

Table 24 – Absolute Maximum Ratings

Electrical Characteristics

Voltage Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Low	V_{IL}	—	—	—	0.8	V
Input Voltage High	V_{IH}	—	2.0	—	—	V
Output Voltage Low	V_{OL}	—	—	—	0.4	V
Output Voltage High	V_{OH}	—	2.4	3.3		V
Power Supply Voltage	V_{DDxx}	—	3.0	3.3	3.6	V

Note: (T_A = 20 °C, V_{DDxx} = 3.3 V ± 10%, V_{SS} = 0 V)

Table 25 – Voltage Characteristics

Operation Current Parameters - Typical	
High Speed V_{DD} supply current (I_{CC}) – Idle	180 mA (typ)
High Speed V_{DD} supply current (I_{CC}) – Active	< 200 mA (typ)
Full Speed V_{CC} supply current (I_{DD}) – Idle	121 mA (typ)
Full Speed V_{CC} supply current (I_{DD}) – Active	< 135 mA (typ)
Supply current w/ nRESET asserted	30mA (typ)
Low power w/ USB remote wakeup enabled	2.7 mA (typ)
Low power w/o USB remote wakeup enabled	< 20 µA (typ)

Note: (T_A = 20 °C, V_{CC} = 3.3 V ± 10%, V_{SS} = 0 V)

Table 26 – Power Supply Current Characteristics

Timing Characteristics

I²C Memory Device Interface Timing

The I²C memory device interface supports a subset of the I²C "slow mode" specification implementation document. Timing specifics are given below.

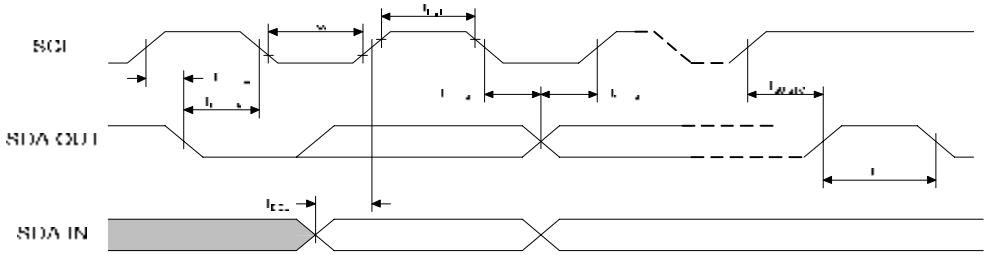


Figure 6 – I²C Memory Device Interface Timing

I²C Parameter	Symbol	Value
Clock high time	T_{CKH}	5066 ns
Clock low time	T_{CKL}	5066 ns
Start condition hold time	$T_{HD:STA}$	5066 ns
Start condition setup time	$T_{SU:STA}$	5066 ns
Data output hold time	$T_{HD:DAT}$	5066 ns
Data output setup time	$T_{SU:DAT}$	5066 ns
Stop condition setup time	$T_{SU:STO}$	5066 ns
Required data valid before clock	T_{DSU}	500 ns
Min time bus must be free before next transmission	t_{BUF}	5066 ns

Table 27 – I²C Memory Device Interface Timing

SYS_IRQ Interface Timing

The timing specifications for SYS_IRQ relative to the USB interrupt pipe data are given below.

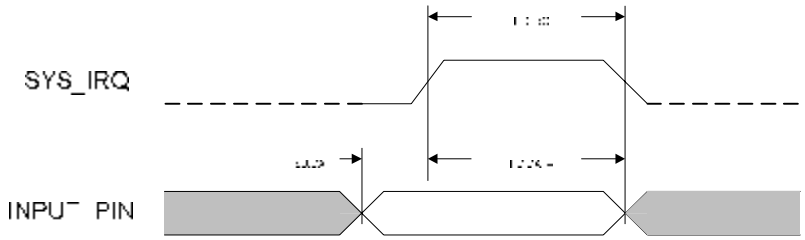


Figure 7 – SYS_IRQ Interface Timing

SYS_IRQ Parameter	Symbol	Value
Interrupt pipe data set-up time	T_{SU_DATA}	0 ns
SYS_IRQ hold time	T_{HLD_IRQ}	150 ns
Interrupt pipe data hold time	T_{HLD_DATA}	150 ns

Table 28 – SYS_IRQ Interface Timing

ATA/ATAPI Port Timing Characteristics

All input signals on the ATA/ATAPI port are considered asynchronous, and are synchronized to the chip's internal system clock. All output signals are clocked using the chip's internal system clock, for which there is no external reference. Thus, the output signals should be considered asynchronous. The PIO mode used for data register accesses is retrieved from the device or specified in the ISD-300A1 configuration bytes.

Clock

Crystal	Frequency	Duty Cycle
KDS AT-49 crystal, 10pf load capacitance.	30 MHz ± 0.005%	n/a

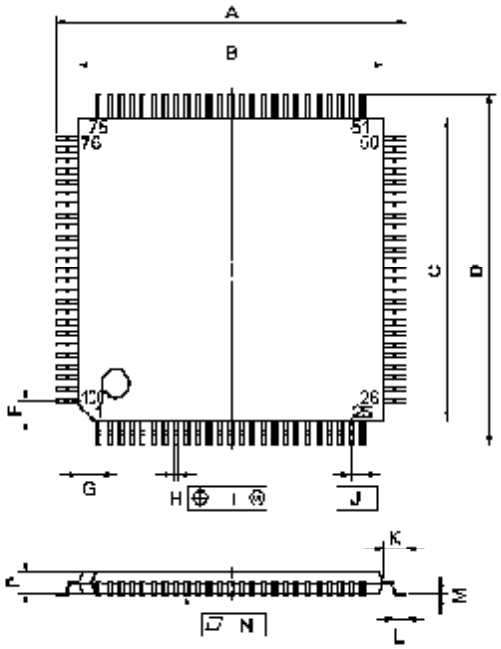
Note: Clock signal frequency is measured at $V_{DDPW}/2$ point. Rise and fall times should be 2 ns or less.

Table 29 – Clock Requirements

Reset

The ISD-300A1 requires an off-chip power-on reset circuit. NRESET must be held asserted for a minimum of 1 ms after power is stable.

Physical Diagrams



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) at its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	$0.22^{+0.05}_{-0.04}$	$0.009^{+0.002}_{-0.002}$
	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.008}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.008}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.0±0.1	$0.039^{+0.005}_{-0.004}$
Q	0.1±0.05	0.004±0.002
R	$3^{+7}_{-3}°$	$3^{+7}_{-3}°$
S	1.27 MAX.	0.050 MAX.

S100GC-50-8BU-1

Figure 8 – Package Outline Diagram

Appendix A – Example EEPROM or FBh Identify Data Contents

Address	Field Name	Description	Example SROM Data
ISD-300A1 Configuration Data			
0x0 (Byte 0)	PC memory device Signature (lsb)	lsb PC memory device Signature byte. Register does not exist in HW	0x54
0x1 (Byte 1)	PC memory device Signature (msb)	msb PC memory device Signature byte. Register does not exist in HW	0x4D
0x2 (Byte 0)	Event Notification	ATAPI event notification command. Setting this field to 0x00 disables this feature.	0xFC
0x3 (Byte 1)	APM Value	Bit(7:0) ATA Device Advanced Power Management Value. If an attached ATA device supports APM and this field contains other than 0x00, the Initialization state machines will issue a SET FEATURES command to Enable APM with the register value during the drive initialization process. Setting APM Value to 0x00 disables this function ality. This register value is ignored with ATAPI devices.	0x00
0x4	ATA Initialization Timeout	Time in 128 millisecond granularity before the ISD-300A1 stops polling the ALT STAT register for reset complete and restarts the reset process (0x80 = 16.4 seconds).	0x80

Address	Field Name	Description	Example SROM Data
0x5	USB Bus Mode	Bit (7) – read only. USB bus mode of operation 0 USB bus is operating in full speed mode (12 Mbit/sec). 1 USB bus is operating in high speed mode (480 Mbit/sec).	0x00
	ATAPI Command Block Size	Bit (6) CBW Command Block Size 0 12 byte ATAPI CB 1 16 byte ATAPI CB	
	Master/Slave Selection	Bit (5) Device number selection. This bit is valid only when "Skip ATA/ATAPI Device Initialization" is active. Under ISD-300A1 control ("Skip ATA/ATAPI Device Initialization" = '0'), the value is ignored. 0 Drive 0 (master) 1 Drive 1 (slave)	
	ATAPI Reset	Bit (4) ATAPI reset during drive initialization. Setting this bit enables the ATAPI reset algorithm in the drive initialization state machines	
	ATA /ATAPI	Bit (3) – read only. Indicates if an ATA or ATAPI device is detected 0 ATAPI device 1 ATA device or possible device initialization failure.	
	Force USB FS	Bit (2) Force USB full speed only operation. Setting this bit prevents the ISD-300A1 from negotiating HS operation during USB reset events 0 Normal operation – allow HS negotiation during USB reset 1 USB FS only – do not allow HS negotiation during USB reset	
	VS / MSC SOFT_RESET	Bit (1) Vendor Specific / MSC SOFT_RESET control 0 Vendor Specific USB command utilized for SOFT_RESET 1 Mass Storage Class USB command utilized for SOFT_RESET	
	DISK_READY Polarity	Bit (0) DISK_READY active polarity. DISK_READY Polarity is ignored if I_MODE is set to 1. During I_MODE operation DISK_READY polarity is active high. 0 Active high polarity 1 Active low polarity	
0x6	ATA Command Designator (Byte 0, lsb)	Value in CBW CB field that designates if the CB is decoded as vendor specific ATA commands instead of the ATAPI command block.	0x21
0x7	ATA Command Designator (Byte 1, msb)	Value in CBW CB field that designates if the CB is decoded as vendor specific ATA commands instead of the ATAPI command block.	0x21

Address	Field Name	Description	Example SROM Data
0x8	Initialization Status	Bit (7) – read only Drive Initialization Status If set, indicates the drive initialization sequence state machine is active	0x00
	Force ATA Device	Bit (6) Allows software to manually enable ATA Translation with devices that do not support ISD-300A1 device initialization algorithms. *Note: Force ATA Device must be set '1' in conjunction with Skip ATA/ATAPI Device Initialization and ATA Translation Enable.* Software must issue an INQUIRY command followed with a MSC reset to allow the ISD-300A1 to parse drive information and optimize system performance and operation. Force ATA Device should be set '0' for devices that support ISD-300A1 device initialization algorithms.	
	Skip ATA / ATAPI Device Initialization	Bit (5) Skip_Init. This bit should be cleared for I_MODE operation. The host driver must initialize the attached device (if required) when this bit is set. *Note: for ATAPI devices, if Skip_Init is set the host driver must issue an INQUIRY command utilizing ATAC0h to allow the ISD-300A1 to parse drive information to optimize system performance and operation. Refer to bmATACommandSet in the* ATA Command Block - **Field Descriptions** *section on page 30 for further information.* 0 normal operation 1 only reset the device and write the device control register prior to processing commands.	
	Obsolete	Bit (4:3) – Shall be set to '0'	
	Last LUN Identifier	Bits (2:0) Maximum number of LUNs device supports.	
0x9	ATA_EN	Bits (7) – read only. Current logic state of the ATA_EN pin	0x01
	Obsolete	Bit (6:1) – Should be set to 0	
	SRST Enable	Bit (0) SRST reset during drive initialization. Setting this bit enables the SRST reset algorithm in the drive initialization state machines.	
0xA	ATA Data Assert	Bits (7:4) Standard values for ATA compliant devices and a 30.0 MHz system clock (in binary). *Note: These values are only valid when the Override PIO Timing configuration bit is set.* mode 0 0101 (5−1)*33.33 = 200 ns mode 1 0011 (3−1)*33.33 = 133 ns mode 2 0011 (3−1)*33.33 = 133 ns mode 3 0010 (2−1)*33.33 = 100 ns mode 4 0010 (2−1)*33.33 = 100 ns	0x20
	ATA Data Recover	Bits (3:0) ATA cycle times are calculated using Data Assert and Data Recover values. Standard recover values and cycle times for ATA compliant devices and a 30.0 MHz system clock (in binary). *Note: These values are only valid when the Override PIO Timing configuration bit is set.* mode 0 1100 (4−1)+(12+1)*33.33 = 600 ns mode 1 0111 (3−1)+(7−1)*33.33 = 400 ns mode 2 0011 (2−1)+(3−1)*33.33 = 233 ns mode 3 0010 (2−1)+(2−1)*33.33 = 200 ns mode 4 0000 (2−1)+(0−1)*33.33 = 133 ns	

Address	Field Name	Description	Example SROM Data
0x1B	ATA Data Setup	Bits (7:5) Setup time is only incurred on the first data cycle of a burst. Standard values for ATA compliant devices and a 30.0 MHz system clock are (in binary): *Note: These values are only valid when the Override PIO Timing configuration bit is set.* mode 0 010 (2+1)*33.33 = 132 ns mode 1 001 (1+1)*33.33 = 66 ns mode 2 001 (1+1)*33.33 = 66 ns mode 3 001 (1+1)*33.33 = 66 ns mode 4 000 (0+1)*33.33 = 33 ns	0x600
	Drive Power Valid Polarity	Bit (4) Controls the polarity of DRV_PWR_VALID pin 0 Active low ("connected to ground" indication) 1 Active high (power indication from device)	
	Override PIO Timing	Bit (3) This field is used in conjunction with ATA Data Setup, ATA Data Assertion, ATA Data Recovery, and PIO Mode Select bit fields. 0 Use timing information acquired from the Drive 1 Override device timing information with configuration values	
	Drive Power Valid Enable	Bit (2) Enable for the DRV_PWR_VALID pin. Drive Power Valid should only be enabled in cable applications where the ISD-300A1 is VBUS powered. 0 pin disabled (most systems) 1 pin enabled	
	ATA Read Kludge	Bit (1) PIO data read 3-state control. Enabling this will 3-state (hi-Z) the ATA data bus during PIO read operations while addressing the data register. In most applications this bit is set to '0'. This functionality is provided as a solution for devices that erroneously drive the ATA data bus continuously during PIO data register reads. 0 Normal operation as per ATA/ATAPI interface specification. 1 3-state (hi-Z) LDI[15:0] during PIO data register reads.	
	I_MODE	Bit (0) – read only This bit reflects the current state of the I_MODE input pin.	

Address	Field Name	Description	Example SROM Data
0xC	SYS_IRQ	Bit7) – read only This bit reflects the current logic state of the SYS_IRQ input.	0x32
	DISK_READY	Bit6) – read only This bit reflects the current logic state of the DISK_READY input.	
	ATA Translation Enable	Bit5) Enable ATAPI to ATA protocol translation enable. If enabled, AND if an ATA device is detected, ATA translation is enabled. *Note: If Skip ATA/ATAPI Device Initialization is set '1', Force ATA Device must also be set '1' in order to utilize ATA translation. Software must further issue an IDQUERY command followed with an IDRST reset to enable ATA translation operation.* 0 ATA Translation Disabled 1 ATA Translation Enable	
	ATA UDMA Enable	Bit4) Enable Ultra Mode data transfer support for ATA devices. If enabled, AND the ATA device reports UDMA support, the ISD-300A1 will utilize UDMA data transfers. 0 Disable ATA device UDMA support 1 Enable ATA device UDMA support	
	ATAPI UDMA Enable	Bit3) Enable Ultra Mode data transfer support for ATAPI devices. If enabled, AND the ATAPI device reports UDMA support, the ISD-300A1 will utilize UDMA data transfers. 0 Disable ATAPI device UDMA support 1 Enable ATAPI device UDMA support	
	ROM UDMA Mode	Bits2:0) ROM UDMA Mode indicates the highest UDMA mode supported by the product. The ISD-300A1 will utilize the lesser of ROM UDMA Mode or the highest mode supported by the device. *Note: UDMA read operation needs timing is controlled by the device.* mode 0 000 153.3 ns per 16-bit word write mode 1 001 100 ns per 16-bit word write mode 2 010 66.7 ns per 16-bit word write mode 3 011 66.7 ns per 16-bit word write mode 4 100 33.3 ns per 16-bit word write	

Address	Field Name	Description	Example SROM Data
0xD	PIO Mode Selection	Bits (7:5) PIO Mode Selection. The PIO mode reported back to the device if the Override PIO Timing configuration bit is set. This field represents the PIO mode of operation configured by the ATA Data Setup, ATA Data Assertion, ATA Data Recover, and Override PIO Timing fields. mode 0 000 mode 1 001 mode 2 010 mode 3 011 mode 4 100	0x23
	Skip Pin Reset	Bit (4) Skip ATA_NRESET assertion. *Note: Soft Enable must be set in conjunction with Skip Pin Reset.* Setting this bit causes the Initialize algorithm to bypass ATA_NRESET assertion unless a drive Power On Reset cycle occurred, utilizing SRST as the drive reset mechanism. 0 Allow ATA_NRESET assertion 1 Disable ATA_NRESET assertion	
	General Purpose IO	Bits (3:2) GPIO[3:2] input / output control Writing this register controls the output state of the GPIO pin (if the 3-state control is enabled) Reading this register returns the logic value from the GPIO pin	
	General Purpose IO 3-state control	Bits (1:0) GPIO[3:2] 3-state control 0 Output enabled (GPIO pin is an output) 1 3-state (hi-Z) (GPIO pin is an input)	
0xE	General Purpose IO	Bits(7:0) GPIO[7:0] input / output control Writing this register controls the output state of the GPIO pin (if the 3-state control is enabled) Reading this register returns the logic value from the GPIO pin	0x00
0xF	General Purpose IO 3-state control	Bits(7:0) GPIO[7:0] 3-state control 0 Output enabled (GPIO pin is an output) 1 3-state (hi-Z) (GPIO pin is an input)	0xFF
USB Device Descriptor			
0x10	bLength	Length of device descriptor in bytes.	0x12
0x11	bDescriptor Type	Descriptor type.	0x01
0x12	bcdUSB (LSB)	USB Specification release number in BCD.	0x00
0x13	bcdUSB (MSB)		0x02
0x14	bDeviceClass	Device class.	0x00
0x15	bDeviceSubClass	Device subclass.	0x00
0x16	bDeviceProtocol	Device protocol.	0x00
0x17	bMaxPacketSize0	Maximum USB packet size supported	0x40
0x18	idVendor (LSB)	Vendor ID.	0xAB
0x19	idVendor (MSB)		0x05
0x1A	idProduct (LSB)	Product ID.	0x80
0x1B	idProduct (MSB)		0x00
0x1C	bcdDevice (LSB)	Device release number in BCD lsb (product release number)	0x00
0x1D	bcdDevice (MSB)	Device release number in BCD msb (silicon release number). NOTE: *This field entry is always returned from internal ROM contents, regardless of the descriptor source.*	0x10
0x1E	Manufacturer	Index to manufacturer string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x19

Address	Field Name	Description	Example SROM Data
0x1F	iProduct	Index to product string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x5A
0x20	iSerialNumber	Index to serial number string. This entry must equal half of the address value where the string starts or 0 if the string does not exist. *The USB Mass Storage Class Bulk-Only Transport Specification requires a unique serial number.*	0x61
0x21	bNumConfigurations	Number of configurations supported.	0x01
		USB Device Qualifier Descriptor	
0x22	bLength	Length of device descriptor in bytes.	0x0A
0x23	bDescriptor Type	Descriptor type.	0x06
0x24	bcdUSB (LSB)	USB Specification release number in BCD.	0x00
0x25	bcdUSB (MSB)		0x02
0x26	bDeviceClass	Device class.	0x00
0x27	bDeviceSubClass	Device subclass.	0x00
0x28	bDeviceProtocol	Device protocol.	0x00
0x29	bMaxPacketSize0	Maximum USB packet size supported	0x40
0x2A	bNumConfigurations	Number of configurations supported	0x01
0x2B	bReserved	Reserved for future use, must be zero	0x00
		USB Standard Configuration Descriptor 1	
0x2C	bLength	Length of configuration descriptor in bytes.	0x09
0x2D	bDescriptorType	Descriptor type.	0x02
0x2E	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27
0x2F	bTotalLength (MSB)		0x00
0x30	bNumInterfaces	Number of interfaces supported. The ISD-300A1 only supports one interface.	0x01
0x31	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. This value must be set to 0x02	0x02
0x32	iConfiguration	Index to the configuration string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x00
0x33	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On-board default 7 Reserved. '1' 6 Self-powered. '1' 5 Remote wake-up. '0' 4-0 Reserved, set to 0. '0'	0x80
0x34	bMaxPower	Maximum power consumption for this configuration. Units used are mA*2 (i.e. 0x31 = 98 mA, 0x99 = 498 mA).	0x09
		USB Other Speed Configuration Descriptor 1	
0x35	bLength	Length of configuration descriptor in bytes.	0x09
0x36	bDescriptorType	Descriptor type.	0x07
0x37	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interfaces and endpoint descriptors.	0x27
0x38	bTotalLength (MSB)		0x00
0x39	bNumInterfaces	Number of interfaces supported. The ISD-300A1 only supports one interface.	0x01
0x3A	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. This value must be set to 0x02	0x02
0x3B	iConfiguration	Index to configuration string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x00
0x3C	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On-board default 7 Reserved. '1' 6 Self-powered. '1' 5 Remote wake-up. '0' 4-0 Reserved, set to 0. '0'	0x80

Address	Field Name	Description	Example SROM Data
0x30	bMaxPower	Maximum power consumption for the second configuration. Units used are mA*2 (i.e. 0x31 = 98 mA, 0xF9 = 498 mA).	0x09
USB InterFace Descriptor (HS)			
0x32	bLength	Length of interface descriptor in bytes.	0x09
0x33	bDescriptorType	Descriptor type.	0x04
0x40	bInterfaceNumber	Interface number.	0x00
0x41	bAlternateSettings	Alternate settings	0x00
0x42	bNumEndpoints	Number of endpoints	0x03
0x43	bInterfaceClass	Interface class.	0x08
0x44	bInterfaceSubClass	Interface subclass.	0x06
0x45	bInterfaceProtocol	Interface protocol.	0x50
0x46	iInterface	Index to first interface string. This entry must equal half of the address value where the string starts or zero if the string does not exist.	0x00
USB Bulk Out (HS)			
0x47	bLength	Length of this descriptor in bytes.	0x07
0x48	bDescriptorType	Endpoint descriptor type.	0x05
0x49	bEndpointAddress	This is an Out endpoint, endpoint number 1.	0x01
0x4A	bmAttributes	This is a bulk endpoint.	0x02
0x4B	wMaxPacketSize (lsb)	Max data transfer size.	0x00
0x4C	wMaxPacketSize (msb)		0x02
0x4D	bInterval	HS interval for polling (max NAK rate)	0x01
USB Bulk In (HS)			
0x4E	bLength	Length of this descriptor in bytes.	0x07
0x4F	bDescriptorType	Endpoint descriptor type.	0x05
0x50	bEndpointAddress	This is an In endpoint, endpoint number 2.	0x82
0x51	bmAttributes	This is a bulk endpoint.	0x02
0x52	wMaxPacketSize (LSB)	Max data transfer size.	0x00
0x53	wMaxPacketSize (MSB)		0x02
0x54	bInterval	HS interval for polling (max NAK rate). Does not apply to FS bulk endpoints.	0x01
USB Interrupt (HS)			
0x55	bLength	Length of this descriptor in bytes.	0x07
0x56	bDescriptorType	Endpoint descriptor type.	0x05
0x57	bEndpointAddress	This is an Interrupt endpoint, endpoint number 3.	0x83
0x58	bmAttributes	This is an interrupt endpoint	0x03
0x59	wMaxPacketSize (LSB)	Max data transfer size.	0x02
0x5A	wMaxPacketSize (MSB)		0x00
0x5B	bInterval	This is the polling interval. 0x0A = 64ms.	0x0A
0x5C		Unused I2C memory device / internal ROM space for address pointer alignment	0x00
USB Interface Descriptor (FS)			
0x5D	bLength	Length of interface descriptor in bytes.	0x09
0x5E	bDescriptorType	Descriptor type.	0x04
0x5F	bInterfaceNumber	Interface number.	0x00
0x60	bAlternateSettings	Alternate settings	0x00
0x61	bNumEndpoints	Number of endpoints	0x03
0x62	bInterfaceClass	Interface class.	0x08
0x63	bInterfaceSubClass	Interface subclass.	0x06
0x64	bInterfaceProtocol	Interface protocol.	0x50

Address	Field Name	Description	Example SROM Data
0x65	Interface	Index to first interface string. This entry must equal half of the address value where the string starts or zero if the string does not exist.	0x00
		USB Bulk Out (FS)	
0x66	bLength	Length of this descriptor in bytes.	0x07
0x67	bDescriptorType	Endpoint descriptor type.	0x05
0x68	bEndpointAddress	This is an Out endpoint, endpoint number 1.	0x01
0x69	bmAttributes	This is a bulk endpoint.	0x02
0x6A	wMaxPacketSize (lsb)	Max data transfer size.	0x40
0x6B	wMaxPacketSize (msb)		0x00
0x6C	bInterval	Interval for polling	0x00
		USB Bulk In (FS)	
0x6D	bLength	Bulk In descriptor length	0x07
0x6E	bDescriptorType	Descriptor type	0x05
0x6F	bEndpointAddress	Endpoint address	0x82
0x70	bmAttributes	Attributes	0x02
0x71	wMaxPacketSize (lsb)	Max packet size lsb	0x40
0x72	wMaxPacketSize (msb)	Max packet size msb	0x00
0x73	bInterval	Interval for polling	0x00
		USB Interrupt (FS)	
0x74	bLength	Interrupt descriptor length	0x07
0x75	bDescriptorType	Descriptor type	0x05
0x76	bEndpointAddress	Endpoint address	0x83
0x77	bmAttributes	Attributes	0x03
0x78	wMaxPacketSize (lsb)	Max packet size lsb	0x02
0x79	wMaxPacketSize (msb)	Max packet size msb	0x00
0x7A	bInterval	Interval for polling	0x40
0x7B		Unused I2C memory device / internal ROM space for address pointer alignment	0x00
		USB String Descriptor (LANGID)	
0x7C	bLength	LANGID descriptor length	0x04
0x7D	bDescriptorType	Descriptor type	0x03
0x7E	LANGID (lsb)	Language supported lsb	0x09
0x7F	LANGID (msb)	Language supported msb	0x04
		USB Standard Configuration Descriptor 2	
0x80	bLength	Length of configuration descriptor in bytes.	0x09
0x81	bDescriptorType	Descriptor type.	0x02
0x82	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27
0x83	bTotalLength (MSB)		0x00
0x84	bNumInterfaces	Number of interfaces supported. The ISD-300A1 only supports one interface.	0x01
0x85	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. This value must be set to 0x02	0x02
0x86	Configuration	Index to the configuration string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x00
0x87	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On-board default 7 Reserved. '1' 6 Self-powered. '1' 5 Remote wake-up. '0' 4-0 Reserved, set to 0. '0'	0xC0
0x88	bMaxPower	Maximum power consumption for this configuration. Units used are mA*2 (i.e. 0x31 98 mA, 0xF9 498 mA).	0x0x31

Address	Field Name	Description	Example SROM Data
		USB Other Speed Configuration Descriptor 2	
0x39	bLength	Length of configuration descriptor in bytes.	0x09
0x3A	bDescriptorType	Descriptor type.	0x07
0x3B	bTotalLength (LSB)	Number of bytes returned in this configuration. This includes the configuration descriptor plus all the interface and endpoint descriptors.	0x27
0x3C	bTotalLength (MSB)		0x00
0x3D	bNumInterfaces	Number of interfaces supported. The ISD-300A1 only supports one interface.	0x01
0x3E	bConfiguration Value	The value to use as an argument to Set Configuration to select the configuration. This value must be set to 0x02	0x02
0x3F	Configuration	Index to configuration string. This entry must equal half of the address value where the string starts or 0 if the string does not exist.	0x00
0x40	bmAttributes	Device attributes for this configuration. Configuration characteristics: Bit Description On-board default 7 Reserved. '1' 6 Self-powered. '0' 5 Remote wake-up. '0' 4-0 Reserved, set to 0. '0'	0x00
0x41	bMaxPower	Maximum power consumption for the second configuration. Units used are mA*2 (i.e. 0x31 = 98 mA, 0xF9 = 498 mA).	0x31
		USB String Descriptor (Manufacturer)	
0x42	bLength	Descriptor length	0x22
0x43	bDescriptorType	Descriptor type	0x03
0x44	bString	("P")	0x49
0x45	bString	("NULL")	0x00
0x46	bString	("r")	0x6E
0x47	bString	("NULL")	0x00
0x48	bString	("o")	0x2D
0x49	bString	("NULL")	0x00
0x4A	bString	("S")	0x53
0x4B	bString	("NULL")	0x00
0x4C	bString	("y")	0x79
0x4D	bString	("NULL")	0x00
0x4E	bString	("s")	0x73
0x4F	bString	("NULL")	0x00
0x50	bString	("t")	0x74
0x51	bString	("NULL")	0x00
0x52	bString	("e")	0x65
0x53	bString	("NULL")	0x00
0x54	bString	("m")	0x6D
0x55	bString	("NULL")	0x00
0x56	bString	(" ")	0x20
0x57	bString	("NULL")	0x00
0x58	bString	("D")	0x44
0x59	bString	("NULL")	0x00
0x5A	bString	("e")	0x65
0x5B	bString	("NULL")	0x00
0x5C	bString	("v")	0x76
0x5D	bString	("NULL")	0x00
0x5E	bString	("i")	0x69
0x5F	bString	("NULL")	0x00
0x60	bString	("c")	0x63

Address	Field Name	Description	Example SROM Data
0xB1	bString	("NULL")	0x00
0xB2	bString	("V")	0x56
0xB3	bString	("NULL")	0x00
USB String Descriptor (Product)			
0xB4	bLength	Descriptor length	0x28
0xB5	bDescriptorType	Descriptor type	0x03
0xB6	bString	("U")	0x55
0xB7	bString	("NULL")	0x00
0xB8	bString	("S")	0x53
0xB9	bString	("NULL")	0x00
0xBA	bString	("B")	0x42
0xBB	bString	("NULL")	0x00
0xBC	bString	(" ")	0x20
0xBD	bString	("NULL")	0x00
0xBE	bString	("S")	0x53
0xBF	bString	("NULL")	0x00
0xC0	bString	("t")	0x74
0xC1	bString	("NULL")	0x00
0xC2	bString	("o")	0x6F
0xC3	bString	("NULL")	0x00
0xC4	bString	("r")	0x72
0xC5	bString	("NULL")	0x00
0xC6	bString	("a")	0x61
0xC7	bString	("NULL")	0x00
0xC8	bString	("g")	0x67
0xC9	bString	("NULL")	0x00
0xCA	bString	("e")	0x65
0xCB	bString	("NULL")	0x00
0xCC	bString	(" ")	0x20
0xCD	bString	("NULL")	0x00
0xCE	bString	("A")	0x41
0xCF	bString	("NUL")	0x00
0xD0	bString	("d")	0x64
0xD1	bString	("NUL")	0x00
0xD2	bString	("a")	0x61
0xD3	bString	("NULL")	0x00
0xD4	bString	("p")	0x70
0xD5	bString	("NULL")	0x00
0xD6	bString	("t")	0x74
0xD7	bString	("NULL")	0x00
0xD8	bString	("e")	0x65
0xD9	bString	("NUL")	0x00
0xDA	bString	("r")	0x72
0xDB	bString	("NUL")	0x00
USB String Descriptor (Serial Number)			
0xDC	bLength	Descriptor length	0x24
0xDD	bDescriptorType	Descriptor Type	0x03

Address	Field Name	Description	Example SROM Data
0xEE	bString	("0")	0x30
0xEF	bString	("NUL")	0x00
0xF0	bString	("1")	0x31
0xF1	bString	("NUL")	0x00
0xF2	bString	("2")	0x32
0xF3	bString	("NUL")	0x00
0xF4	bString	("3")	0x33
0xF5	bString	("NUL")	0x00
0xF6	bString	("4")	0x34
0xF7	bString	("NUL")	0x00
0xF8	bString	("5")	0x35
0xF9	bString	("NUL")	0x00
0xFA	bString	("6")	0x36
0xFB	bString	("NUL")	0x00
0xFC	bString	("7")	0x37
0xFD	bString	("NUL")	0x00
0xFE	bString	("8")	0x38
0xFF	bString	("NUL")	0x00
0x100	bString	("9")	0x39
0x101	bString	("NUL")	0x00
0x102	bString	("0")	0x30
0x103	bString	("NUL")	0x00
0x104	bString	("1")	0x31
0x105	bString	("NUL")	0x00
0x106	bString	("2")	0x32
0x107	bString	("NUL")	0x00
0x108	bString	("3")	0x33
0x109	bString	("NUL")	0x00
0x10A	bString	("4")	0x34
0x10B	bString	("NUL")	0x00
0x10C	bString	("5")	0x35
0x10D	bString	("NUL")	0x00
0x10E	bString	("6")	0x36
0x10F	bString	("NUL")	0x00
0x110 –		Unused I²C memory device space	0xXX

Table 30 – Example I²C memory device / VBh Identify Data