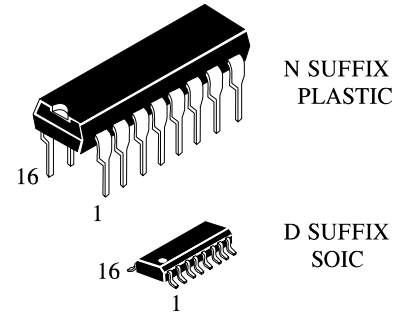


QUAD CLOCKED «D» LATCH
High-Voltage Silicon-Gate CMOS

CD4042B types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical. Information present at the data input is transferred to outputs Q and Q during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

The CD4042B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes); 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 1.0 V min @ 5.0 V supply
 2.0 V min @ 10.0 V supply
 2.5 V min @ 15.0 V supply

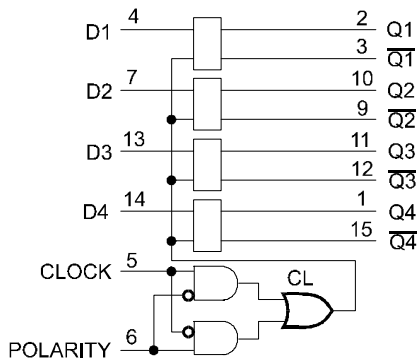


ORDERING INFORMATION

IW4042BN Plastic
 IW4042BD SOIC

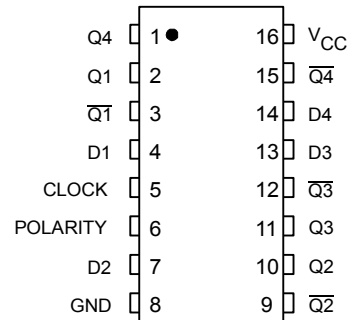
T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN 16 = V_{CC}
 PIN 8 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
Clock	Polarity	Q
0	0	D
1	0	Latch
1	1	D
0	1	Latch

IW4042B

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_I	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_I	DC Input Current, per Pin	± 10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_{tot}	Dissipation per Output Transistor	100	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_I, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.5 V or V _{CC} - 0.5 V V _{OUT} =1.0 V or V _{CC} - 1.0 V V _{OUT} =1.5 V or V _{CC} - 1.5 V	5.0	3.5	3.5	3.5	V
			10	7	7	7	
			15	11	11	11	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.5 V or V _{CC} - 0.5 V V _{OUT} =1.0 V or V _{CC} - 1.0 V V _{OUT} =1.5 V or V _{CC} - 1.5 V	5.0	1.5	1.5	1.5	V
			10	3	3	3	
			15	4	4	4	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =GND or V _{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
I _{IN}	Maximum Input Leakage Current	V _{IN} = GND or V _{CC}	18	±0.1	±0.1	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = GND or V _{CC}	5.0	1	1	30	μA
			10	2	2	60	
			15	4	4	120	
			20	20	20	600	
I _{OL}	Minimum Output Low (Sink) Current	V _{IN} = GND or V _{CC} V _{OL} =0.4 V V _{OL} =0.5 V V _{OL} =1.5 V	5.0	0.64	0.51	0.36	mA
			10	1.6	1.3	0.9	
			15	4.2	3.4	2.4	
I _{OH}	Minimum Output High (Source) Current	V _{IN} = GND or V _{CC} V _{OH} =2.5 V V _{OH} =4.6 V V _{OH} =9.5 V V _{OH} =13.5 V	5.0	-2.0	-1.6	-1.15	mA
			5.0	-0.64	-0.51	-0.36	
			10	-1.6	-1.3	-0.9	
			15	-4.2	-3.4	-2.4	

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AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, $R_L=200\text{ k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			≥ -55 $^{\circ}\text{C}$	25°C	≤ 125 $^{\circ}\text{C}$	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Clock to Q (Figure 1)	5.0	450	450	900	ns
		10	200	200	400	
		15	160	160	320	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Cl \bar{o} ck to Q (Figure 1)	5.0	500	500	1000	ns
		10	230	230	460	
		15	180	180	360	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Data to Q (Figure 2)	5.0	220	220	440	ns
		10	110	110	220	
		15	80	80	160	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Da \bar{t} a to Q (Figure 2)	5.0	300	300	600	ns
		10	150	150	300	
		15	100	100	200	
t_{TLH} , t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	80	80	160	
C_{IN}	Maximum Input Capacitance	-		7.5		pF

TIMING REQUIREMENTS ($C_L=50\text{pF}$, $R_L=200\text{ k}\Omega$, Input $t_r=t_f=20\text{ ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			≥ -55 $^{\circ}\text{C}$	25°C	$\leq 125^{\circ}$ $^{\circ}\text{C}$	
t_w	Minimum Pulse Width, Clock (Figure 1)	5.0	200	200	400	ns
		10	100	100	200	
		15	60	60	120	
t_{su}	Minimum Setup Time, Data to Clock (Figure 1)	5.0	50	50	100	ns
		10	30	30	60	
		15	25	25	50	
t_h	Minimum Hold Time, Clock to Data (Figure 1)	5.0	120	120	240	ns
		10	60	60	120	
		15	50	50	100	
t_r , t_f	Maximum Input Rise or Fall Time, Clock (Figure 1)	5.0 10 15	Not rise or fall time sensitive			μs

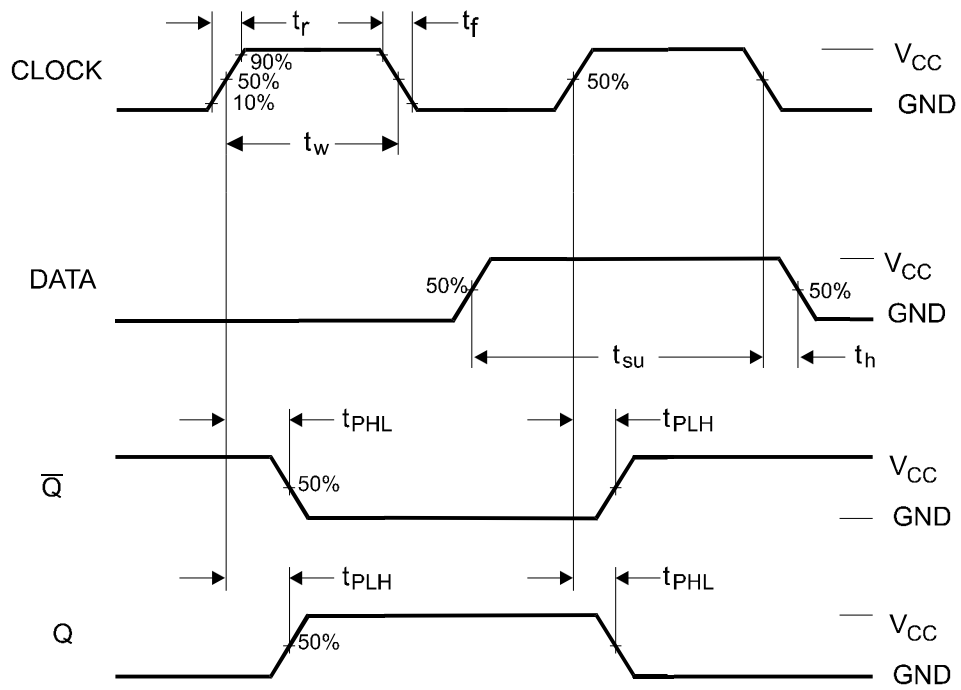


Figure 1. Switching Waveforms

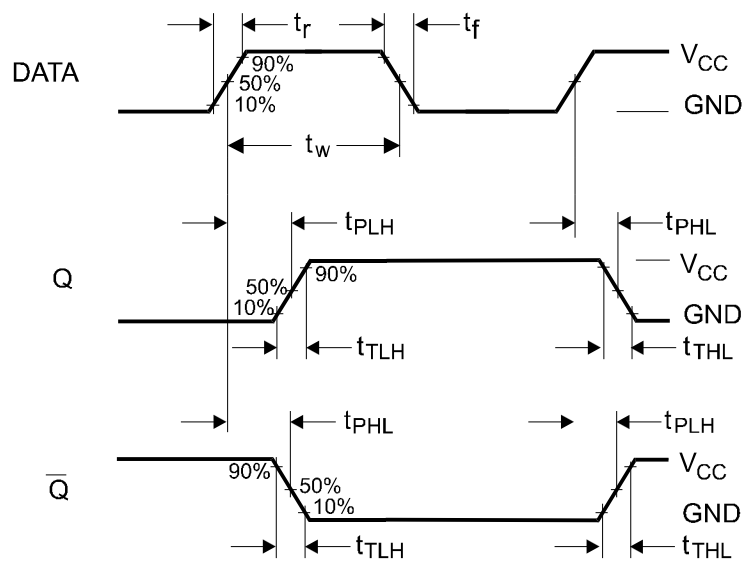


Figure 2. Switching Waveforms