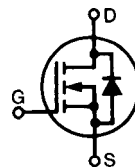


MegaMOS™FET

IXTH 14N80

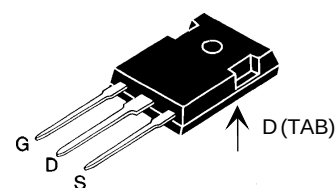
$V_{DSS} = 800\text{ V}$
 $I_{D25} = 14\text{ A}$
 $R_{DS(on)} = 0.70\ \Omega$

N-Channel Enhancement Mode



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}$	800	V
V_{DGR}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}; R_{GS} = 1\text{ M}\Omega$	800	V
V_{GS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	14	A
I_{DM}	$T_C = 25^\circ\text{C}$, pulse width limited by T_{JM}	56	A
P_D	$T_C = 25^\circ\text{C}$	300	W
T_J		$-55 \dots +150$	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		$-55 \dots +150$	$^\circ\text{C}$
Max. lead temperature for soldering 300		$^\circ\text{C}$	
1.6 mm (0.063 in) from case for 10 s			
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		6	g

TO-247 AD



G = Gate,
S = Source,
D = Drain,
TAB = Drain

Features

- International standard package
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Low package inductance ($< 5\text{ nH}$)
 - easy to drive and to protect
- Fast switching times

Applications

- Switch-mode and resonant-mode power supplies
- Motor control
- Uninterruptible Power Supplies (UPS)
- DC choppers

Advantages

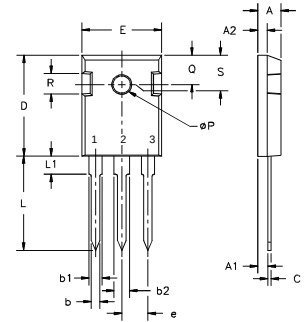
- Easy to mount with 1 screw (isolated mounting screw hole)
- Space savings
- High power density

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0\text{ V}, I_D = 3\text{ mA}$	800		V
$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2		4.5 V
I_{GSS}	$V_{GS} = \pm 20\text{ V}_{DC}, V_{DS} = 0$			$\pm 100\text{ nA}$
I_{DSS}	$V_{DS} = 0.8 \cdot V_{DSS}$ $V_{GS} = 0\text{ V}$ $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$			250 μA 1 mA
$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 0.5 I_{D25}$ Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$			0.7 Ω

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
g_{fs}	$V_{DS} = 10\text{ V}$; $I_D = 0.5 \cdot I_{D25}$, pulse test	8	14	S
C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$		4500	pF
C_{oss}			310	pF
C_{rss}			65	pF
$t_{d(on)}$	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 I_{D25}$ $R_G = 2\ \Omega$, (External)		20	50 ns
t_r			33	50 ns
$t_{d(off)}$			63	100 ns
t_f			32	50 ns
$Q_{g(on)}$	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 I_{D25}$		145	170 nC
Q_{gs}			30	45 nC
Q_{gd}			55	80 nC
R_{thJC}			0.42	K/W
R_{thCK}				K/W

Source-Drain Diode		Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
Symbol	Test Conditions	min.	typ.	max.
I_S	$V_{GS} = 0\text{ V}$			14 A
I_{SM}	Repetitive; pulse width limited by T_{JM}			56 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{ V}$, Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$			1.5 V
t_{rr}	$I_F = I_S$, $-di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 100\text{ V}$		800	ns

TO-247 AD Outline



Terminals: 1 - Gate 2 - Drain
3 - Source Tab - Drain

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.7	5.3	.185	.209
A ₁	2.2	2.54	.087	.102
A ₂	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b ₁	1.65	2.13	.065	.084
b ₂	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
ØP	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15	BSC	.242	BSC

Figure 1. Output Characteristics at 25°C

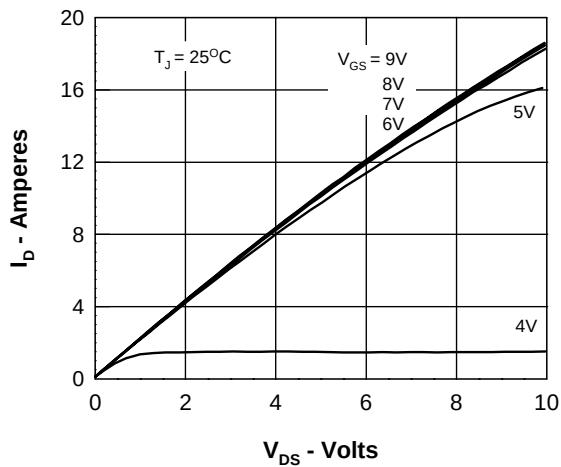


Figure 2. Output Characteristics at 125°C

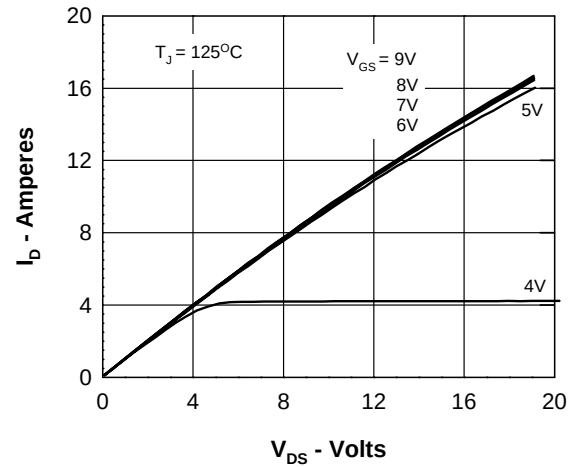
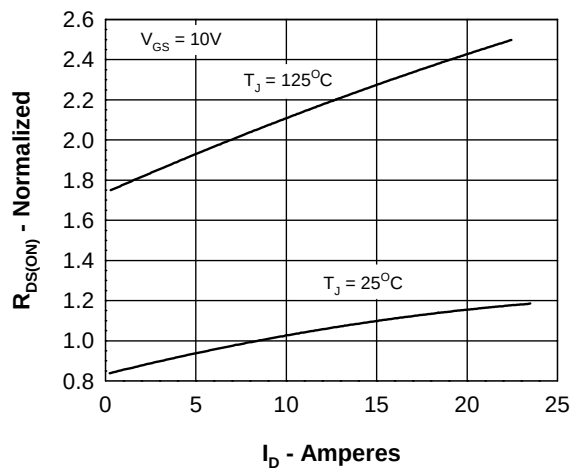
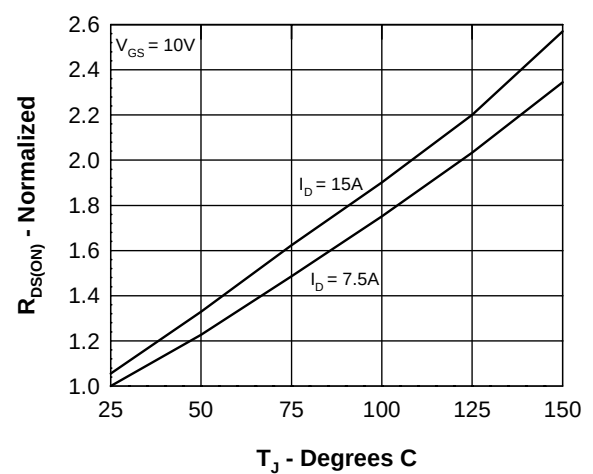

Figure 3. $R_{DS(on)}$ normalized to 0.5 I_{D25} value vs. I_D

Figure 4. $R_{DS(on)}$ normalized to 0.5 I_{D25} value vs. T_J


Figure 5. Drain Current vs. Case Temperature

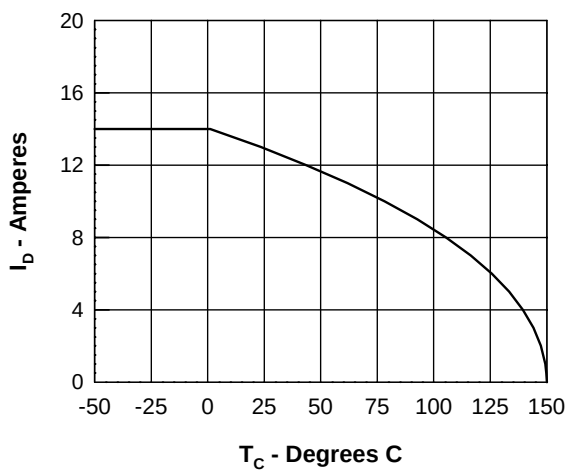


Figure 6. Admittance Curves

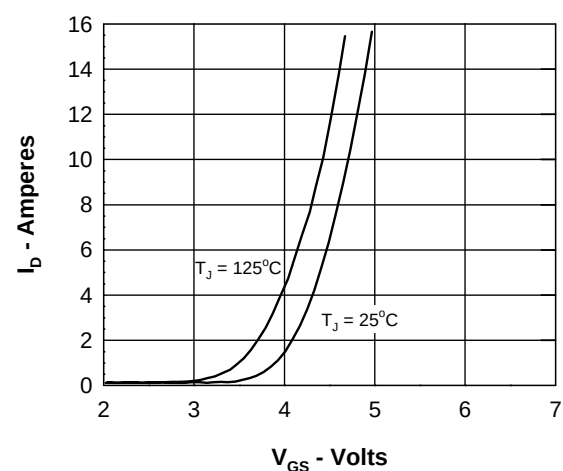


Figure 7. Gate Charge

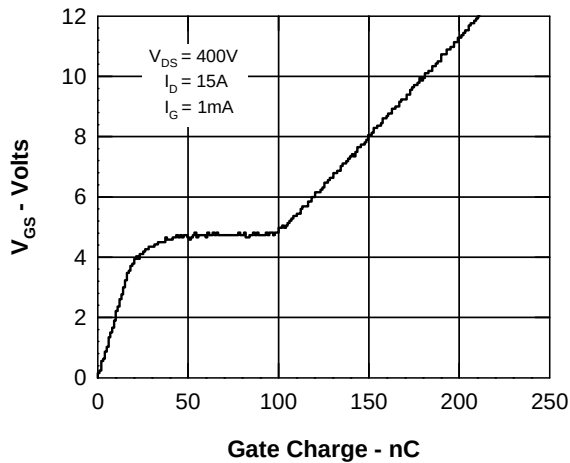


Figure 8. Capacitance Curves

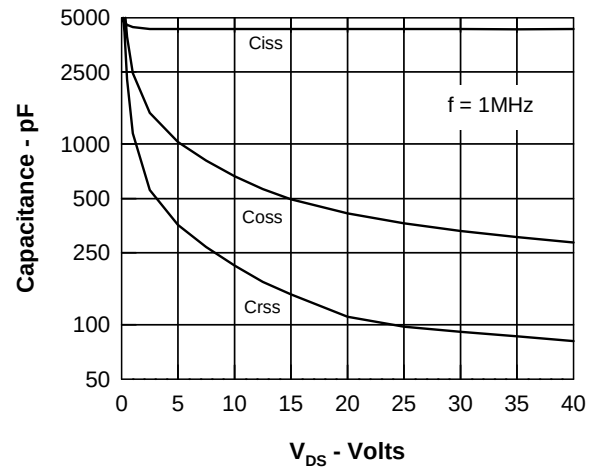


Figure 9. Source Current vs. Source to Drain Voltage

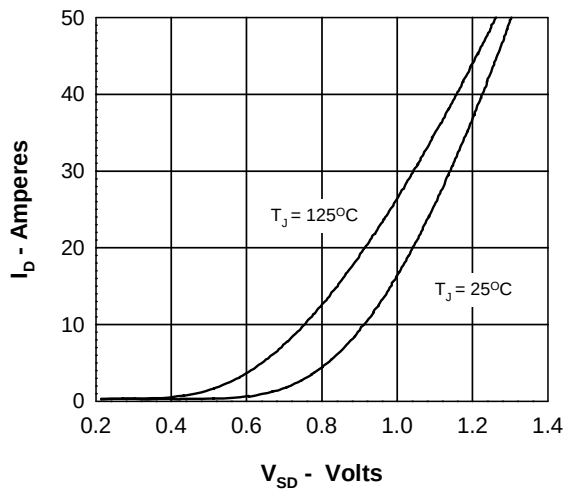


Figure 10. Forward Bias Safe Operating Area

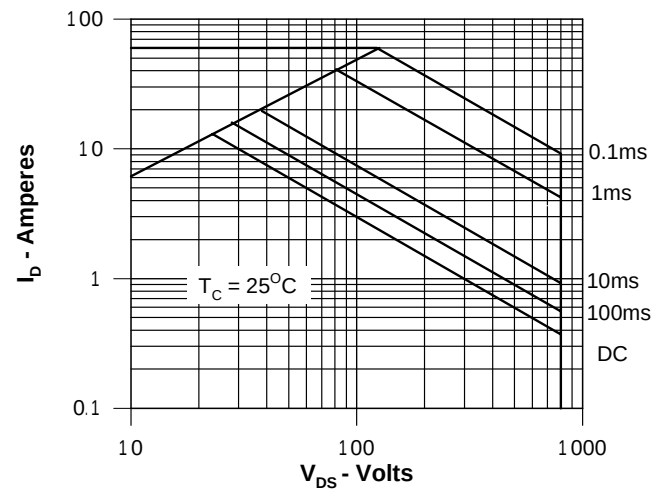


Figure 11. Transient Thermal Resistance

