M37409M2-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37409M2-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 52-pin shrink plastic molded DIP (flat package type also available). This single-chip microcomputer is useful for the communication application used as a slave-microcomputer.
In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.
The differences between the M37409M2-XXXSP and the M37409M2-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

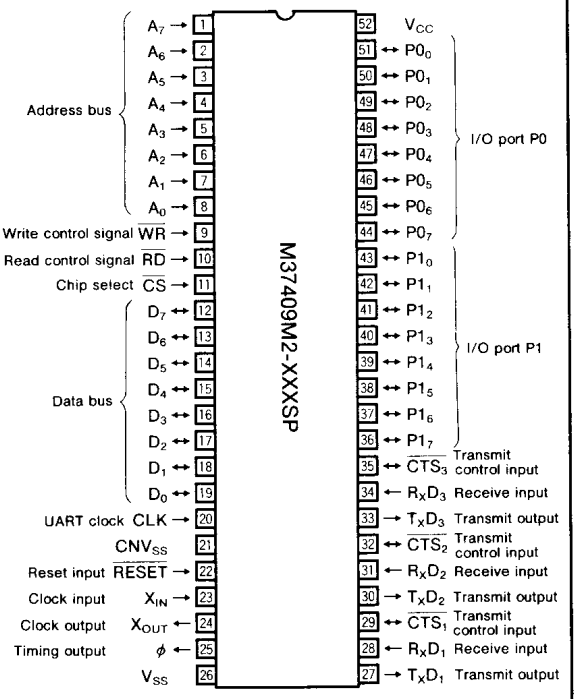
FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 4096 bytes
  RAM ..... 128 bytes
- Instruction execution time
  ... 0.8μs (minimum instructions at 10MHz frequency)
- Single power supply f(X_{IN})=10MHz ..... 5V±10%
- Power dissipation
  normal operation mode (at 10MHz frequency) .. 50mW
- Subroutine nesting ..... 64 levels (Max.)
- Interrupt ..... 10 types
- 8-bit timer 1
- UART (Full-duplex) ..... 3 channels
- Dual-port RAM ..... 192 bytes
- Communication registers
  Access flag ..... 192 bits
  Collision detect register ..... 8-bit×1
  IPC* semaphore register ..... 7-bit×1
  IPC mode register ..... 8-bit×4
  IPC error register ..... 8-bit×4
- Programmable I/O ports
  (Ports P0, P1, $\overline{CTS_1}$~$\overline{CTS_3}$) 19
- Bus interface
  Address bus 8
  Data bus 8
  Control signal ($\overline{WR}$, $\overline{RD}$, $\overline{CS}$) 3

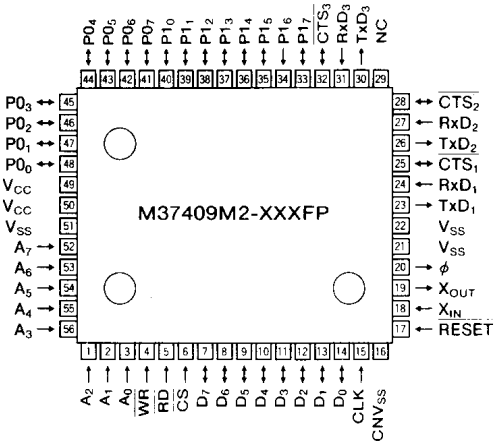
APPLICATION

Office automation equipment

PIN CONFIGURATION (TOP VIEW)



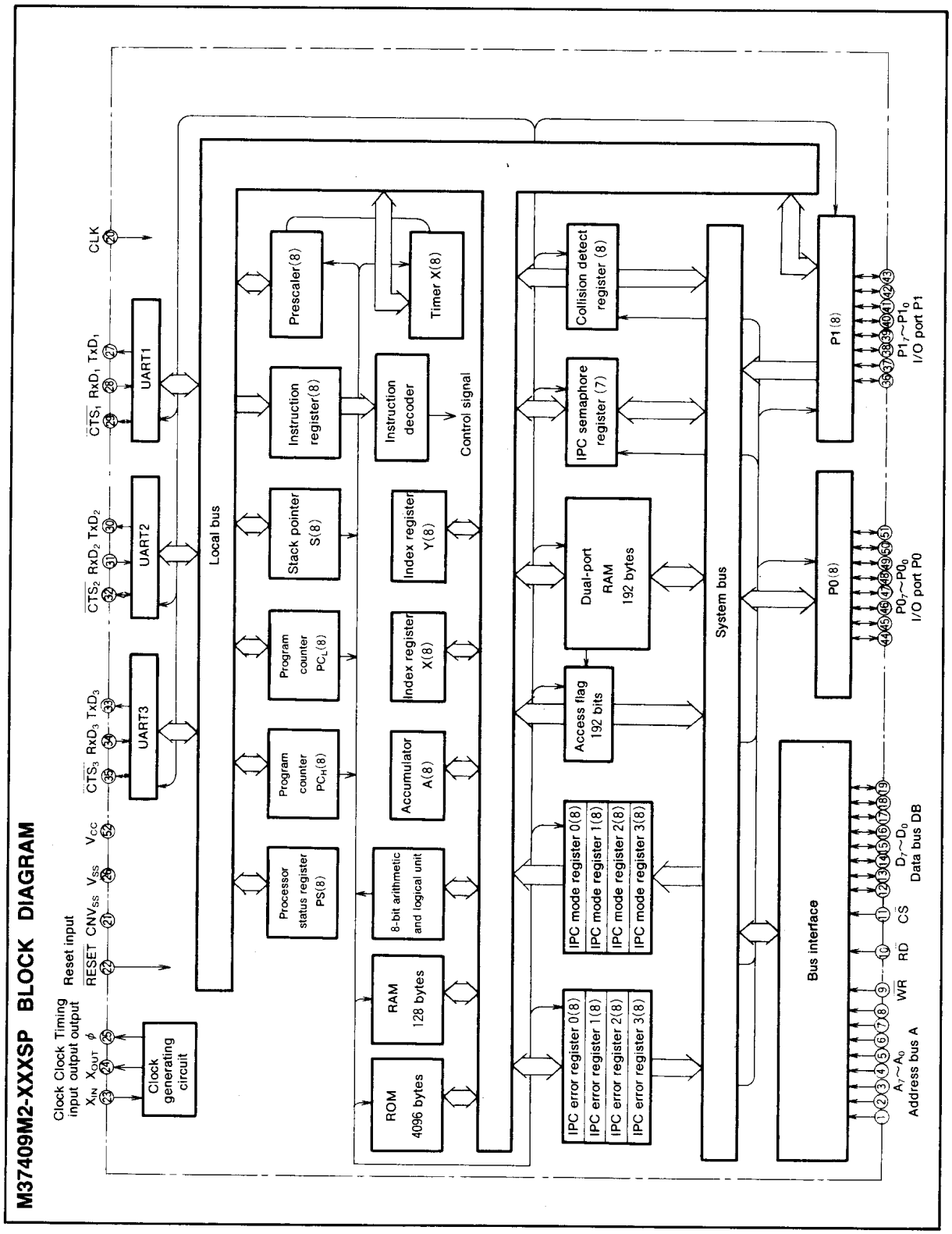
Outline 52P4B



Outline 56P6N

NC : No connection

*IPC···Intelligent Protcol Controller



MITSUBISHI ELECTRIC

FUNCTIONS OF M37409M2-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			0.8μs (minimum instructions, at 10MHz frequency)
Clock frequency			10MHz
Memory size	ROM		4096 bytes
	RAM		128 bytes
Input/Output ports	$P0_0$~$P0_7$	I/O	8-bit×1 (System bus I/O)
	$P1_0$~$P1_7$	I/O	8-bit×1 (Local bus I/O, System bus input)
	$\overline{CTS_1}$~$\overline{CTS_3}$	I/O	1-bit×3 (Common with UART transmit control input)
Bus interface	A_0~A_7	Input	8-bit×1
	D_0~D_7	I/O	8-bit×1
	$\overline{RD}$, $\overline{WR}$, $\overline{CS}$	Input	1-bit×3
UART			3 (with programmable baud rate generator)
Timer			8-bit×1 (with 8-bit prescaler)
Interrupt			System bus (IPCM0) interrupt 1, UART interrupt 6, Timer interrupt 1, Collision interrupt 1
Dual-port RAM			192 bytes
Communication registers	Access flag		192 bits
	Collision detect register		8-bit×1
	IPC semaphore register		7-bit×1
	IPC mode register		8-bit×4
	IPC error register		8-bit×4
Subroutine nesting			64 levels (max.)
Clock generating circuit			Built-in (externally connected ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	at operation		50mW
	at wait mode		5mW
	at stop mode	T_a=25℃	0.05mW
		T_a=70℃	0.5mW
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package	M37409M2-XXXSP		52-pin shrink plastic molded DIP
	M37409M2-XXXFP		56-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output. This port is connected to the system bus only, and can not be accessed from the local bus. At reset this port becomes input mode. The output structure is CMOS output.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. This port is connected to the local bus and can be used as only input port from the system bus. The output structure is CMOS output.
T_XD_1 ~T_XD_3	UART transfer output	Output	These are UART transfer data output pins.
R_XD_1 ~R_XD_3	UART receive input	Input	These are UART receive data input pins.
$\overline{CTS_1}$ ~$\overline{CTS_3}$	UART transfer control input	I/O	These are UART transfer control signal input pins and can be used as I/O port which have basically same function as port P1.
CLK	UART clock input	Input	This port is an external clock input pin for baud rate.
A_0~A_7	Address input	Input	This port is input for system address.
D_0~D_7	Data input/output	I/O	This port is input or output the system data.
$\overline{CS}$	Chip select	Input	System data can be read or written by inputting "L" to this port.
$\overline{RD}$	Read control input	Input	Memory or register data specified by A_0~A_7 is read from D_0~D_7 by inputting "L" to this port.
$\overline{WR}$	Write control input	Input	Data input from D_0~D_7 is written to memory or register specified by A_0~A_7 by inputting "L" to this port.

BASIC FUNCTION BLOCKS

MEMORY

M37409M2-XXXSP has two buses; the local bus connected to the CPU of its own, and the system bus connected to the CPU of the external master computer. There are two corresponding address area. Figure 1 shows the memory map of the local bus and the system bus, respectively.

The local bus has thirteen address buses and eight data buses. The address area, which is 8192 bytes, is addresses from 0000_{16} to $1FFF_{16}$.

For this local bus area, addresses 1000_{16} to $1FFF_{16}$ are assigned to the built-in ROM area which consists of 4096 bytes.

Addresses $1F00_{16}$ to $1FFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $1FEC_{16}$ to $1FFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, dual port RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $007F_{16}$ are assigned to the built-in RAM and consist of 128 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

The system bus has eight address buses and eight data buses. The address area, which is 256 bytes, is addresses from 00_{16} to FF_{16}.

The dual port RAM, access flag, port, IPC mode / IPC error register etc., are assigned to this area.

The internal memories and registers are connected to one or both of these buses. Therefore, it is necessary, in writing programs, to know the operation of each functional block as well as to which bus the memories and registers are connected at what addresses.

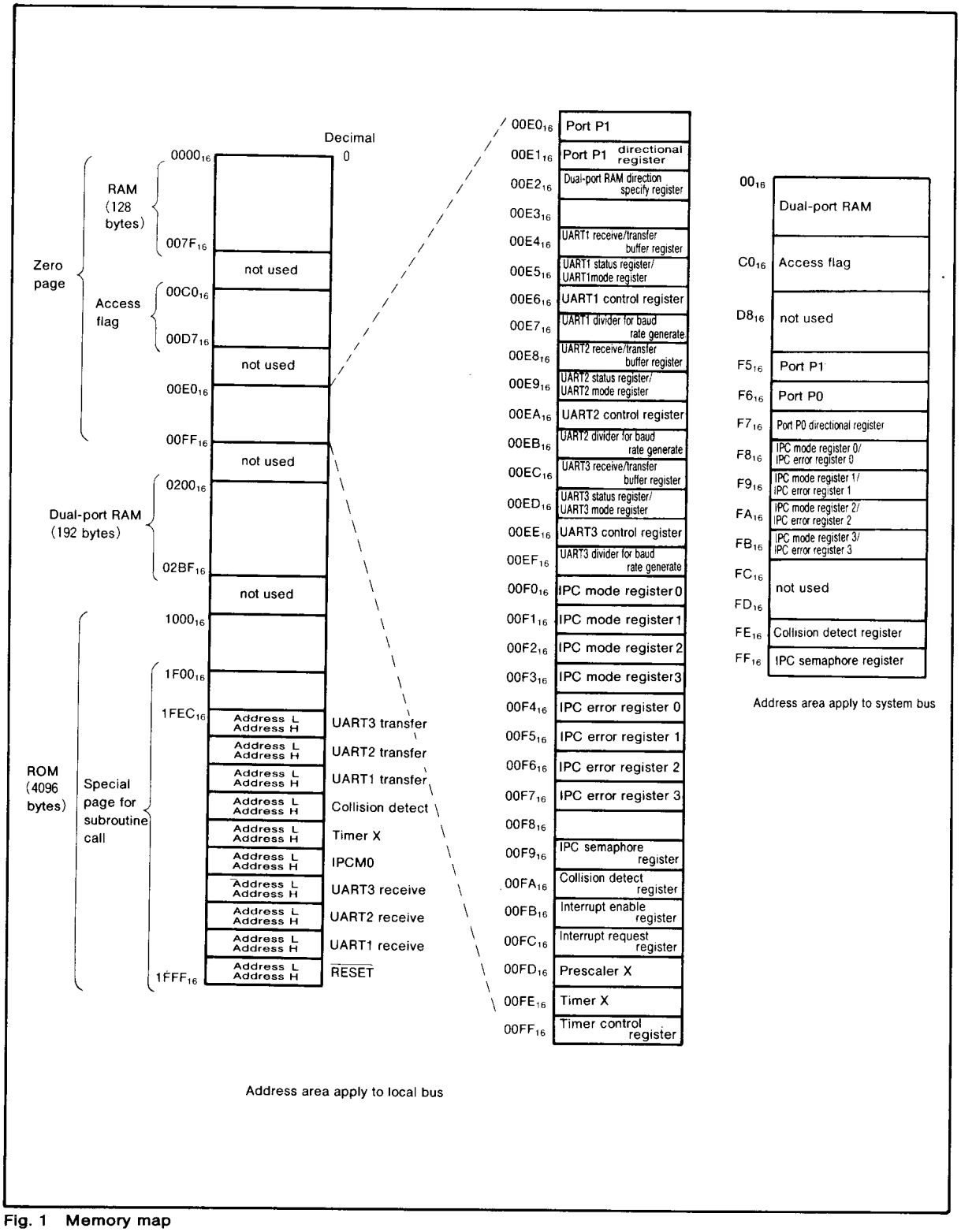


Fig. 1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.

In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.

In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

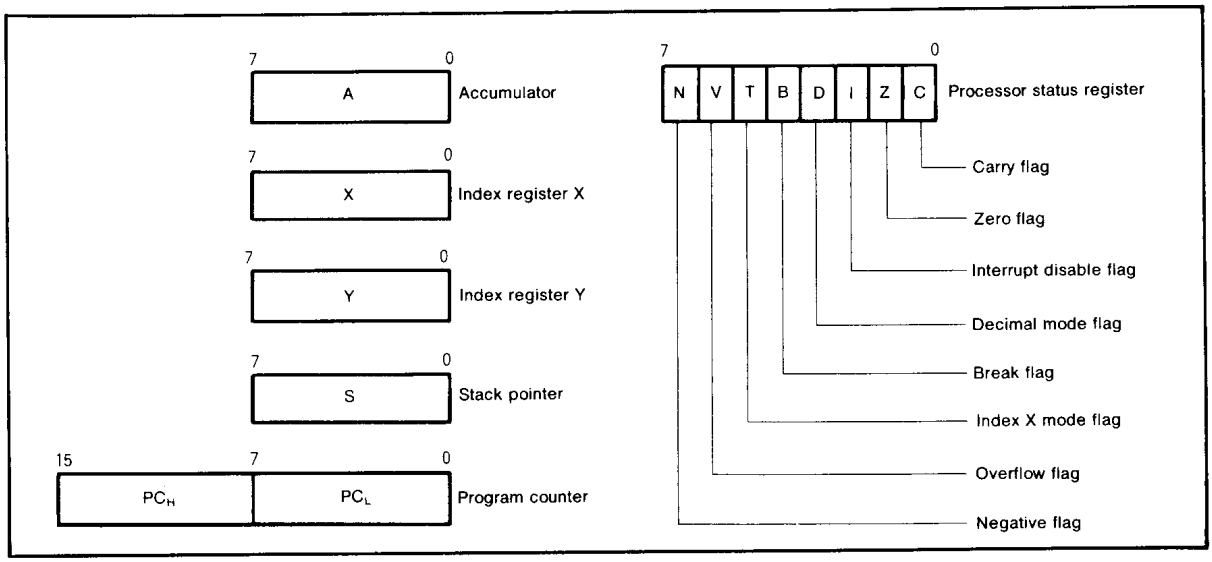


Fig. 2 Register structure

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Bus Interface

M37409M2-XXXSP has the bus interface to operate itself by the control signal sent from the master CPU. The master CPU can access the memories and registers located in the system address area described below via this bus interface. The bus interface has address pins A_0 to A_7, data pins D_0 to D_7, and three controls signals $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ which can be directly connected to TTL.

Driving the $\overline{CS}$ pin to "L" put this microcomputer in the read/write enabled state. When writing data from the master CPU, specify the address by $A_0 \sim A_7$ and set $\overline{WR}$ to "L", and the data at $D_0 \sim D_7$ is written to the specified address. When reading data, specify the address by $A_0 \sim A_7$ and set $\overline{RD}$ to "L", and the contents of the specified address are output to $D_0 \sim D_7$.

Driving the $\overline{CS}$ pin to "H" puts the M37409M2-XXXSP in the state which does not allow the read and write operations from the master CPU. At this time, the outputs of D_0 to D_7 are in the floating state.

Figure 3 shows the block diagram of the bus interface.

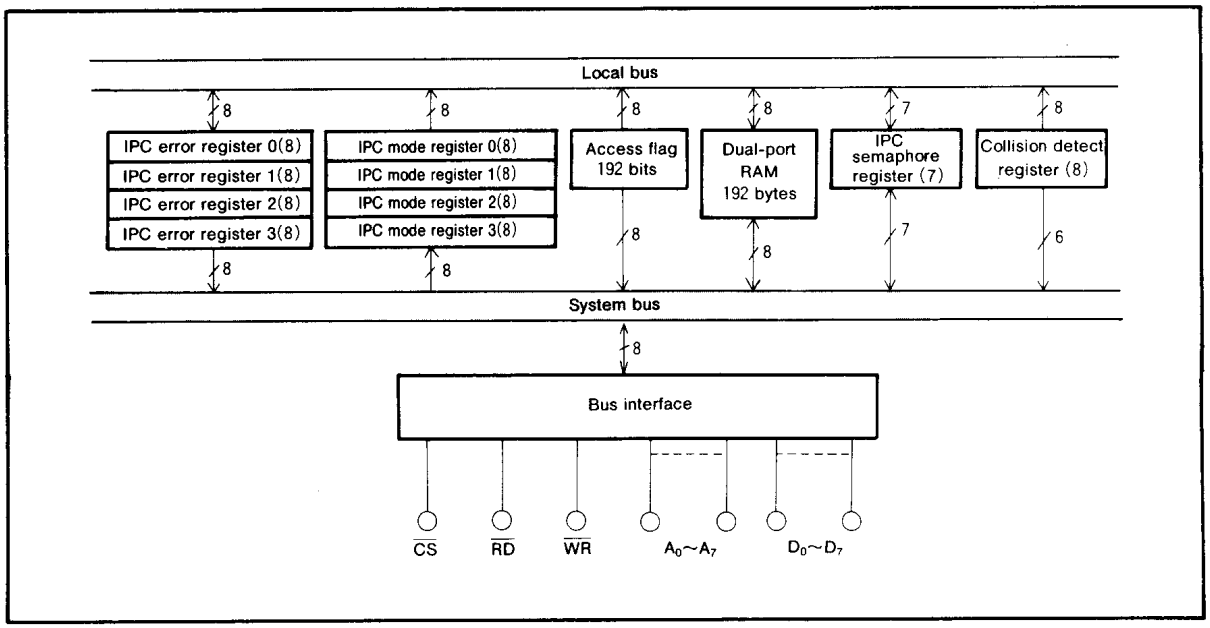


Fig. 3 Block diagram of bus interface

Dual-port RAM

The dual-port RAM, which is 192 bytes, is the memory which allows the read/write operation from both the local and system buses independently. From the local bus, it is allocated at addresses 0200_{16} to $02BF_{16}$; from the system bus, addresses 00_{16} to BF_{16}. Table 1 shows the result when the write and read operations from both buses compete at the same address.

Table 1. Result obtained by simultaneously accessing the same address from the system and local buses

	Write	Read
Simultaneous read from both buses	—	Correct data
Simultaneous write from both buses	Unpredictable	—
Read from one bus, write from the other	Correct data	Uncertain

[Access flag]

Local bus : address $00C0_{16}$~$00D7_{16}$
System bus : address $C0_{16}$~$D7_{16}$

The access flag arbitrates the access to the dual-port RAM. One bit of access flag is allocated to one byte of dual port RAM, amounting 192 bits (24 bytes) in total. The access flag can be read from both the system and local buses. Figure 4 shows the relationship between each byte of the dual port RAM and each bit of the access flag. Each bit is cleared to "0" when an access to read is made to the dual port RAM from either bus; it is set to "1" when an access to write is made. If an access to read from one bus and an access to write from the other compete at the same address of the dual port RAM, the values of the corresponding access flags are uncertain. At reset, all access flags are cleared to "0".

[Dual-port RAM direction specify register]

Local bus : address $00E2_{16}$

This register specifies that the read operation of which bus clears each bit of the access flag. One bit of this register corresponds to 32 bytes of the dual-port RAM (32 bits of the access flag). This register consists of six bits. Each access flag is cleared by the read operation from the system bus when the corresponding dual-port RAM direction specify register is "0"; when it is "1", each access flag is cleared by the read operation from the local bus. As for a write operation, the access flag is set regardless of which bus has made it. Table 2 shows the relationship between each bit of the dual-port RAM direction specify register and the dual-port RAM and the access flag. At reset, all bits are cleared to "0".

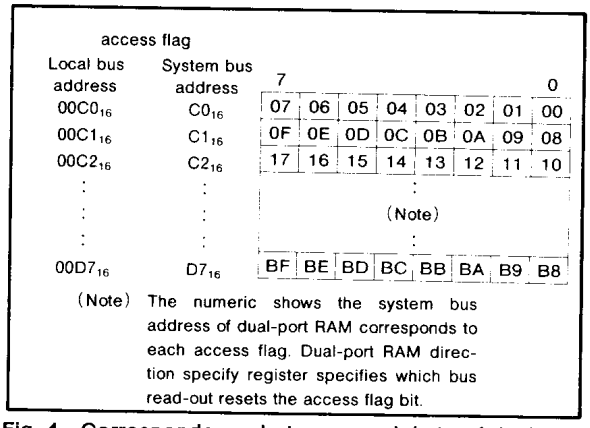


Fig. 4 Correspondence between each byte of dual-port RAM and each bit of access flag

Table 2. Correspondence among each bit of dual-port RAM direction specify register, dual-port RAM and access flag

Dual-port RAM direction specify register	Dual-port RAM		Access flag	
	Local bus address	System bus address	Local bus address	System bus address
bit 0	0200_{16}~$021F_{16}$	00_{16}~$1F_{16}$	$00C0_{16}$~$00C3_{16}$	$C0_{16}$~$C3_{16}$
bit 1	0220_{16}~$023F_{16}$	20_{16}~$3F_{16}$	$00C4_{16}$~$00C7_{16}$	$C4_{16}$~$C7_{16}$
bit 2	0240_{16}~$025F_{16}$	40_{16}~$5F_{16}$	$00C8_{16}$~$00CB_{16}$	$C8_{16}$~CB_{16}
bit 3	0260_{16}~$027F_{16}$	60_{16}~$7F_{16}$	$00CC_{16}$~$00CF_{16}$	CC_{16}~CF_{16}
bit 4	0280_{16}~$029F_{16}$	80_{16}~$9F_{16}$	$00D0_{16}$~$00D3_{16}$	$D0_{16}$~$D3_{16}$
bit 5	$02A0_{16}$~$02BF_{16}$	$A0_{16}$~BF_{16}	$00D4_{16}$~$00D7_{16}$	$D4_{16}$~$D7_{16}$

[IPC mode register, IPC error register]

Local bus : address $00F0_{16}$~$00F7_{16}$
System bus : address $F8_{16}$~FB_{16}

IPC mode registers 0~3 (IPCM0~IPCM3) and IPC error registers 0~3 (ERR0~ERR3) are the 8-bit registers which can be set by the user without restriction. IPC mode registers 0~3 are used to specify the mode setting such as UART from the external master CPU via the system bus. IPC error registers 0~3 are used to indicate the error found on the local CPU to the outside via the system bus. On the system bus, IPC mode registers 0~3 and IPC error registers 0~3 share four bytes of the same address, with the former being for write only and the latter for read only. On the local bus, the former is for read only and the latter is for both read and write.

The data written from the system bus to IPC mode registers 0~3 can be read from the local bus only. If an access to read or write is performed from the system bus on IPC mode register 0/IPC error register 0, an interrupt request (IPCM0) is caused.

When IPC error registers 0~3 are accessed for read from the system bus, only the bits which are found "1" are reset by hardware. When these registers are read from the local bus, their values remain unchanged. If an access to read is performed by the system bus between the read cycle and write cycle of the local bus when IPC error registers 0~3 are accessed from the local bus by a read-modify-write instruction, the hardware reset signal for the bit which is found "1" by the system bus continues until the local CPU fetches a next instruction.

[IPC semaphore register]

Local bus : address $00F9_{16}$
System bus : address FF_{16}

This register is for handshaking with the master CPU and consists of block semaphore flags (BS0~BS5) and the ready flag (RDY). BS0~BS5 can be read/written from both the local and system buses. RDY can be read/written from the local bus and read only from the system bus. With this register, all bits can be read at a time but, in a write operation, only one bit can be written at a time. The low-order three bits of the data to be written are used to specify to which register bit the data is to be written. Bit 7 is used to specify whether to write "1" or "0". At reset, all bits are cleared to "0".

RDY is cleared to "0" also when an access to write is performed by the system bus on IPC mode register 0.

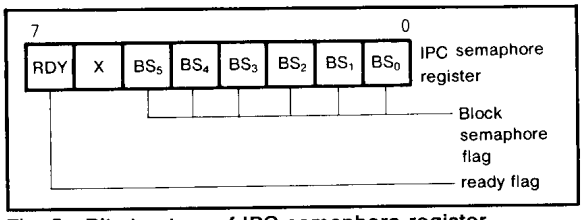


Fig. 5 Bit structure of IPC semaphore register

[Collision detect register]

Local bus : address $00FA_{16}$
System bus : address FE_{16}

This register consists of six bits of collision detect flags (CD_0~CD_5), the collision interrupt enable bit, and collision interrupt request bit. The collision detect flags are set when an access to read is performed by the system bus on the same address on the dual port RAM to which the local bus is writing data. These flags indicate that the data read by the master CPU may be incorrect. When these flags are set, a collision detect interrupt request occurs.

Each collision flag corresponds to each 32 bits of the dual port RAM. The flag bit corresponding to the address at which access competition occurred is set. The relationship between the flag bits and the dual port RAM is shown in Table 3. These flags can be read from both buses. All bits are cleared when read from the system bus or at reset.

The collision interrupt enable bit can be read/written from the local bus. When it is read from the system bus, "0" is always output. The collision interrupt request bit can be read only from the local bus. Only "0" can be written.

Table 3. Correspondence between collision detect flag and dual-port RAM

Collision detect flag	Dual-port RAM	
	Local bus address	System bus address
CD_0	0200_{16}~$021F_{16}$	00_{16}~$1F_{16}$
CD_1	0220_{16}~$023F_{16}$	20_{16}~$3F_{16}$
CD_2	0240_{16}~$025F_{16}$	40_{16}~$5F_{16}$
CD_3	0260_{16}~$027F_{16}$	60_{16}~$7F_{16}$
CD_4	0280_{16}~$029F_{16}$	80_{16}~$9F_{16}$
CD_5	$02A0_{16}$~$02BF_{16}$	$A0_{16}$~BF_{16}

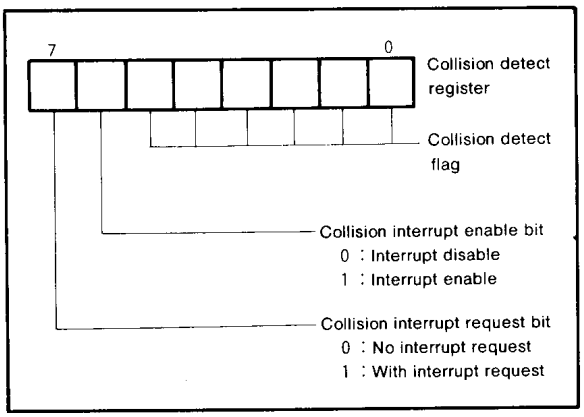


Fig. 6 Structure of collision detect register

INTERRUPT

Interrupts can be caused by 10 different events.

Interrupts are vectored interrupts with priorities shown in Table 4. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed as described in the stack pointer (S) section above, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be inhibited. Other interrupts are disabled when the interrupt inhibit flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1",interrupt request bit is "1", and the interrupt inhibit bit is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 7 shows interrupts control.

All interrupt request bits except the collision detect interrupt are in the interrupt request register (address $00FC_{16}$). The collision detect interrupt request bit is in the collision detect register (address $00FA_{16}$). The interrupt request bit is set when the following conditions occur:

(1) When the data is set to receive buffer of UART1, UART2, or UART3
(2) When the master CPU accesses the IPC mode/IPC error register 0 through bus interface
(3) When the contents of the timer X goes to "0"
(4) When one of the bit 0~bit 5 of the collision detect register is set to "1"
(5) When the data is set to transmit buffer of UART1, UART2, or UART3

There are two interrupt enable bits for each interrupt except collision detect interrupt. One is in interrupt enable register (address $00FB_{16}$), the other is in UART1, UART2, UART3 control register (address $00E6_{16}$, $00EA_{16}$, $00EE_{16}$) or timer control register (address $00FF_{16}$). Interrupts are become enable when these two enable bits are both "1". The collision interrupt enable bit is in bit 6 of collision detect register.

UART transmit interrupt is controlled by $\overline{CTS_1}$, $\overline{CTS_2}$ or $\overline{CTS_3}$ function select bit and $\overline{CTS_1}$, $\overline{CTS_2}$ or $\overline{CTS_3}$ pin input (see UART section).

Since the BRK instruction interrupt and the UART3 transmit interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if UART3 transmit generated the interrupt.

Table 4. Interrupt vector address and priority

Interrupt	Priority	Vector addresses
$\overline{RESET}$	1	$1FFF_{16}$, $1FFE_{16}$
UART1 receive	2	$1FFD_{16}$, $1FFC_{16}$
UART2 receive	3	$1FFB_{16}$, $1FFA_{16}$
UART3 receive	4	$1FF9_{16}$, $1FF8_{16}$
IPCM0	5	$1FF7_{16}$, $1FF6_{16}$
Timer X	6	$1FF5_{16}$, $1FF4_{16}$
Collision detect	7	$1FF3_{16}$, $1FF2_{16}$
UART1 transmit	8	$1FF1_{16}$, $1FF0_{16}$
UART2 transmit	9	$1FEF_{16}$, $1FEE_{16}$
UART3 transmit/ BRK instruction	10	$1FED_{16}$, $1FEC_{16}$

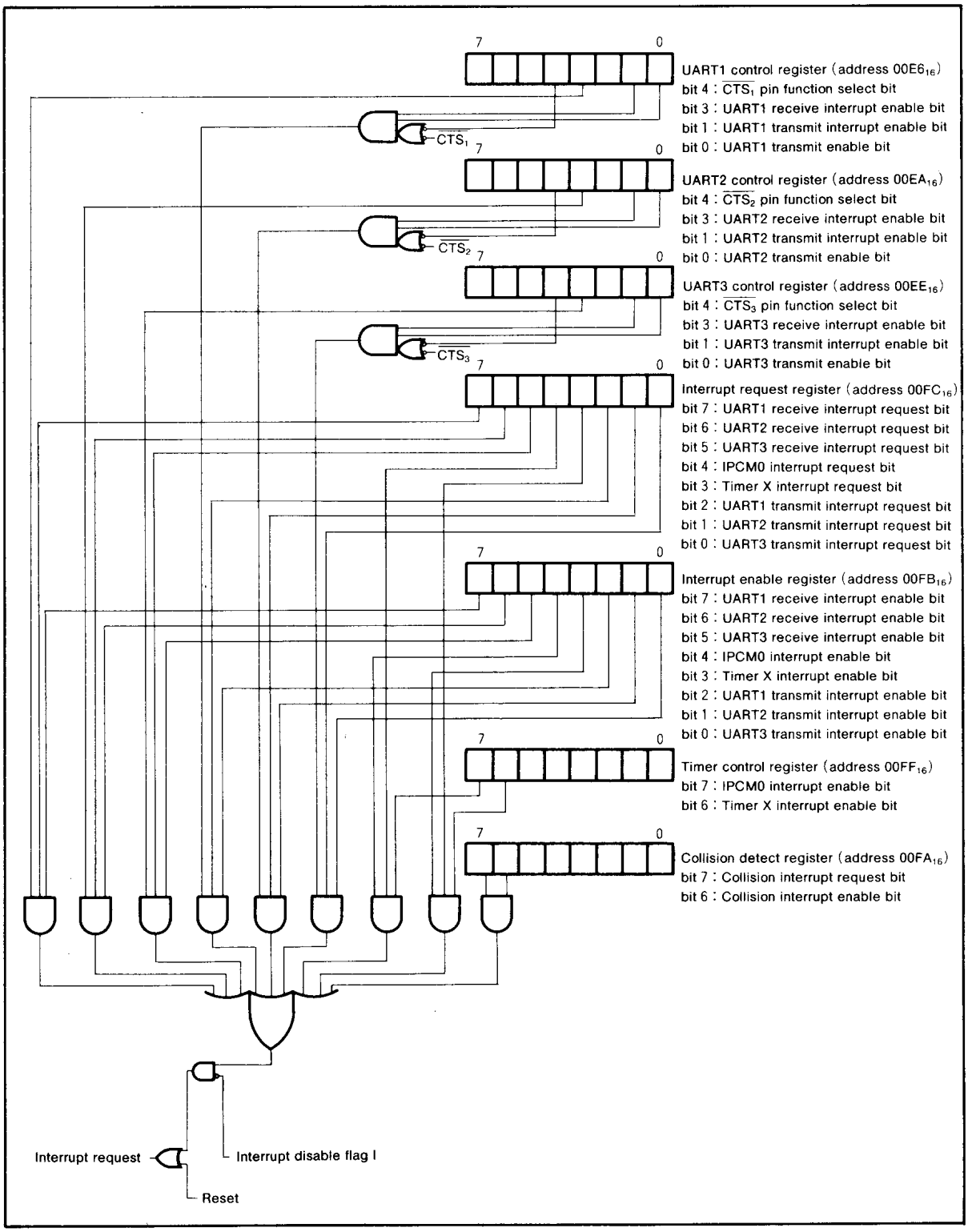


Fig. 7 Interrupt control

TIMER

The M37409M2-XXXSP has one timer: timer X. It has an 8-bit prescaler. Each timer or prescaler is structured with 8-bit counter. A block diagram of timer X is shown in Figure 9. Timer or prescaler is a down-counter which is reloaded from the latch when the next clock pulse after the timer reaches zero. The division ratio is defined as $1/(n+1)$ where n is the decimal contents of the timer latch. The timer interrupt request bit (bit 3 of the address $00FC_{16}$ of local address bus) is also set to "1" at this time. Timer counts the oscillation frequency divided by 16 when the bit 5 of timer control register is "0", and stops when "1". The structure of the timer control register is shown in Figure 8.

When the STP instruction is excuted, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. For more details on the STP instruction, refer to the oscillation circuit section.

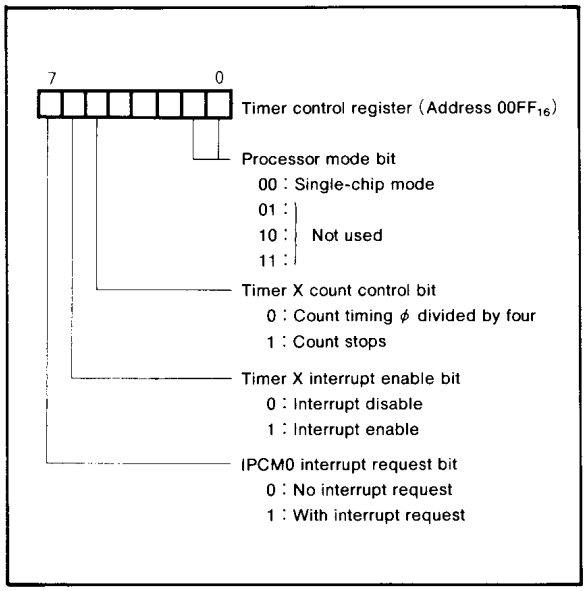


Fig. 8 Structure of timer control register

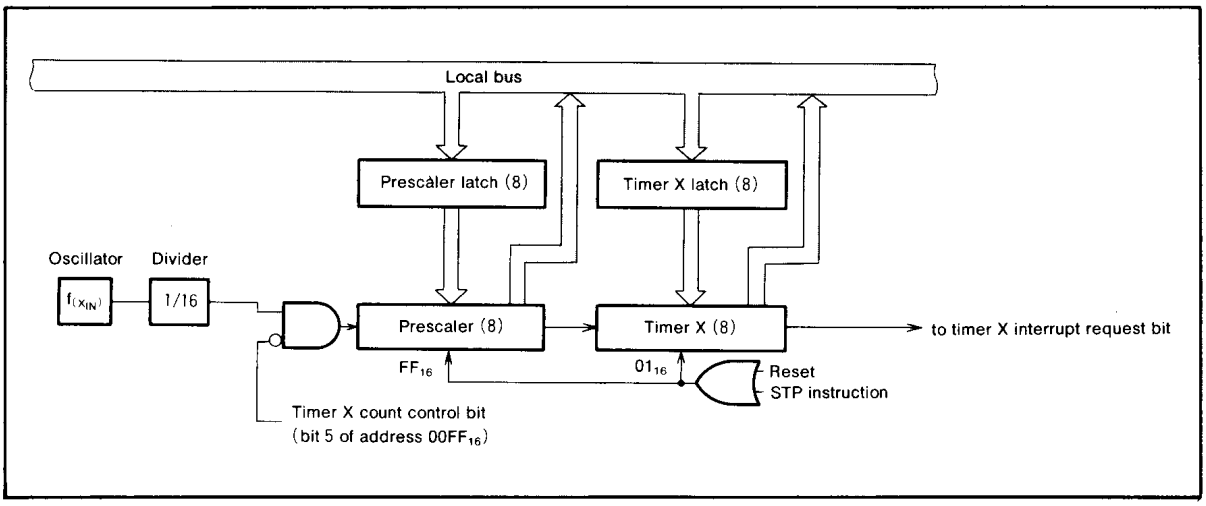


Fig. 9 Timer X block diagram

UART

The M37409M2-XXXSP contains three channels of UART's (UARTi(i=1, 2, 3)). Functionally, they are all equal and can be separately operated. Each channel has three pins (TxDi (transmit output), RxDi(receive input), and $\overline{CTS}$i (clear to send) and contains the receive (transmit) shift register, the receive (transmit) buffer register, the UARTi mode register, the UARTi control register, the UARTi status register, and the baud rate generating divider. It also has a CLK pin (the input pin of the external clock for baud rate generation) which is shared by three channels. An interrupt can be generated on each channel at receive and transmit independently. Figure 10 shows the UARTi block diagram. Because the differences between the channels are only pin numbers and internal addresses, the following description uses UART1 for reference.

[Receive operation]

Setting the receive enable bit (bit 2 of the UART1 control register) to "1" puts the system in the receive enable state. When there is no input of receive data, "H" is input to RxD_1 pin. When the falling edge is input to RxD_1 pin and "L" input is detected twice consecutively by sampling with the clock having a frequency 16 times the baud rate, the start bit is triggered. Then, sampling is performed three time in the middle of the start bit. When "L" is detected twice or more, the receive operation begins, capturing the data bits into the receive shift register. If "L" has not been detected twice or more, start bit detection begins again. When the data bits and parity bit have been captured into the receive shift register and the stop bit is detected, the receive data is transferred from the receive shift register to the receive buffer register, setting the receiver ready flag (bit 1 of the UART1 status register). If a parity error occurred, the parity error flag is set. The framing error flag is set when the first stop bit is found "L". If the previous data has not been read out of the receive buffer register, the overrun error flag is set, clearing the previous data. The receiver ready flag is reset when the receive buffer register is read. Each error flag can be reset by writing "1" to the error flag reset bit (bit 7 of the UART1 control register). Any of these errors does not affect the receive operation. The data bit, the parity bit, and the stop bit are sampled three times in the middle of them each. When "L" or "H" is detected twice or more, "0" or "1" is determined respectively.

Each time a receive operation has been completed, setting the receiver ready flag, the UART1 receive interrupt request bit (bit 7 of the interrupt request register) is set. An interrupt is acknowledged when the two UART1 receive interrupt enable bits (bit 3 of the UART1 control register and bit 7 of the interrupt enable register) are both "1", and the interrupt disable flag I is "0". The UART1 receive interrupt request bit is reset when a UART1 receive interrupt is acknowledged.

Setting the receive enable bit (bit 2 of the UART1 control register) to "0" puts the system in the receive stopped state. At this time, the receiver ready flag is "0" (ready), the receive shift register is in the stopped state, and the start bit detection is stopped.

[Transmit operation]

When the send data is written to the transmit buffer register, the start bit, parity bit, and stop bit are added to the data, which is transferred to the transmit shift register. The transmit shift register begins shift when it becomes enable for transmission, sending the serial data to TxD_1 pin. For the description of the transmit enable state, see Table 5.

In the transmit enable state, each time transmission of the stop bit of the serial data being transmitted has been completed, it is checked whether the next data has been written to the transmit buffer register. If the data is found written, transmission of the next data begins. If the data is found not written, TxD_1 pin is held at "H" until the next transmit data is written, setting the transmitter empty flag. When the transmit enable state is cleared during transmission, the transmission is stopped after completing the transmission of the transmit data so far written to the transmit buffer register.

When the transmitter ready flag (bit 0 of the UART1 status register) is "1", it indicates that the transmit buffer is ready for writing data. The immediately preceding data is transferred from the transmit buffer register to the transmit shift register. Every time the start bit is output from TxD_1 pin, this flag is set. Every time the transmitter ready flag is set, the UART1 transmit interrupt request bit (bit 2 of the interrupt request register) is set. An interrupt is acknowledged when two UART1 transmit interrupt enable bits (bit 3 of the UART1 control register and bit 2 of the interrupt enable register) are both "1" and the interrupt disable flag 1 is "0". Note that an interrupt occurs only in the transmit ready state.

Bit 6 of the UART1 control register initializes the UART1 transmit side. When this bit "0", the transmit side is in the initial state.

Table 5. **Bit and pin states when transmission is enable**

TE_1	$CTSE_1$	$\overline{CTS_1}$
1	0	X
	1	L

TE_1 : UART1 transmit enable bit
$CTSE_1$: $\overline{CTS_1}$ pin function selection bit
$\overline{CTS_1}$: $\overline{CTS_1}$ pin input level

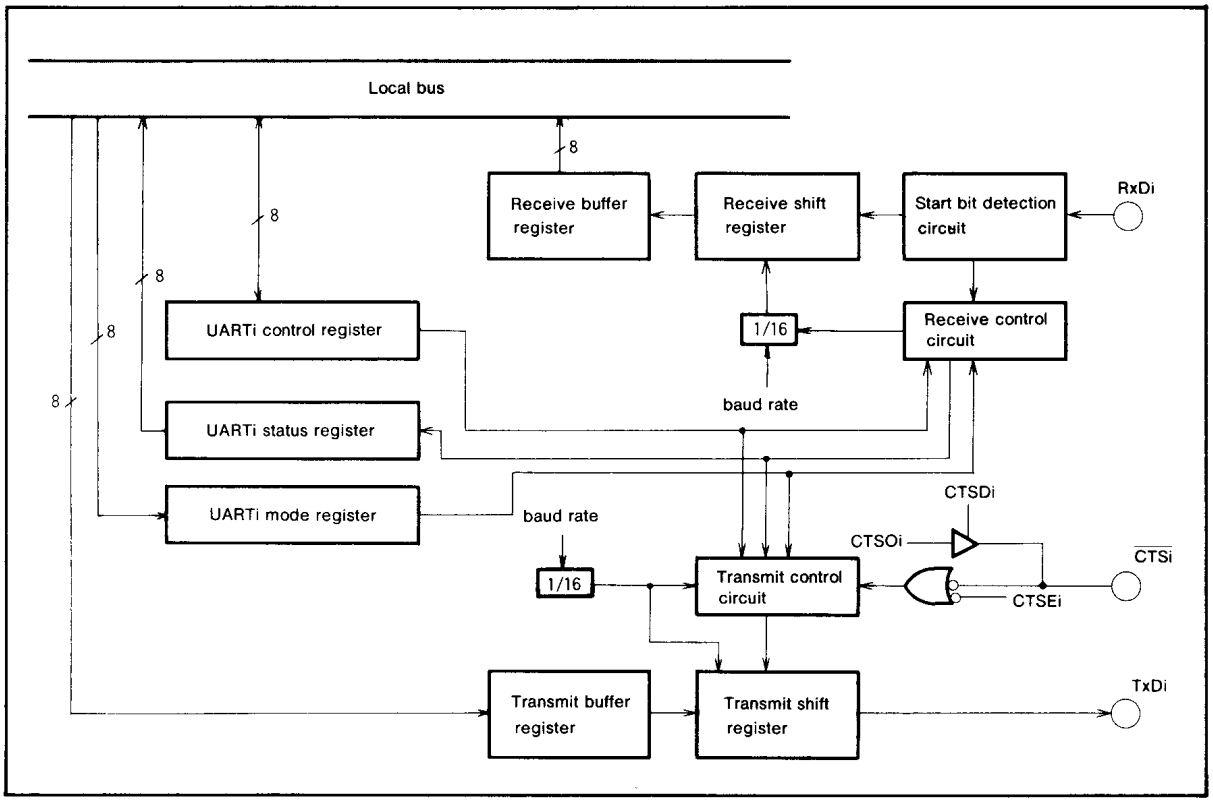


Fig. 10 UARTi block diagram

[UARTi divider for baud rate generator]

This is an 8-bit programmable divider which generates the baud rate for the UARTi receive or transmit operation.

When the setting value is N_{BR} (0 to 255), the divide ratio becomes $1/(N_{BR}+1)$. There are three count sources; X_{IN} clock divided by 2, X_{IN} clock divided by 32, and the external clock. Choose sources by bits 4 and 5 of the UARTi mode register. Table 6 shows the baud rate calculation for each bit combination.

When the external clock is used, the frequency of the input clock must be below 1.6MHz. Writing to the baud rate generating divider must be performed when bits 2 and 6 of the UARTi control register are both "0".

Table 6. Baud rate calculation

EX_i	BR_i	Calculation
0	0	baud rate (bps) $=\frac{f(X_{IN})}{32(N_{BR}+1)}$
0	1	baud rate (bps) $=\frac{f(X_{IN})}{512(N_{BR}+1)}$
1	X	baud rate (bps) $=\frac{f(CLK)}{16(N_{BR}+1)}$

EX_i : Clock selection bit for baud rate generator
BR_i : Divide ratio selection bit for baud rate generator

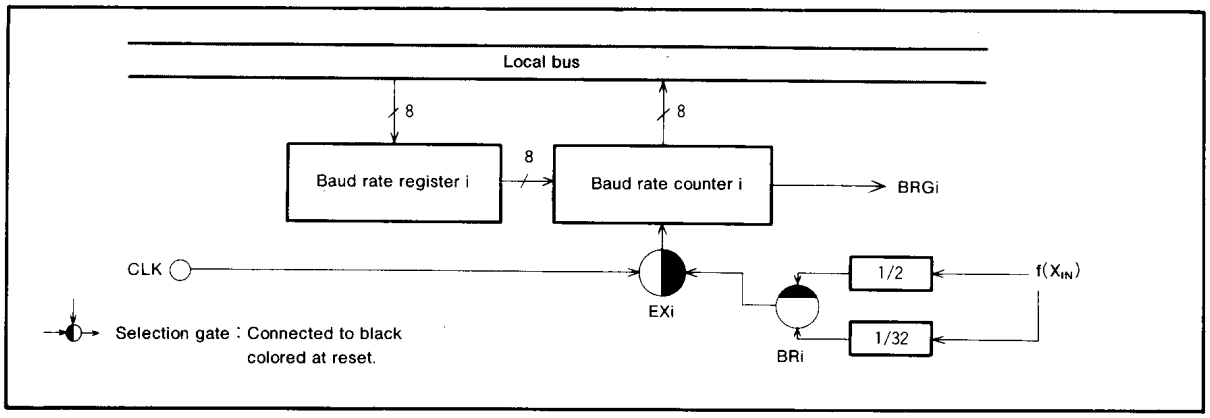


Fig. 11 Baud rate generating circuit

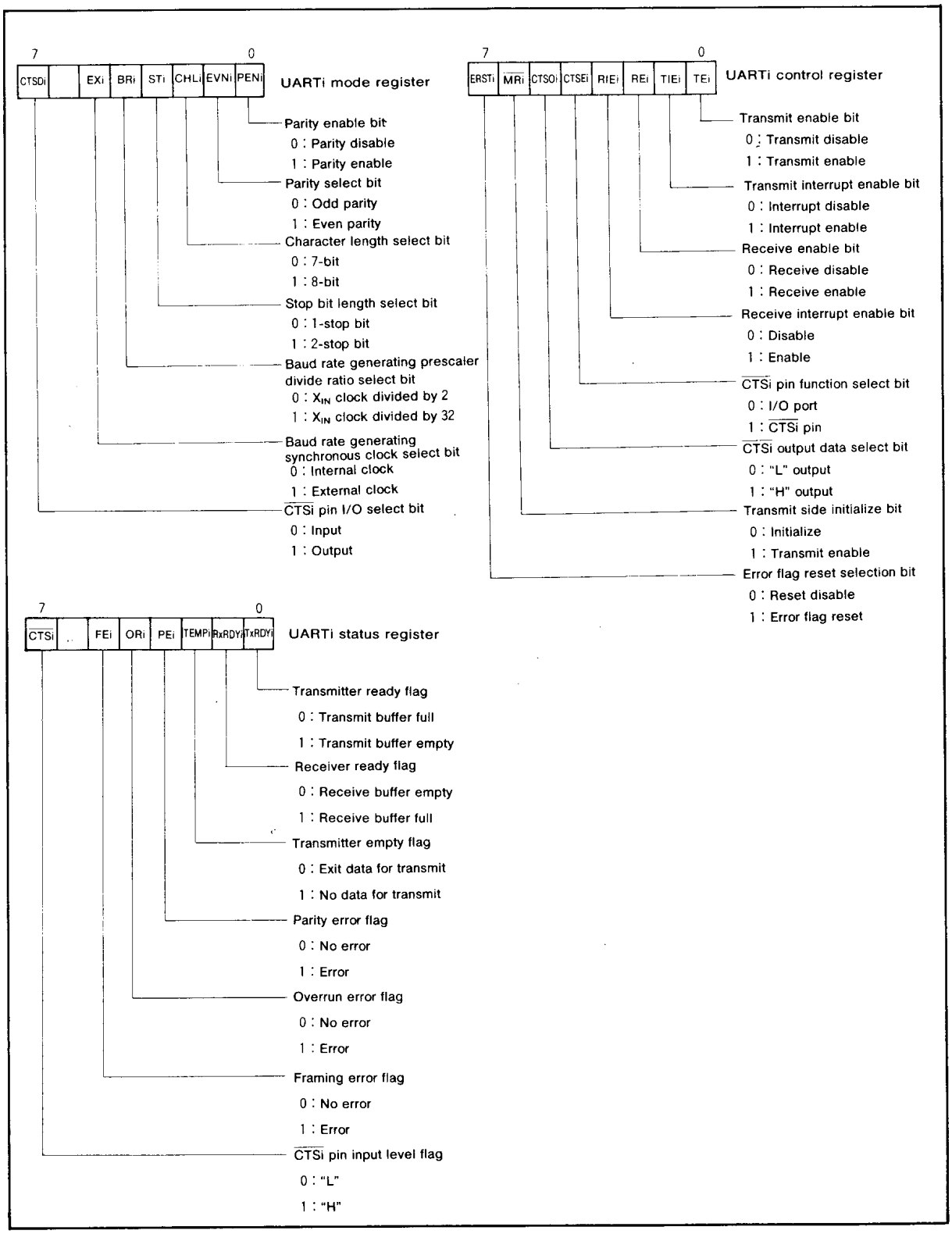


Fig. 12 Structure of registers related to UARTi

[$\overline{\text{CTSi}}$ pin]

The $\overline{\text{CTSi}}$ pin can be used as the 1-bit I/O port when bit 4 of the UARTi control register (CTSEi) is "0". In this case, the input/output direction can be determined by bit 7 of the UARTi mode register (CTSDi) and the output data can be set by bit 5 of the UARTi control register (CTSOi). Additionally, the input level can be known by bit 7 of the UARTi status register (CTSi).

[UARTi mode register]

- Parity enable bit : PENi
  Setting this bit to "1" adds a parity bit to the transmit data. In a receive operation, this bit is used for parity evaluation.
- Parity select bit : EVNi
  This bit specifies the parity bit to be generated in a transmit operation and the parity bit to be evaluated in a receive operation. Depending on the content of this bit, the number of 1's in data is made even or odd.
- Character length select bit : CHLi
  This bit specifies the character length of data.
- Stop bit length select bit : STi
  This bit specifies the stop bit length.
- Baud rate generating prescaler divide ratio select bit : BRi
  When this bit is "0", the signal obtained by dividing X_{IN} clock by 2 becomes the count source of the baud rate divider. When this bit is "1", the signal is obtained by dividing the clock by 32.
- Baud rate generating synchronous clock selection bit : EXi
  This bit specifies baud rate synchronous clock. When this bit is "1", external clock is input from the CLK pin.
- $\overline{\text{CTSi}}$ pin I/O select bit : CTSDi
  When this bit is "0", the $\overline{\text{CTSi}}$ pin is the input pin.
  When this bit is "1", the pin is the output pin. To use the $\overline{\text{CTSi}}$ pin as the $\overline{\text{CTSi}}$ input, set "0".

[UARTi control register]

- Transmit enable bit : TEi
  Setting this bit to "1" enables a transmit operation.
- Transmit interrupt enable bit : TIEi
  When this bit is "1", the interrupt in a transmit operation is enabled.
- Receive enable bit : REi
  Setting this bit to "1" enables a receive operation.
- Receive interrupt enable bit : RIEi
  When this bit is "1", the interrupt in a receive operation is enabled.
- $\overline{\text{CTSi}}$ pin function select bit : CTSEi
  When this bit is "1", the $\overline{\text{CTSi}}$ pin becomes the $\overline{\text{CTSi}}$ input.
- $\overline{\text{CTSi}}$ output data select bit : CTSOi
  When this bit is "0", "L" is output. When it is "1", "H" is output.
- Transmit side initialize bit : MRi
  When this bit is "0", the transmit side is initialized.
- Error flag reset select bit : ERSTi
  Setting this bit to "1" resets all error flags. When this bit is read, "0" is always read.

[UARTi status register]

- Transmitter ready flag : TxRDYi
  When this flag is "1", it indicates that the transmit buffer register is empty and ready for writing transmit data.
- Receiver ready flag : RxRDYi
  When this flag is "1", it indicates that the receive buffer register is holding receive data. When the receive buffer register is read, it is cleared.
- Transmitter empty flag : TEMPi
  When this flag is "1", it indicates that neither the transmit shift register nor the transmit buffer register holds the data to be transmitted.
- Parity error flag : PEi
  This bit is set to "1" when the parity of the received data is different from the parity which was set.
- Overrun error flag : ORi
  When this flag is "1", it indicates that, before the data in the receive buffer register is read, the next data is transferred from the receive shift register to the receive buffer register and the previous data is lost.
- Framing error flag : FEi
  This flag is set to "1" when the stop bit is found "L" when data is transferred from the receive shift register to the receive buffer register.
- $\overline{\text{CTSi}}$ pin input level flag : $\overline{\text{CTSi}}$
  When the input level of the $\overline{\text{CTSi}}$ pin is "L", "0" is read; when it is "H", "1" is read.

RESET CIRCUIT

The M37409M2-XXXSP is reset according to the sequence shown in Figure 14. It starts the program from the address formed by using the content of address $1FFF_{16}$ as the high order address and the content of the address $1FFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than $2\mu s$ while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 15 and 16.

An example of the reset circuit is shown in Figure 13.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

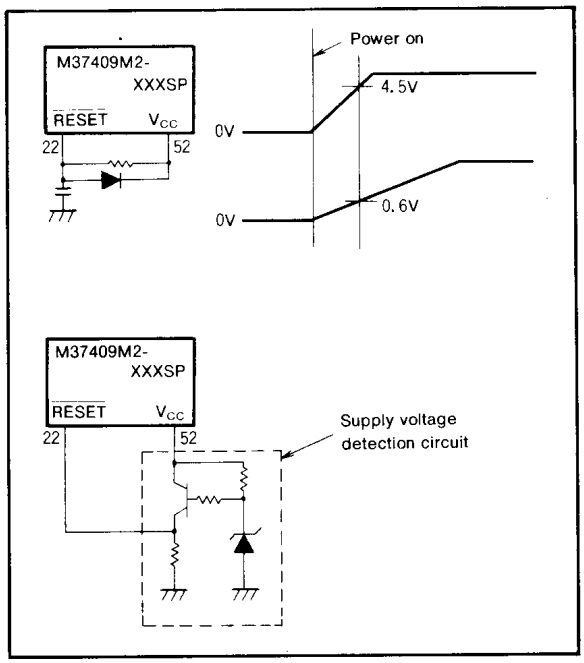


Fig. 13 Example of reset circuit

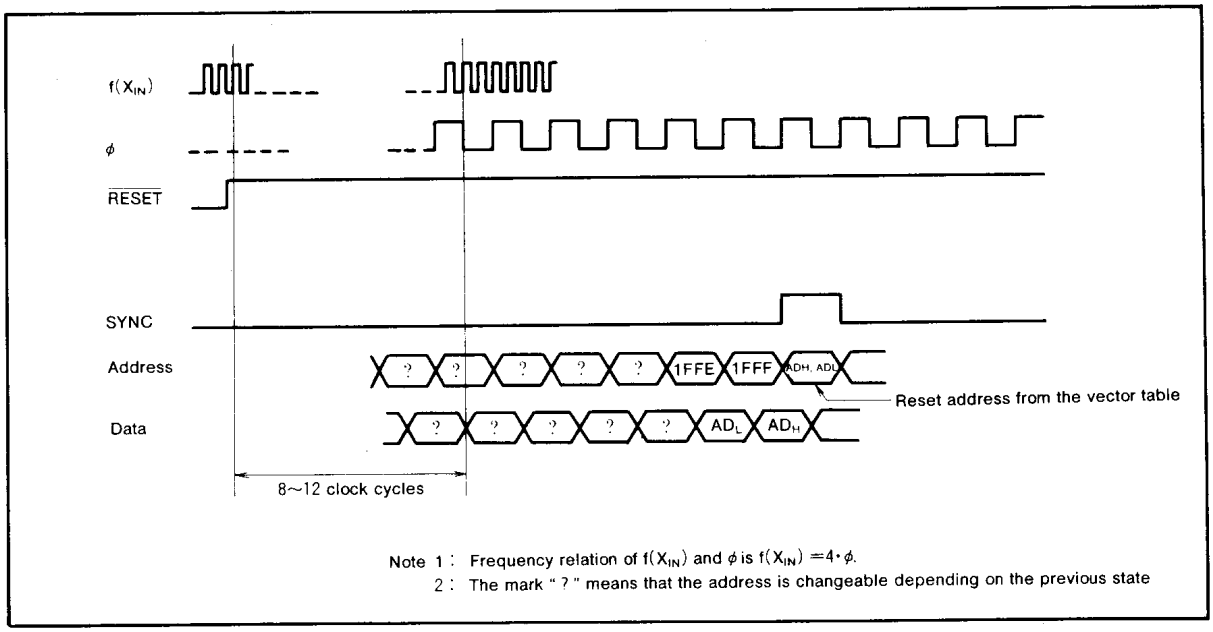


Fig.14 Timing diagram at reset

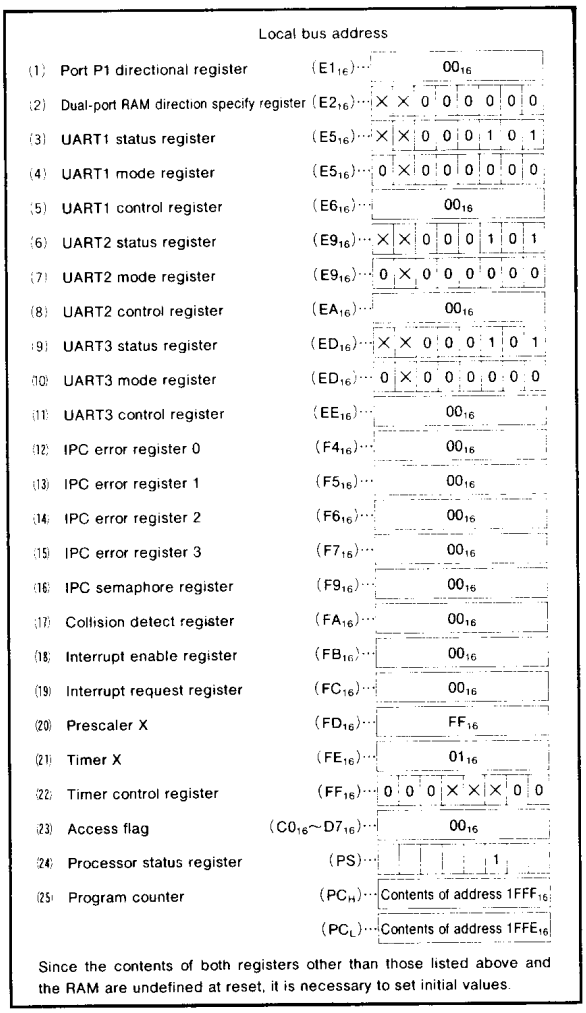


Fig.15 Internal state of microcomputer at reset (1)

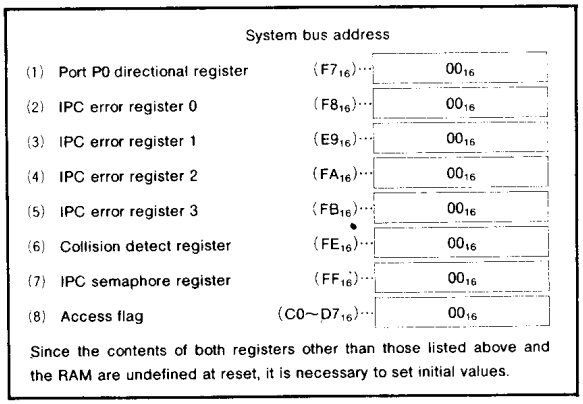


Fig.16 Internal state of microcomputer at reset (2)

I/O PORTS

(1) Port P0 System bus : address $F6_{16}$

Port P0 is an 8-bit I/O port with CMOS output. It can be accessed from system bus only and can not be accessed from local bus.

As shown in the memory map (Figure 1), port P0 can be accessed at system bus address $F6_{16}$. Port P0 has a directional register (address $F7_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state. This port becomes input at reset.

(2) Port P1 Local bus : address $00E0_{16}$
System bus : address $F5_{16}$

Port P1 is an 8-bit I/O port and connected to local bus. It has the same function as port P0 except the connected bus.

It's directional register is at local bus address $00E1_{16}$.

Also port P1 can be read from system bus but the pin state is read regardless the value of the port P1 directional register.

(3) Address pins

Address pins $A_0 \sim A_7$ are the input pins directly connected to the system bus. The 8-bit address corresponding to the system bus is input to these pins. The input level is TTL.

(4) Data pins

Data pins $D_0 \sim D_7$ are the output pins directly connected to the system bus. The 8-bit data corresponding to the system bus is input/output on these pins. When the $\overline{CS}$ pin is "L" and the $\overline{RD}$ pin is "L", the data pins become the output pins. When the $\overline{CS}$ pin is "L" and the $\overline{WR}$ pin is "L", the data pins become the input pins. Setting the $\overline{CS}$ pin to "H" puts pins $D_0 \sim D_7$ in the floating state. The I/O level is TTL.

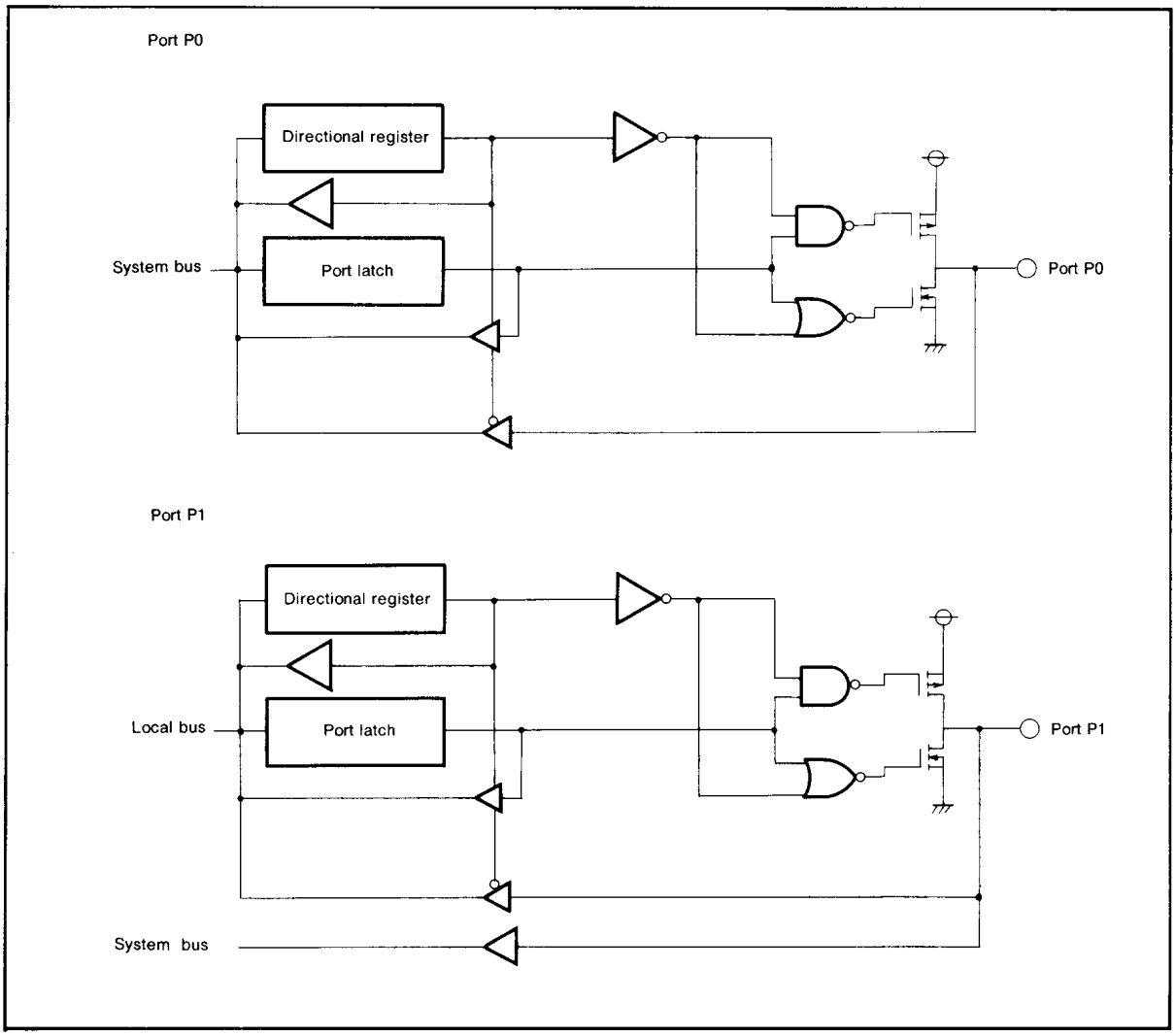


Fig. 17 Port P0, P1 block diagram

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 18.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleard when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 19 and 20.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock uasge is shown in Figure 21. X_{IN} is the input, and X_{OUT} is open.

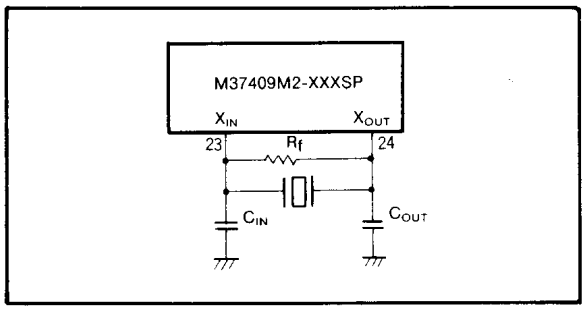


Fig. 19 External ceramic resonator circuit

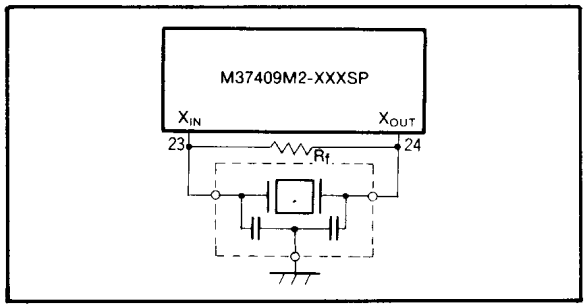


Fig. 20 External ceramic resonator circuit (capacity built-in type)

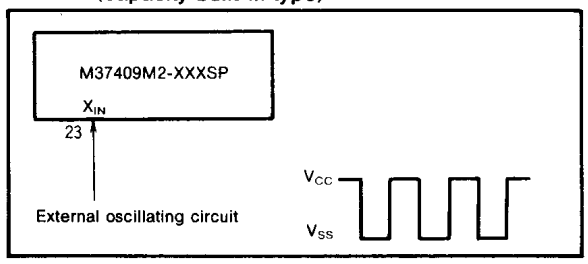


Fig. 21 External clock input circuit

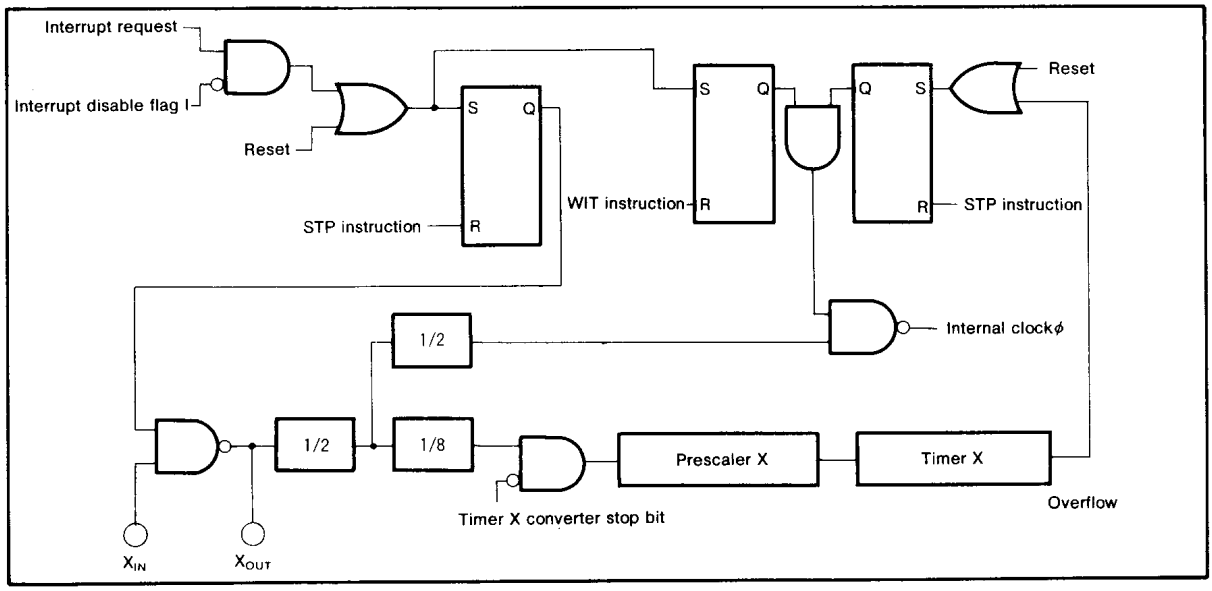


Fig. 18 Block diagram of clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is $1/(n+1)$.

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) Change the address $A_0 \sim A_7$ input and the $\overline{CS}$ input when both the $\overline{RD}$ input and $\overline{WR}$ input are "H".

(4) Registers whose values change when read, are connected to the system bus of the M37409M2-XXXSP. If the master CPU generates an invalid read cycle, data is not correctly transferred.

(5) A NOP instruction must be used after the execution of a PLP instruction.

(6) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(7) The STP instruction must be executed after setting timer X count enable bit to enable "0", timer X interrupt enable bit to inhibit ("0"), and timer X interrupt request bit to no request ("0").

(8) The power current is max. 10mA in DC. However, because a rush current and a bus charge-discharge current flow transiently, a bypass capacitor must be connected between V_{SS} and V_{CC}.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mark specification form

(3) ROM data ..... EPROM 3sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors cut-off	−0.3~7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}		−0.3~7	V
V_I	Input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, D_0~D_7, A_0~A_7, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, CLK, R_XD_1~R_XD_3, $\overline{CTS_1}$~$\overline{CTS_3}$		−0.3~V_{CC}+0.3	V
V_I	Input voltage, CNV_{SS}		−0.3~13	V
V_O	Output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, X_{OUT}, ϕ, D_0~D_7, T_XD_1~T_XD_3, $\overline{CTS_1}$~$\overline{CTS_3}$		−0.3~V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
T_{opr}	Operating temperature		−10~70	℃
T_{stg}	Storage temperature		−40~125	℃

Note 1 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5V±10%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage X_{IN}, $\overline{RESET}$, CLK, $P0_0$~$P0_7$, $P1_0$~$P1_7$, R_XD_1~R_XD_3, $\overline{CTS_1}$~$\overline{CTS_3}$	0.8V_{CC}		V_{CC}+0.3	V
V_{IH}	"H" input voltage A_0~A_7, D_0~D_7, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$	2		V_{CC}+0.3	V
V_{IL}	"L" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, CLK, R_XD_1~R_XD_3, $\overline{CTS_1}$~$\overline{CTS_3}$	−0.3		0.2V_{CC}	V
V_{IL}	"L" input voltage A_0~A_7, D_0~D_7, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$	−0.3		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	−0.3		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	−0.3		0.16V_{CC}	V
I_{OH}	"H" output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, ϕ, T_XD_1~T_XD_3, $\overline{CTS_1}$~$\overline{CTS_3}$			−10	mA
I_{OH}	"H" output current D_0~D_7			−1.0	mA
I_{OL}	"L" output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, ϕ, T_XD_1~T_XD_3, $\overline{CTS_1}$~$\overline{CTS_3}$			10	mA
I_{OL}	"L" output current D_0~D_7			−1.6	mA

Note 2 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms
3 : Total of $I_{OL(peak)}$, of ports P0, P1, T_XD_1~T_XD_3 and $\overline{CTS_1}$~$\overline{CTS_3}$ is −50mA
Total of $I_{OH(peak)}$, of ports P0, P1, T_XD_1~T_XD_3 and $\overline{CTS_1}$~$\overline{CTS_3}$ is 50mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{SS} = 0V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, ϕ, TxD_1~TxD_3, $\overline{CTS_1}$~$\overline{CTS_3}$	I_{OH}=−10mA		V_{CC}−2			V
V_{OH}	"H" output voltage D_0~D_7	I_{OH}=−1mA		2.4			V
V_{OL}	"L" output voltage $P0_0$~ $P0_7$, $P1_0$~$P1_7$, ϕ, TxD_1~TxD_3, $\overline{CTS_1}$~$\overline{CTS_3}$	I_{OL}=10mA				2	V
V_{OL}	"L" output voltage D_0~D_7	I_{OL}=1.6mA				0.4	V
I_I	Input leak current A_0~A_7, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, CLK	V_{SS}≦V_I≦V_{CC}		−5		5	μA
I_I	Input leak current $\overline{RESET}$, X_{IN}	V_{SS}≦V_I≦7V		−5		5	μA
I_{OZ}	Tri-state leak current $P0_0$~$P0_7$, $P1_0$~$P1_7$, D_0~D_7, $\overline{CTS_1}$~$\overline{CTS_3}$	V_{SS}+0.5≦V_O≦V_{CC}−0.5V		−5		5	μA
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$, CLK, R_xD_1~R_xD_3, $\overline{CTS_1}$~$\overline{CTS_3}$				0.6		V
I_{CC}	Supply current	Output terminals are opened, others to V_{SS}, $\overline{CS}$=V_{CC}	$f_{(X_{IN})}$=8~10MHz Square wave			10	mA
			ditto (wait mode)			1	mA
			At stop mode T_a = 25℃			1	μA
			At stop mode T_a = 70℃			10	μA

TIMING REQUIREMENTS

System bus (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, f(X_{IN})=5~10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(A-WR)}$	A_0~A_7 $\overline{CS}$ input set-up time	Fig. 22	50			ns
$t_{SU(A-RD)}$	A_0~A_7 $\overline{CS}$ input set-up time		50			ns
$t_{SU(D-WR)}$	D_0~D_7 input set-up time		80			ns
$t_{h(WR-A)}$	A_0~A_7 $\overline{CS}$ input hold time		0			ns
$t_{h(RD-A)}$	A_0~A_7 $\overline{CS}$ input hold time		0			ns
$t_{h(WR-D)}$	D_0~D_7 input hold time		10			ns
$t_{W(WR)}$	$\overline{WR}$ input "L" pulse width		200			ns
$t_{W(RD)}$	$\overline{RD}$ input "L" pulse width		200			ns

Local bus (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, f(X_{IN})=5~10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(P1-\phi)}$	$P1_0$~$P1_7$ input set-up time	Fig. 22	300			ns
$t_{h(\phi-P1)}$	$P1_0$~$P1_7$ input hold time		50			ns

SWITCHING CHARACTERISTICS

System bus (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, f(X_{IN})=5~10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(D-RD)}$	D_0~D_7 output delay time	Fig. 22			150	ns
$t_{v(D-RD)}$	D_0~D_7 output effective time		0			ns
$t_{en(RD-D)}$	D_0~D_7 output enable time		10			ns
$t_{dis(RD-D)}$	D_0~D_7 output disable time				50	ns

Local bus (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, f(X_{IN})=5~10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P1)}$	$P1_0$~$P1_7$ output delay time	Fig. 22			300	ns

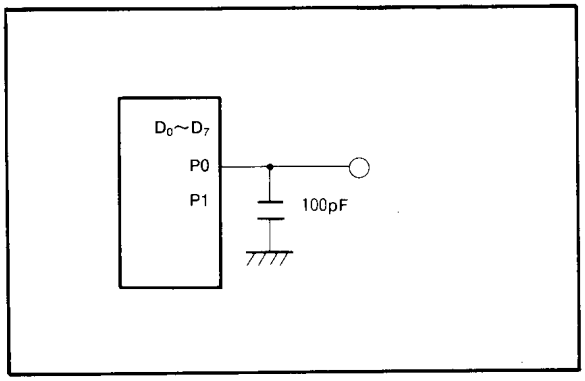
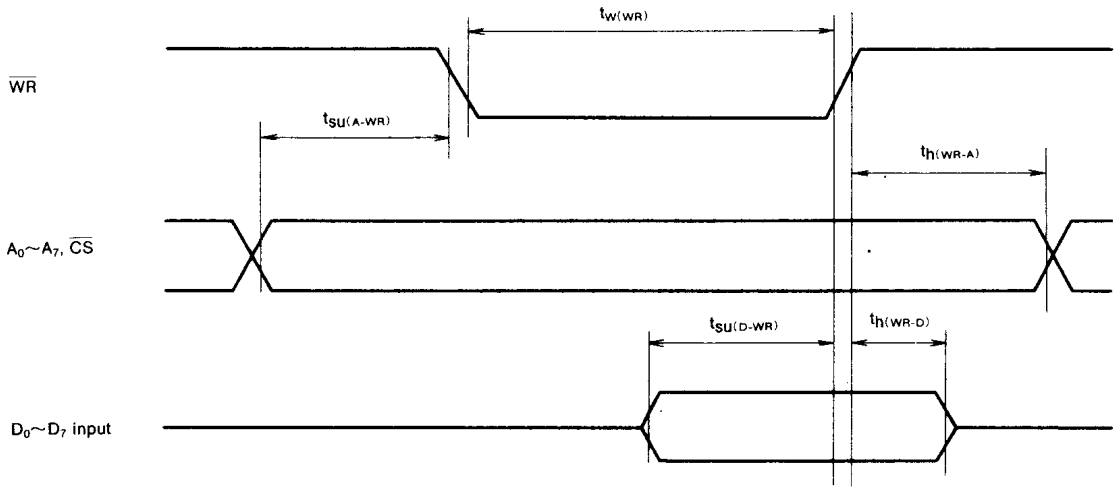


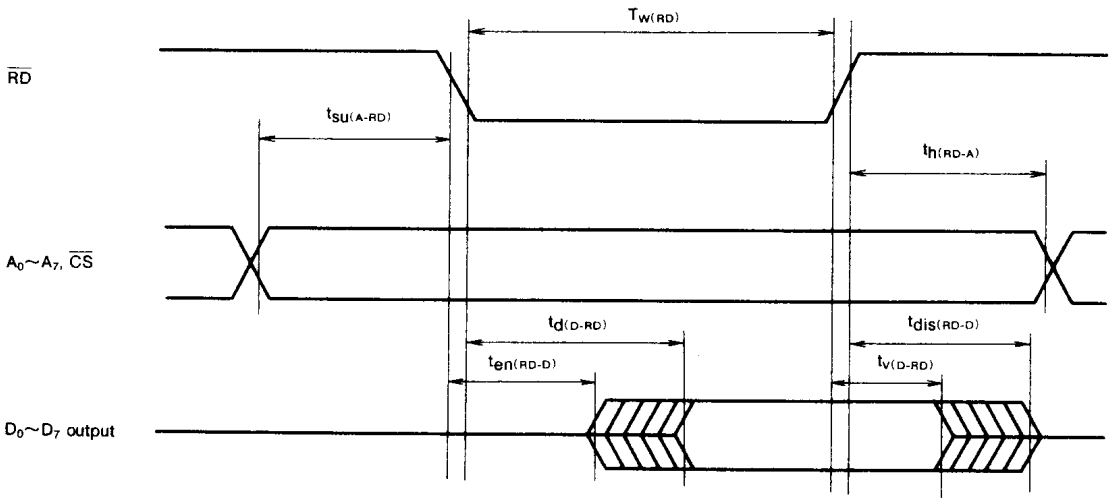
Fig. 22 Port P0, P1, D_0~D_7 test circuit

TIMING DIAGRAMS

System bus write cycle



System bus read cycle



Local bus