M50LPW002

2 Mbit (256Kb x8, Boot Block)
3V Supply Low Pin Count Flash Memory

PRELIMINARY DATA

FEATURES SUMMARY

■ SUPPLY VOLTAGE
- V_{CC} = 3 V to 3.6 V for Program, Erase and Read Operations
- V_{PP} = 12 V for Fast Program and Fast Erase (optional)

■ TWO INTERFACES
- Low Pin Count (LPC) Standard Interface for embedded operation with PC Chipsets.
- Address/Address Multiplexed (A/A Mux) Interface for programming equipment compatibility.

■ LOW PIN COUNT (LPC) HARDWARE INTERFACE MODE
- 5 Signal Communication Interface supporting Read and Write Operations
- Hardware Write Protect Pins for Block Protection
- Register Based Read and Write Protection
- 5 Additional General Purpose Inputs for platform design flexibility
- Synchronized with 33 MHz PCI clock

■ PROGRAMMING TIME
- 10 µs typical
- Quadruple Byte Programming Option

■ 7 MEMORY BLOCKS
- 1 Boot Block (Top Location)
- 4 Main Blocks and 2 Parameter Blocks
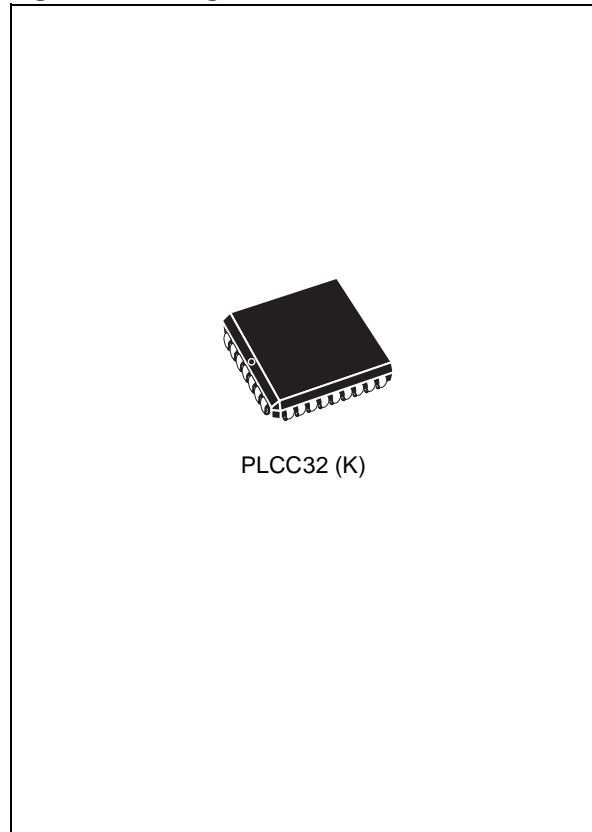
■ PROGRAM/ERASE CONTROLLER
- Embedded Byte Program, Block Erase and Chip Erase algorithms
- Status Register Bits

■ PROGRAM and ERASE SUSPEND
- Read other Blocks during Program/Erase Suspend
- Program other Blocks during Erase Suspend

■ FOR USE in PC BIOS APPLICATIONS

Figure 1. Packages

PLCC32 (K)

■ ELECTRONIC SIGNATURE
- Manufacturer Code: 20h
- Device Code: 31h

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SUMMARY DESCRIPTION

The M50LPW002 is a 2 Mbit (256Kb x8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (3.0 to 3.6V) supply. For fast programming and fast erasing in production lines an optional 12V power supply can be used to reduce the programming and the erasing times.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Blocks can be protected individually to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

The device features an asymmetrical blocked architecture. The device has an array of 7 blocks:

- 1 Boot Block of 16 KByte
- 2 Parameter Blocks of 8 KByte each
- 1 Main Block of 32 KByte
- 3 Main Blocks of 64 KByte each

Two different bus interfaces are supported by the memory. The primary interface is the Low Pin Count (or LPC) Standard Interface. This has been designed to remove the need for the ISA bus in current PC Chipsets; the M50LPW002 acts as the PC BIOS on the Low Pin Count bus for these PC Chipsets.

The secondary interface, the Address/Address Multiplexed (or A/A Mux) Interface, is designed to be compatible with current Flash Programmers for production line programming prior to fitting to a PC Motherboard.

The memory is delivered with all the bits erased (set to 1).

Figure 2. PLCC Connections

Note: Pins 27 and 28 are not internally connected.

Figure 3. Logic Diagram (LPC Interface)

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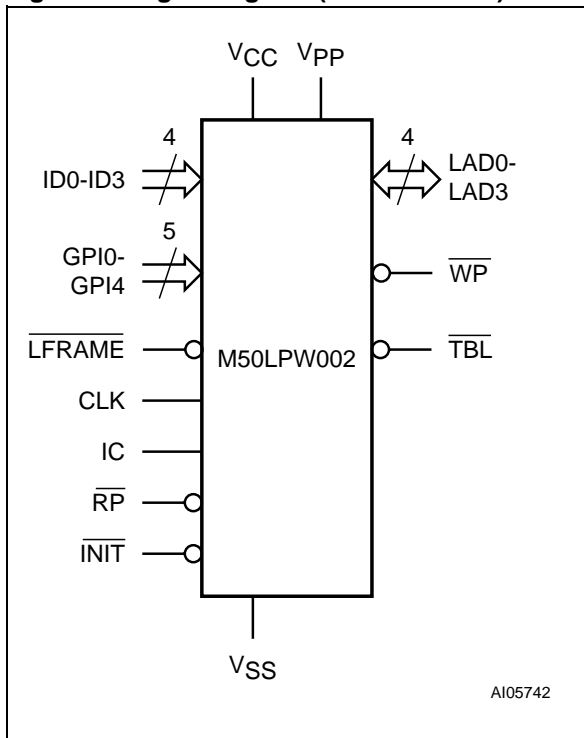
Figure 4. Logic Diagram (A/A Mux Interface)

AI05743
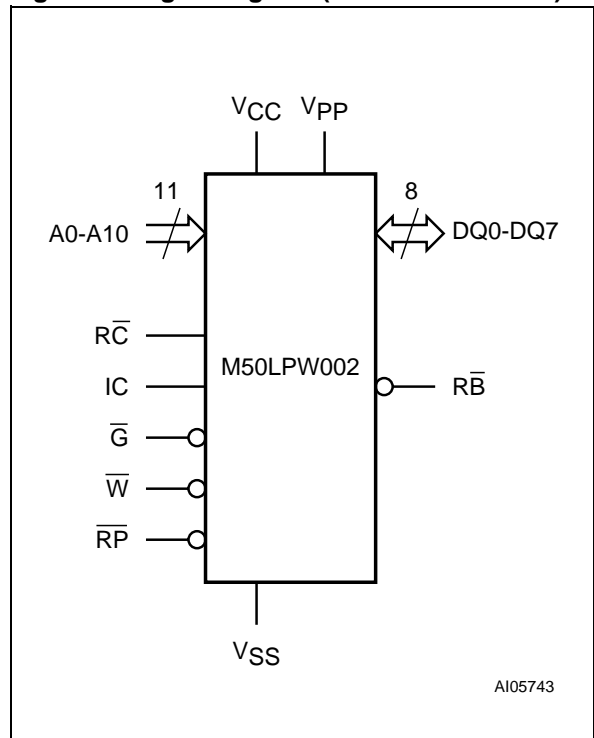
Table 1. Signal Names (LPC Interface)

LAD0-LAD3	Input/Output Communications
$\overline{\text{LFRAME}}$	Input Communication Frame
ID0-ID3	Identification Inputs
GPI0-GPI4	General Purpose Inputs
IC	Interface Configuration
$\overline{\text{RP}}$	Interface Reset
$\overline{\text{INIT}}$	CPU Reset
CLK	Clock
$\overline{\text{TBL}}$	Top Block Lock
$\overline{\text{WP}}$	Write Protect
RFU	Reserved for Future Use. Leave disconnected
V_{CC}	Supply Voltage
V_{PP}	Optional Supply Voltage for Fast Erase Operations
V_{SS}	Ground
NC	Not Connected Internally

Table 2. Signal Names (A/A Mux Interface)

IC	Interface Configuration
A0-A10	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
$\overline{\text{G}}$	Output Enable
$\overline{\text{W}}$	Write Enable
R$\overline{\text{C}}$	Row/Column Address Select
R$\overline{\text{B}}$	Ready/Busy Output
$\overline{\text{RP}}$	Interface Reset
V_{CC}	Supply Voltage
V_{PP}	Optional Supply Voltage for Fast Program and Fast Erase Operations
V_{SS}	Ground
NC	Not Connected Internally

SIGNAL DESCRIPTIONS

There are two different bus interfaces available on this part. The active interface is selected before power-up or during Reset using the Interface Configuration Pin, IC.

The signals for each interface are discussed in the Low Pin Count (LPC) Signal Descriptions section and the Address/Address Multiplexed (A/A Mux) Signal Descriptions section below. The supply signals are discussed in the Supply Signal Descriptions section below.

Low Pin Count (LPC) Signal Descriptions

For the Low Pin Count (LPC) Interface see Figure 3, Logic Diagram, and Table 1, Signal Names.

Input/Output Communications (LAD0-LAD3). All Input and Output Communication with the memory take place on these pins. Addresses and Data for Bus Read and Bus Write operations are encoded on these pins.

Input Communication Frame ($\overline{\text{LFRAME}}$). The Input Communication Frame ($\overline{\text{LFRAME}}$) signals the start of a bus operation. When Input Communication Frame is Low, V_{IL}, on the rising edge of the Clock a new bus operation is initiated. If Input Communication Frame is Low, V_{IL}, during a bus operation then the operation is aborted. When Input Communication Frame is High, V_{IH}, the current bus operation is proceeding or the bus is idle.

Identification Inputs (ID0-ID3). The Identification Inputs (ID0-ID3) allow to address up to 16 memories on a bus. The value on addresses A18-A21 is compared to the hardware strapping on the ID0-ID3 pins to select which memory is being addressed. For an address bit to be '1' the correspondent ID pin can be left floating or driven Low, V_{IL}; an internal pull-down resistor is included with a value of R_{IL}. For an address bit to be '0' the correspondent ID pin must be driven High, V_{IH}; there will be a leakage current of I_{LI2} through each pin when pulled to V_{IH}; see Table 20.

By convention the boot memory must have ID0-ID3 pins left floating or driven Low, V_{IL} and a '1111' value on A18-A21 and all additional memories take sequential ID0-ID3 configuration, as shown in Table 3.

General Purpose Inputs (GPI0-GPI4). The General Purpose Inputs can be used as digital inputs for the CPU to read. The General Purpose Input Register holds the values on these pins. The pins must have stable data from before the start of the cycle that reads the General Purpose Input Register until after the cycle is complete. These pins must not be left to float, they should be driven Low, V_{IL}, or High, V_{IH}.

Interface Configuration (IC). The Interface Configuration input selects whether the Low Pin Count (LPC) or the Address/Address Multiplexed (A/A Mux) Interface is used. The chosen interface must be selected before power-up or during a Reset and, thereafter, cannot be changed. The state of the Interface Configuration, IC, should not be changed during operation.

To select the Low Pin Count (LPC) Interface the Interface Configuration pin should be left to float or driven Low, V_{IL}; to select the Address/Address Multiplexed (A/A Mux) Interface the pin should be driven High, V_{IH}. An internal pull-down resistor is included with a value of R_{IL}; there will be a leakage current of I_{LI2} through each pin when pulled to V_{IH}; see Table 20.

Interface Reset ($\overline{\text{RP}}$). The Interface Reset ($\overline{\text{RP}}$) input is used to reset the memory. When Interface Reset ($\overline{\text{RP}}$) is set Low, V_{IL}, the memory is in Reset mode: the outputs are put to high impedance and the current consumption is minimized. When $\overline{\text{RP}}$ is set High, V_{IH}, the memory is in normal operation. After exiting Reset mode, the memory enters Read mode.

CPU Reset ($\overline{\text{INIT}}$). The CPU Reset, $\overline{\text{INIT}}$, pin is used to Reset the memory when the CPU is reset. It behaves identically to Interface Reset, $\overline{\text{RP}}$, and the internal Reset line is the logical OR (electrical AND) of $\overline{\text{RP}}$ and $\overline{\text{INIT}}$.

Clock (CLK). The Clock, CLK, input is used to clock the signals in and out of the Input/Output Communication Pins, LAD0-LAD3. The Clock conforms to the PCI specification.

Top Block Lock ($\overline{\text{TBL}}$). The Top Block Lock input is used to prevent the Top Block (Block 6) from being changed. When Top Block Lock, $\overline{\text{TBL}}$, is set Low, V_{IL}, Program and Erase operations in the Top Block have no effect, regardless of the state of the Lock Register. When Top Block Lock, $\overline{\text{TBL}}$, is set High, V_{IH}, the protection of the Block is determined by the Lock Register. The state of Top Block Lock, $\overline{\text{TBL}}$, does not affect the protection of the other blocks (Blocks 0 to 5).

Top Block Lock, $\overline{\text{TBL}}$, must be set prior to a Program or Erase operation is initiated and must not be changed until the operation completes or unpredictable results may occur. Care should be taken to avoid unpredictable behavior by changing $\overline{\text{TBL}}$ during Program or Erase Suspend.

Write Protect ($\overline{\text{WP}}$). The Write Protect input is used to prevent the blocks 0 to 5 from being changed. When Write Protect, $\overline{\text{WP}}$, is set Low, V_{IL}, Program and Erase operations in these blocks have no effect, regardless of the state of the Lock Register. When Write Protect, $\overline{\text{WP}}$, is set High, V_{IH}, the protection of the block is determined by the Lock Register. The state of Write Protect, $\overline{\text{WP}}$, does not affect the protection of the Top Block (Block 6).

Write Protect, $\overline{WP}$, must be set prior to a Program or Erase operation is initiated and must not be changed until the operation completes or unpredictable results may occur. Care should be taken to avoid unpredictable behavior by changing $\overline{WP}$ during Program or Erase Suspend.

Reserved for Future Use (RFU). These pins do not have assigned functions in this revision of the part. They must be left disconnected.

Address/Address Multiplexed (A/A Mux) Signal Descriptions

For the Address/Address Multiplexed (A/A Mux) Interface see Figure 4, Logic Diagram, and Table 2, Signal Names.

Address Inputs (A0-A10). The Address Inputs are used to set the Row Address bits (A0-A10) and the Column Address bits (A11-A17). They are latched during any bus operation by the Row/Column Address Select input, $R\overline{C}$.

Data Inputs/Outputs (DQ0-DQ7). The Data Inputs/Outputs hold the data that is written to or read from the memory. They output the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine. The Data Inputs/Outputs, DQ0-DQ7, are latched during a Bus Write operation.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, controls the Bus Read operation of the memory.

Write Enable ($\overline{W}$). The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command Interface.

Row/Column Address Select (R$\overline{C}$). The Row/Column Address Select input selects whether the Address Inputs should be latched into the Row Address bits (A0-A10) or the Column Address bits (A11-A17). The Row Address bits are latched on the falling edge of R$\overline{C}$ whereas the Column Address bits are latched on the rising edge.

Ready/Busy Output (R$\overline{B}$). The Ready/Busy pin gives the status of the memory's Program/Erase Controller. When Ready/Busy is Low, V_{OL}, the memory is busy with a Program or Erase operation and it will not accept any additional Program or Erase command except the Program/Erase

Suspend command. When Ready/Busy is High, V_{OH}, the memory is ready for any Read, Program or Erase operation.

Supply Signal Descriptions

The Supply Signals are the same for both interfaces.

V$_{CC}$ Supply Voltage. The V_{CC} Supply Voltage supplies the power for all operations (Read, Program, Erase etc.).

The Command Interface is disabled when the V_{CC} Supply Voltage is less than the Lockout Voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid. After V_{CC} becomes valid the Command Interface is reset to Read mode.

A 0.1µF capacitor should be connected between the V_{CC} Supply Voltage pins and the V_{SS} Ground pin to decouple the current surges from the power supply. Both V_{CC} Supply Voltage pins must be connected to the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

V$_{PP}$ Optional Supply Voltage. The V_{PP} Optional Supply Voltage pin is used to select the Fast Program (see the Quadruple Byte Program Command description) and Fast Erase options of the memory and to protect the memory. When V_{PP} < V_{PPLK} Program and Erase operations cannot be performed and an error is reported in the Status Register if an attempt to change the memory contents is made. When V_{PP} = V_{CC} Program and Erase operations take place as normal. When V_{PP} = V_{PPH} Fast Program (if a Quadruple Byte Program Command is performed) and Fast Erase operations are used. Any other voltage input to V_{PP} will result in undefined behavior and should not be used.

V_{PP} should not be set to V_{PPH} for more than 80 hours during the life of the memory.

V$_{SS}$ Ground. V_{SS} is the reference for all the voltage measurements.

Table 3. Memory Identification Input Configuration

Memory Number	ID3	ID2	ID1	ID0	A21	A20	A19	A18
1 (Boot)	V_{IL} or floating	V_{IL} or floating	V_{IL} or floating	V_{IL} or floating	1	1	1	1
2	V_{IL} or floating	V_{IL} or floating	V_{IL} or floating	V_{IH}	1	1	1	0
3	V_{IL} or floating	V_{IL} or floating	V_{IH}	V_{IL} or floating	1	1	0	1
4	V_{IL} or floating	V_{IL} or floating	V_{IH}	V_{IH}	1	1	0	0
5	V_{IL} or floating	V_{IH}	V_{IL} or floating	V_{IL} or floating	1	0	1	1
6	V_{IL} or floating	V_{IH}	V_{IL} or floating	V_{IH}	1	0	1	0
7	V_{IL} or floating	V_{IH}	V_{IH}	V_{IL} or floating	1	0	0	1
8	V_{IL} or floating	V_{IH}	V_{IH}	V_{IH}	1	0	0	0
9	V_{IH}	V_{IL} or floating	V_{IL} or floating	V_{IL} or floating	0	1	1	1
10	V_{IH}	V_{IL} or floating	V_{IL} or floating	V_{IH}	0	1	1	0
11	V_{IH}	V_{IL} or floating	V_{IH}	V_{IL} or floating	0	1	0	1
12	V_{IH}	V_{IL} or floating	V_{IH}	V_{IH}	0	1	0	0
13	V_{IH}	V_{IH}	V_{IL} or floating	V_{IL} or floating	0	0	1	1
14	V_{IH}	V_{IH}	V_{IL} or floating	V_{IH}	0	0	1	0
15	V_{IH}	V_{IH}	V_{IH}	V_{IL} or floating	0	0	0	1
16	V_{IH}	V_{IH}	V_{IH}	V_{IH}	0	0	0	0

Table 4. Block Addresses

Size (Kbytes)	Address Range	Block Number	Block Type
16	3C000h-3FFFFh	6	Boot Block (Top)
8	3A000h-3BFFFh	5	Parameter Block
8	38000h-39FFFh	4	Parameter Block
32	30000h-37FFFh	3	Main Block
64	20000h-2FFFFh	2	Main Block
64	10000h-1FFFFh	1	Main Block
64	00000h-0FFFFh	0	Main Block

Note: For A18 and A19 values, refer to Table 3.

BUS OPERATIONS

The two interfaces have similar bus operations but the signals and timings are completely different. The Low Pin Count (LPC) Interface is the usual interface and all of the functionality of the part is available through this interface. Only a subset of functions are available through the Address/ Address Multiplexed (A/A Mux) Interface.

Follow the section Low Pin Count (LPC) Bus Operations below and the section Address/ Address Multiplexed (A/A Mux) Interface Bus Operations below for a description of the bus operations on each interface.

Low Pin Count (LPC) Bus Operations

The Low Pin Count (LPC) Interface consists of four data signals (LAD0-LAD3), one control line ($\overline{\text{LFRAME}}$) and a clock (CLK). In addition protection against accidental or malicious data corruption can be achieved using two further signals ($\overline{\text{TBL}}$ and $\overline{\text{WP}}$). Finally two reset signals ($\overline{\text{RP}}$ and $\overline{\text{INIT}}$) are available to put the memory into a known state.

The data signals, control signal and clock are designed to be compatible with PCI electrical specifications. The interface operates with clock speeds up to 33MHz.

The following operations can be performed using the appropriate bus cycles: Bus Read, Bus Write, Standby, Reset and Block Protection.

Bus Read. Bus Read operations read from the memory cells, specific registers in the Command Interface or Low Pin Count Registers. A valid Bus Read operation starts when Input Communication Frame, $\overline{\text{LFRAME}}$, is Low, V_{IL}, as Clock rises and the correct Start cycle is on LAD0-LAD3. On the following clock cycles the Host will send the Cycle Type + Dir, Address and other control bits on LAD0-LAD3. The memory responds by outputting Sync data until the wait-states have elapsed followed by Data0-Data3 and Data4-Data7.

Refer to Table 5, Bus Read Field Definitions (LPC Interface), and Figure 5, Bus Read Waveforms (LPC Interface), for a description of the Field definitions for each clock cycle of the transfer. See Table 22, AC Signal Timing Characteristics (LPC Interface), and Figure 10, AC Signal Timing Waveforms (LPC Interface), for details on the timings of the signals.

Bus Write. Bus Write operations write to the Command Interface or Low Pin Count Registers. A valid Bus Write operation starts when Input

Communication Frame, $\overline{\text{LFRAME}}$, is Low, V_{IL}, as Clock rises and the correct Start cycle is on LAD0-LAD3. On the following Clock cycles the Host will send the Cycle Type + Dir, Address, other control bits, Data0-Data3 and Data4-Data7 on LAD0-LAD3. The memory outputs Sync data until the wait-states have elapsed.

Refer to Table 6, Bus Write Field Definitions (LPC Interface), and Figure 6, Bus Write Waveforms (LPC Interface), for a description of the Field definitions for each clock cycle of the transfer. See Table 22, AC Signal Timing Characteristics (LPC Interface), and Figure 10, AC Signal Timing Waveforms (LPC Interface), for details on the timings of the signals.

Bus Abort. The Bus Abort operation can be used to immediately abort the current bus operation. A Bus Abort occurs when $\overline{\text{LFRAME}}$ is driven Low, V_{IL}, during the bus operation; the memory will tri-state the Input/Output Communication pins, LAD0-LAD3.

Note that, during a Bus Write operation, the Command Interface starts executing the command as soon as the data is fully received; a Bus Abort during the final TAR cycles is not guaranteed to abort the command; the bus, however, will be released immediately.

Standby. When $\overline{\text{LFRAME}}$ is High, V_{IH}, the memory is put into Standby mode where LAD0-LAD3 are put into a high-impedance state and the Supply Current is reduced to the Standby level, I_{CC1}.

Reset. During Reset mode all internal circuits are switched off, the memory is deselected and the outputs are put in high-impedance. The memory is in Reset mode when Interface Reset, $\overline{\text{RP}}$, or CPU Reset, $\overline{\text{INIT}}$, is Low, V_{IL}. $\overline{\text{RP}}$ or $\overline{\text{INIT}}$ must be held Low, V_{IL}, for t_{PLPH}. The memory resets to Read mode upon return from Reset mode and the Lock Registers return to their default states regardless of their state before Reset, see Table 13. If $\overline{\text{RP}}$ or $\overline{\text{INIT}}$ goes Low, V_{IL}, during a Program or Erase operation, the operation is aborted and the memory cells affected no longer contain valid data; the memory can take up to t_{PLRH} to abort a Program or Erase operation.

Block Protection. Block Protection can be forced using the signals Top Block Lock, $\overline{\text{TBL}}$, and Write Protect, $\overline{\text{WP}}$, regardless of the state of the Lock Registers.

Table 5. Bus Read Field Definitions (LPC Interface)

Clock Cycle Number	Clock Cycle Count	Field	LAD0-LAD3	Memory I/O	Description
1	1	START	0000b	I	On the rising edge of CLK with $\overline{\text{LFRAME}}$ Low, the contents of LAD0-LAD3 must be 0000b to indicate the start of a LPC cycle.
2	1	CYCTYPE + DIR	0100b	I	Indicates the type of cycle. Bits 3:2 must be 01b. Bit 1 indicates the direction of transfer: 0b for read. Bit 0 is '0'.
3-10	8	ADDR	XXXX	I	A 32-bit address phase is transferred starting with the most significant nibble first. A23-A31 must be set to 1. A22 = 1 for Array, A22 = 0 for registers access. For A18-A21 values, refer to Table 3.
11	1	TAR	1111b	I	The host drives LAD0-LAD3 to 1111b to indicate a turnaround cycle.
12	1	TAR	1111b (float)	O	The LPC Flash Memory takes control of LAD0-LAD3 during this cycle.
13-14	2	WSYNC	0101b	O	The LPC Flash Memory drives LAD0-LAD3 to 0101b (short wait-sync) for two clock cycles, indicating that the data is not yet available. Two wait-states are always included.
15	1	RSYNC	0000b	O	The LPC Flash Memory drives LAD0-LAD3 to 0000b, indicating that data will be available during the next clock cycle.
16-17	2	DATA	XXXX	O	Data transfer is two CLK cycles, starting with the least significant nibble.
18	1	TAR	1111b	O	The LPC Flash Memory drives LAD0-LAD3 to 1111b to indicate a turnaround cycle.
19	1	TAR	1111b (float)	N/A	The LPC Flash Memory floats its outputs, the host takes control of LAD0-LAD3.

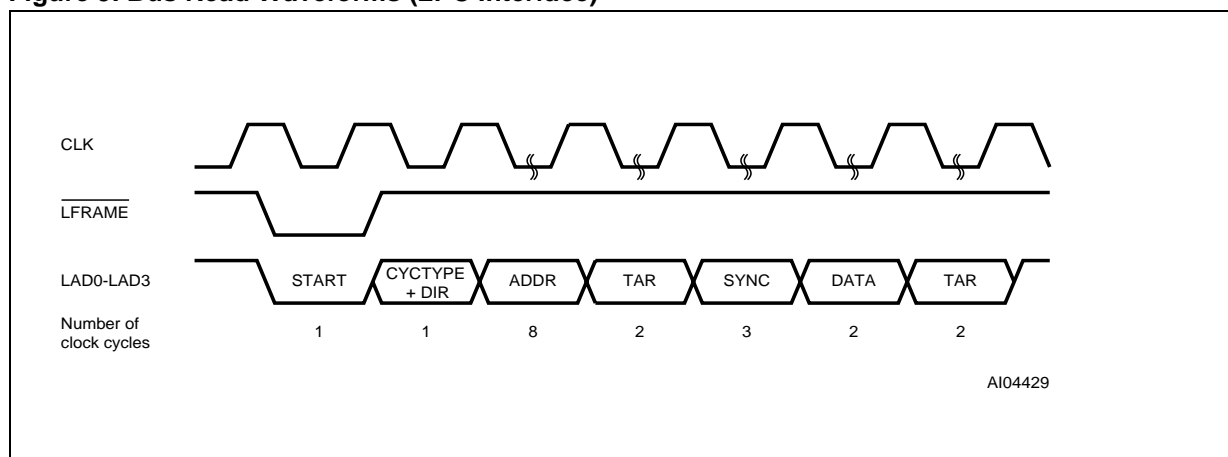**Figure 5. Bus Read Waveforms (LPC Interface)**

Table 6. Bus Write Field Definitions (LPC Interface)

Clock Cycle Number	Clock Cycle Count	Field	LAD0-LAD3	Memory I/O	Description
1	1	START	0000b	I	On the rising edge of CLK with $\overline{\text{LFRAME}}$ Low, the contents of LAD0-LAD3 must be 0000b to indicate the start of a LPC cycle.
2	1	CYCTYPE + DIR	011Xb	I	Indicates the type of cycle. Bits 3:2 must be 01b. Bit 1 indicates the direction of transfer: 1b for write. Bit 0 is don't care (X).
3-10	8	ADDR	XXXX	I	A 32-bit address phase is transferred starting with the most significant nibble first. A23-A31 must be set to 1. A22 = 1 for Array, A22 = 0 for registers access. For A18-A21 values, refer to Table 3.
11-12	2	DATA	XXXX	I	Data transfer is two cycles, starting with the least significant nibble.
13	1	TAR	1111b	I	The host drives LAD0-LAD3 to 1111b to indicate a turnaround cycle.
14	1	TAR	1111b (float)	O	The LPC Flash Memory takes control of LAD0-LAD3 during this cycle.
15	1	SYNC	0000b	O	The LPC Flash Memory drives LAD0-LAD3 to 0000b, indicating it has received data or a command.
16	1	TAR	1111b	O	The LPC Flash Memory drives LAD0-LAD3 to 1111b, indicating a turnaround cycle.
17	1	TAR	1111b (float)	N/A	The LPC Flash Memory floats its outputs and the host takes control of LAD0-LAD3.

Figure 6. Bus Write Waveforms (LPC Interface)
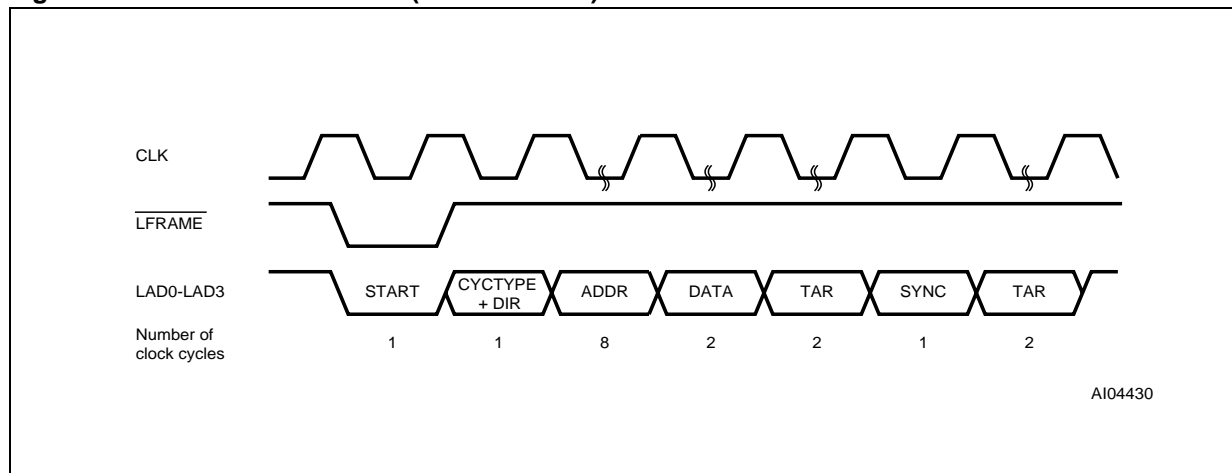
Address/Address Multiplexed (A/A Mux) Bus Operations

The Address/Address Multiplexed (A/A Mux) Interface has a more traditional style interface. The signals consist of a multiplexed address signals (A0-A10), data signals, (DQ0-DQ7) and three control signals (R$\overline{C}$, $\overline{G}$, $\overline{W}$). An additional signal, $\overline{RP}$, can be used to reset the memory.

The Address/Address Multiplexed (A/A Mux) Interface is included for use by Flash Programming equipment for faster factory programming. Only a subset of the features available to the Low Pin Count (LPC) Interface are available; these include all the Commands but exclude the Security features and other registers.

The following operations can be performed using the appropriate bus cycles: Bus Read, Bus Write, Output Disable and Reset.

When the Address/Address Multiplexed (A/A Mux) Interface is selected all the blocks are unprotected. It is not possible to protect any blocks through this interface.

Bus Read. Bus Read operations are used to output the contents of the Memory Array, the Electronic Signature and the Status Register. A valid Bus Read operation begins by latching the Row Address and Column Address signals into the memory using the Address Inputs, A0-A10, and the Row/Column Address Select R$\overline{C}$. Then Write Enable ($\overline{W}$) and Interface Reset ($\overline{RP}$) must be High, V_{IH}, and Output Enable, $\overline{G}$, Low, V_{IL}, in order to perform a Bus Read operation. The Data Inputs/Outputs will output the value, see Figure 12, Read AC Waveforms (A/A Mux Interface), and Table 25, Read AC Characteristics (A/A Mux Interface), for details of when the output becomes valid.

Bus Write. Bus Write operations write to the Command Interface. A valid Bus Write operation begins by latching the Row Address and Column Address signals into the memory using the Address Inputs, A0-A10, and the Row/Column Address Select R$\overline{C}$. The data should be set up on the Data Inputs/Outputs; Output Enable, $\overline{G}$, and Interface Reset, $\overline{RP}$, must be High, V_{IH} and Write Enable, $\overline{W}$, must be Low, V_{IL}. The Data Inputs/Outputs are latched on the rising edge of Write Enable, $\overline{W}$. See Figure 13, Write AC Waveforms (A/A Mux Interface), and Table 26, Write AC Characteristics (A/A Mux Interface), for details of the timing requirements.

Output Disable. The data outputs are high-impedance when the Output Enable, $\overline{G}$, is at V_{IH}.

Reset. During Reset mode all internal circuits are switched off, the memory is deselected and the outputs are put in high-impedance. The memory is in Reset mode when $\overline{RP}$ is Low, V_{IL}. $\overline{RP}$ must be held Low, V_{IL} for t_{PLPH}. If $\overline{RP}$ is goes Low, V_{IL}, during a Program or Erase operation, the operation is aborted and the memory cells affected no longer contain valid data; the memory can take up to t_{PLRH} to abort a Program or Erase operation.

Table 7. A/A Mux Bus Operations

Operation	$\overline{G}$	$\overline{W}$	$\overline{RP}$	V_{PP}	DQ7-DQ0
Bus Read	V_{IL}	V_{IH}	V_{IH}	Don't Care	Data Output
Bus Write	V_{IH}	V_{IL}	V_{IH}	V_{CC} or V_{PPH}	Data Input
Output Disable	V_{IH}	V_{IH}	V_{IH}	Don't Care	Hi-Z
Reset	V_{IL} or V_{IH}	V_{IL} or V_{IH}	V_{IL}	Don't Care	Hi-Z

Table 8. Manufacturer and Device Codes

Operation	$\overline{G}$	$\overline{W}$	$\overline{RP}$	A17-A1	A0	DQ7-DQ0
Manufacturer Code	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	20h
Device Code	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	31h

Table 9. Commands

Command	Cycles	Bus Write Operations									
		1st		2nd		3rd		4th		5th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read Memory Array	1	X	FFh								
Read Status Register	1	X	70h								
Read Electronic Signature	1	X	90h								
	1	X	98h								
Program	2	X	40h	PA	PD						
	2	X	10h	PA	PD						
Quadruple Byte Program	5	X	30h	A_1	PD	A_2	PD	A_3	PD	A_4	PD
Chip Erase	2	X	80h	X	10h						
Block Erase	2	X	20h	BA	D0h						
Clear Status Register	1	X	50h								
Program/Erase Suspend	1	X	B0h								
Program/Erase Resume	1	X	D0h								
Invalid/Reserved	1	X	00h								
	1	X	01h								
	1	X	60h								
	1	X	2Fh								
	1	X	C0h								

Note: X Don't Care, PA Program Address, PD Program Data, $A_{1,2,3,4}$ Consecutive Addresses, BA Any address in the block.

Read Memory Array: After a Read Memory Array command, read the memory as normal until another command is issued.
Read Status Register: After a Read Status Register command, read the Status Register as normal until another command is issued.
Read Electronic Signature: After a Read Electronic Signature command, read Manufacturer Code, Device Code until another command is issued.
Block Erase, Byte Program: After these commands, read the Status Register until the command completes and another command is issued.
Quadruple Byte Program: This command is only valid in A/A Mux mode. Addresses A_1, A_2, A_3 and A_4 must be consecutive addresses differing only for address bit A0 and A1. After this command read the Status Register until the command completes and another command is issued.
Chip Erase: This command is only valid in A/A Mux mode. After this command, read the Status Register until the command completes and another command is issued.
Clear Status Register: After the Clear Status Register command bits 1, 3, 4 and 5 in the Status Register are reset to '0'.
Program/Erase Suspend: After the Program/Erase Suspend command has been accepted, issue Read Memory Array, Read Status Register, Program (during Erase suspend) and Program/Erase resume commands.
Program/Erase Resume: After the Program/Erase Resume command the suspended Program/Erase operation resumes, read the Status Register until the Program/Erase Controller completes and the memory returns to Read Mode.
Invalid/Reserved: Do not use Invalid or Reserved commands.

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations.

After power-up or a Reset operation the memory enters Read mode.

The commands are summarized in Table 9, Commands. Refer to Table 9 in conjunction with the text descriptions below.

Read Memory Array Command. The Read Memory Array command returns the memory to its Read mode where it behaves like a ROM or EPROM. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Once the command is issued the memory remains in Read mode until another command is issued. From Read mode Bus Read operations will access the memory array.

While the Program/Erase Controller is executing a Program or Erase operation the memory will not accept the Read Memory Array command until the operation completes.

Read Status Register Command. The Read Status Register command is used to read the Status Register. One Bus Write cycle is required to issue the Read Status Register command. Once the command is issued subsequent Bus Read operations read the Status Register until another command is issued. See the section on the Status Register for details on the definitions of the Status Register bits.

Read Electronic Signature Command. The Read Electronic Signature command is used to read the Manufacturer Code and the Device Code. One Bus Write cycle is required to issue the Read Electronic Signature command. Once the command is issued subsequent Bus Read operations read the Manufacturer Code or the Device Code until another command is issued.

After the Read Electronic Signature Command is issued the Manufacturer Code and Device Code can be read using Bus Read operations using the addresses in Table 10.

Table 10. Read Electronic Signature

Code	Address	Data
Manufacturer Code	00000h	20h
Device Code	00001h	31h

Note: For A18 and A19 values, refer to Table 3.

Program Command. The Program command can be used to program a value to one address in the memory array at a time. Two Bus Write operations are required to issue the command; the second Bus Write cycle latches the address and data in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

If the address falls in a protected block then the Program operation will abort, the data in the memory array will not be changed and the Status Register will output the error.

During the Program operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Program times are given in Table 23.

Note that the Program command cannot change a bit set at '0' back to '1' and attempting to do so will not cause any modification on its value. One of the Erase commands must be used to set all of the bits in the block to '1'.

See Figure 14, Program Flowchart and Pseudo Code, for a suggested flowchart on using the Program command.

Quadruple Byte Program Command. The Quadruple Byte Program Command can be only used in A/A Mux mode to program four adjacent bytes in the memory array at a time. The four bytes must differ only for the addresses A0 and A1. Programming should not be attempted when V_{PP} is not at V_{PPH}. The operation can also be executed if V_{PP} is below V_{PPH}, but result could be uncertain. Five Bus Write operations are required to issue the command. The second, the third and the fourth Bus Write cycle latches respectively the address and data of the first, the second and the third byte in the internal state machine. The fifth Bus Write cycle latches the address and data of the fourth byte in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Quadruple Byte Program operation the memory will only accept the Read Status register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Quadruple Byte Program times are given in Table 23.

Note that the Quadruple Byte Program command cannot change a bit set to '0' back to '1' and attempting to do so will not cause any modification on its value. An Erase command must be used to set all of the bits in the block to '1'.

See Figure 15, Quadruple Byte Program Flowchart and Pseudo Code (A/A Mux Interface Only), for a suggested flowchart on using the Quadruple Byte Program command.

Chip Erase Command. The Chip Erase command can be used in A/A Mux mode to erase the entire chip at a time. Erasing should not be attempted when V_{PP} is not at V_{PPH}. The operation can also be executed if V_{PP} is below V_{PPH}, but result could be uncertain. Two Bus Write operations are required to issue the command and start the Program/Erase Controller. Once the command is issued, subsequent Bus Read operations read the Status Register. (See the section on the Status Register for details of the definitions of the Status Register bits.)

During the Chip Erase operation, the memory only accepts the Read Status Register command. All other commands are ignored.

Typical Chip Erase times are given in Table 23.

The Chip Erase command sets all of the bits in the memory to '1'. See Figure 17, Chip Erase Flowchart and Pseudo Code, for a suggested flowchart when using the Chip Erase command.

Block Erase Command. The Block Erase command can be used to erase a block. Two Bus Write operations are required to issue the command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

During the Erase operation the memory only accepts the Read Status Register command and the Program/Erase Suspend command. All other commands are ignored. Typical Erase times are given in Table 23.

The Erase command sets all of the bits in the block to '1'. All previous data in the block is lost.

See Figure 18, Block Erase Flowchart and Pseudo Code, for a suggested flowchart on using the Erase command.

Clear Status Register Command. The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register to '0'. One Bus Write is required to issue the Clear Status Register command. Once the command is issued the memory returns to its previous mode, subsequent Bus Read operations continue to output the same data.

The bits in the Status Register are sticky and do not automatically return to '0' when a new Program or Erase command is issued. If an error occurs then it is essential to clear any error bits in the Status Register by issuing the Clear Status Register command before attempting a new Program or Erase command.

Program/Erase Suspend Command. The Program/Erase Suspend command can be used to pause a Program or Erase operation. One Bus Write cycle is required to issue the Program/Erase Suspend command and pause the Program/Erase Controller. Once the command is issued it is necessary to poll the Program/Erase Controller Status bit to find out when the Program/Erase Controller has paused; no other commands will be accepted until the Program/Erase Controller has paused. After the Program/Erase Controller has paused, the memory will continue to output the Status Register until another command is issued.

During the polling period between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing it is possible for the operation to complete. Once Program/Erase Controller Status bit indicates that the Program/Erase Controller is no longer active, the Program Suspend Status bit or the Erase Suspend Status bit can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing see Table 23.

During Program/Erase Suspend the Read Memory Array, Read Status Register, Read Electronic Signature and Program/Erase Resume commands will be accepted by the Command Interface. Additionally, if the suspended operation was Erase then the Program command will also be accepted; only the blocks not being erased may be read or programmed correctly.

See Figure 16, Program Suspend and Resume Flowchart, and Pseudo Code, and Figure 19, Erase Suspend and Resume Flowchart, and Pseudo Code, for suggested flowcharts on using the Program/Erase Suspend command.

Program/Erase Resume Command. The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend has paused it. One Bus Write cycle is required to issue the Program/Erase Resume command. Once the command is issued subsequent Bus Read operations read the Status Register.

STATUS REGISTER

The Status Register provides information on the current or previous Program or Erase operation. Different bits in the Status Register convey different information and errors on the operation.

To read the Status Register the Read Status Register command can be issued. The Status Register is automatically read after Program, Erase and Program/Erase Resume commands are issued. The Status Register can be read from any address.

The Status Register bits are summarized in Table 11, Status Register Bits. Refer to Table 11 in conjunction with the text descriptions below.

Program/Erase Controller Status (Bit 7). The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is '0', the Program/Erase Controller is active; when the bit is '1', the Program/Erase Controller is inactive.

The Program/Erase Controller Status is '0' immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is '1'.

During Program and Erase operation the Program/Erase Controller Status bit can be polled to find the end of the operation. The other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is '1'.

After the Program/Erase Controller completes its operation the Erase Status, Program Status, V_{PP} Status and Block Protection Status bits should be tested for errors.

Erase Suspend Status (Bit 6). The Erase Suspend Status bit indicates that an Erase operation has been suspended and is waiting to be resumed. The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is '1' (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Erase Suspend Status bit is '0' the Program/Erase Controller is active or has completed its operation; when the bit is '1' a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns to '0'.

Erase Status (Bit 5). The Erase Status bit can be used to identify if the memory has applied the maximum number of erase pulses to the block and still failed to verify that the block has erased correctly. The Erase Status bit should be read once the Program/Erase Controller Status bit is '1' (Program/Erase Controller inactive).

When the Erase Status bit is '0' the memory has successfully verified that the block has erased correctly; when the Erase Status bit is '1' the Program/Erase Controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly.

Once the Erase Status bit is set to '1' it can only be reset to '0' by a Clear Status Register command or a hardware reset. If it is set to '1' it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Status (Bit 4). The Program Status bit can be used to identify if the memory has applied the maximum number of program pulses to the byte and still failed to verify that the byte has programmed correctly. The Program Status bit should be read once the Program/Erase Controller Status bit is '1' (Program/Erase Controller inactive).

When the Program Status bit is '0' the memory has successfully verified that the byte has programmed correctly; when the Program Status bit is '1' the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that the byte has programmed correctly.

Once the Program Status bit is set to '1' it can only be reset to '0' by a Clear Status Register command or a hardware reset. If it is set to '1' it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

V_{PP} Status (Bit 3). The V_{PP} Status bit can be used to identify an invalid voltage on the V_{PP} pin during Program and Erase operations. The V_{PP} pin is only sampled at the beginning of a Program or Erase operation. Indeterminate results can occur if V_{PP} becomes invalid during a Program or Erase operation.

When the V_{PP} Status bit is '0' the voltage on the V_{PP} pin was sampled at a valid voltage; when the V_{PP} Status bit is '1' the V_{PP} pin has a voltage that is below the V_{PP} Lockout Voltage, V_{PPLK}, the memory is protected; Program and Erase operation cannot be performed.

Once the V_{PP} Status bit set to '1' it can only be reset to '0' by a Clear Status Register command or a hardware reset. If it is set to '1' it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Suspend Status (Bit 2). The Program Suspend Status bit indicates that a Program operation has been suspended and is waiting to be resumed. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is '1' (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Program Suspend Status bit is '0' the Program/Erase Controller is active or has completed its operation; when the bit is '1' a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns to '0'.

Block Protection Status (Bit 1). The Block Protection Status bit can be used to identify if the Program or Erase operation has tried to modify the contents of a protected block. When the Block Protection Status bit is to '0' no Program or Erase operations have been attempted to protected blocks since the last Clear Status Register command or hardware reset; when the Block Protection Status bit is '1' a Program or Erase operation has been attempted on a protected block.

Once it is set to '1' the Block Protection Status bit can only be reset to '0' by a Clear Status Register command or a hardware reset. If it is set to '1' it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Using the A/A Mux Interface the Block Protection Status bit is always '0'.

Reserved (Bit 0). Bit 0 of the Status Register is reserved. Its value should be masked.

Table 11. Status Register Bits

Operation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
Program active	'0'	X [1]	'0'	'0'	'0'	'0'	'0'
Program suspended	'1'	X [1]	'0'	'0'	'0'	'1'	'0'
Program completed successfully	'1'	X [1]	'0'	'0'	'0'	'0'	'0'
Program failure due to V_{PP} Error	'1'	X [1]	'0'	'0'	'1'	'0'	'0'
Program failure due to Block Protection (LPC Interface only)	'1'	X [1]	'0'	'0'	'0'	'0'	'1'
Program failure due to cell failure	'1'	X [1]	'0'	'1'	'0'	'0'	'0'
Erase active	'0'	'0'	'0'	'0'	'0'	'0'	'0'
Block Erase suspended	'1'	'1'	'0'	'0'	'0'	'0'	'0'
Erase completed successfully	'1'	'0'	'0'	'0'	'0'	'0'	'0'
Block Erase failure due to V_{PP} Error	'1'	'0'	'0'	'0'	'1'	'0'	'0'
Block Erase failure due to Block Protection (LPC Interface only)	'1'	'0'	'0'	'0'	'0'	'0'	'1'
Erase failure due to failed cell(s)	'1'	'0'	'1'	'0'	'0'	'0'	'0'

Note: 1. For Program operations during Erase Suspend Bit 6 is '1', otherwise Bit 6 is '0'.

LOW PIN COUNT (LPC) INTERFACE CONFIGURATION REGISTERS

When the Low Pin Count Interface is selected several additional registers can be accessed. These registers control the protection status of the blocks and read the General Purpose Input pins. See Table 12 for an example of the Register Configuration map, valid for the boot memory, i.e. ID0-ID3 floating or driven L_{OW}, V_{IL} and A18-A21 set to '1'.

Lock Registers

The Lock Registers control the protection status of the blocks. Each block has its own Lock Register. Three bits within each Lock Register control the protection of each block, the Write Lock Bit, the Read Lock Bit and the Lock Down Bit.

The Lock Registers can be read and written, though care should be taken when writing as, once the Lock Down Bit is set, '1', further modifications to the Lock Register cannot be made until cleared, to '0', by a reset or power-up.

See Table 13 for details on the bit definitions of the Lock Registers.

Write Lock. The Write Lock Bit determines whether the contents of the block can be modified (using the Program or Erase Command). When the Write Lock Bit is set, '1', the block is write protected; any operations that attempt to change the data in the block will fail and the Status Register will report the error. When the Write Lock Bit is reset, '0', the block is not write protected through the Lock Register and may be modified unless write protected through some other means.

When V_{PP} is less than V_{PPLK} all blocks are protected and cannot be modified, regardless of the state of the Write Lock Bit. If Top Block Lock, $\overline{TBL}$, is Low, V_{IL}, then the Top Block (Block 6) is write protected and cannot be modified. Similarly, if Write Protect, $\overline{WP}$, is Low, V_{IL}, then the blocks 0 to 5 are write protected and cannot be modified.

After power-up or reset the Write Lock Bit is always set to '1' (write protected).

Read Lock. The Read Lock bit determines whether the contents of the block can be read (from Read mode). When the Read Lock Bit is set, '1', the block is read protected; any operation that attempts to read the contents of the block will read 00h instead. When the Read Lock Bit is reset, '0', read operations in the block return the data programmed into the block as expected.

After power-up or reset the Read Lock Bit is always reset to '0' (not read protected).

Lock Down. The Lock Down Bit provides a mechanism for protecting software data from simple hacking and malicious attack. When the Lock Down Bit is set, '1', further modification to the Write Lock, Read Lock and Lock Down Bits cannot be performed. A reset or power-up is required before changes to these bits can be made. When the Lock Down Bit is reset, '0', the Write Lock, Read Lock and Lock Down Bits can be changed.

General Purpose Input Register

The General Purpose Input Register holds the state of the General Purpose Input pins, GPI0-GPI4. When this register is read, the state of these pins is returned. This register is read-only and writing to it has no effect.

The signals on the General Purpose Input pins should remain constant throughout the whole Bus Read cycle in order to guarantee that the correct data is read.

Table 12. Low Pin Count Register Configuration Map [1]

Mnemonic	Register Name	Memory Address	Default Value	Access
T_BLOCK_LK	Top Block Lock Register (Block 6)	FFBFC002h	01h	R/W
T_MINUS01_LK	Top Block [-1] Lock Register (Block 5)	FFBFA002h	01h	R/W
T_MINUS02_LK	Top Block [-2] Lock Register (Block 4)	FFBF8002h	01h	R/W
T_MINUS03_LK	Top Block [-3] Lock Register (Block 3)	FFBF0002h	01h	R/W
T_MINUS04_LK	Top Block [-4] Lock Register (Block 2)	FFBE0002h	01h	R/W
T_MINUS05_LK	Top Block [-5] Lock Register (Block 1)	FFBD0002h	01h	R/W
T_MINUS06_LK	Top Block [-6] Lock Register (Block 0)	FFBC0002h	01h	R/W
GPI_REG	General Purpose Input Register	FFBC0100h	N/A	R

Note: 1. This map is referred to the boot memory (ID0-ID3 floating or driven, L_{OW}, V_{IL} and A18-A21 set to '1').

Table 13. Lock Register Bit Definitions[1]

Bit	Bit Name	Value	Function
7-3			Reserved
2	Read-Lock	'1'	Bus Read operations in this Block always return 00h.
		'0'	Bus read operations in this Block return the Memory Array contents. (Default value).
1	Lock-Down	'1'	Changes to the Read-Lock bit and the Write-Lock bit cannot be performed. Once a '1' is written to the Lock-Down bit it cannot be cleared to '0'; the bit is always reset to '0' following a Reset (using $\overline{RP}$ or $\overline{INIT}$) or after power-up.
		'0'	Read-Lock and Write-Lock can be changed by writing new values to them. (Default value).
0	Write-Lock	'1'	Program and Erase operations in this Block will set an error in the Status Register. The memory contents will not be changed. (Default value).
		'0'	Program and Erase operations in this Block are executed and will modify the Block contents.

Note: 1. Applies to Top Block Lock Register (T_BLOCK_LK) and Top Block [-1] Lock Register (T_MINUS01_LK) to Top Block [-6] Lock Register (T_MINUS06_LK).

Table 14. General Purpose Input Register Definition[1]

Bit	Bit Name	Value	Function
7-5			Reserved
4	GPI4	'1'	Input Pin GPI4 is at V_{IH}
		'0'	Input Pin GPI4 is at V_{IL}
3	GPI3	'1'	Input Pin GPI3 is at V_{IH}
		'0'	Input Pin GPI3 is at V_{IL}
2	GPI2	'1'	Input Pin GPI2 is at V_{IH}
		'0'	Input Pin GPI2 is at V_{IL}
1	GPI1	'1'	Input Pin GPI1 is at V_{IH}
		'0'	Input Pin GPI1 is at V_{IL}
0	GPI0	'1'	Input Pin GPI0 is at V_{IH}
		'0'	Input Pin GPI0 is at V_{IL}

Note: 1. Applies to the General Purpose Input Register (GPI_REG).

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 15. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{BIAS}	Temperature Under Bias	−50	125	°C
T_{STG}	Storage Temperature	−65	150	°C
V_{IO}	Input or Output Voltage [1,2]	−0.6	V_{CC} +0.6	V
V_{CC}	Supply Voltage	−0.6	4	V
V_{PP}	Program Voltage	−0.6	13	V

Note: 1. Minimum voltage may undershoot to −2V during transition and for less than 20ns during transitions.
    2. Maximum voltage may overshoot to V_{CC} +2V during transition and for less than 20ns during transitions.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 16. Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.6	V
T_A	Ambient Operating Temperature (range 1)	0	70	°C
	Ambient Operating Temperature (range 5)	−20	85	°C

Figure 7. AC Measurement I/O Waveform (LPC Interface)
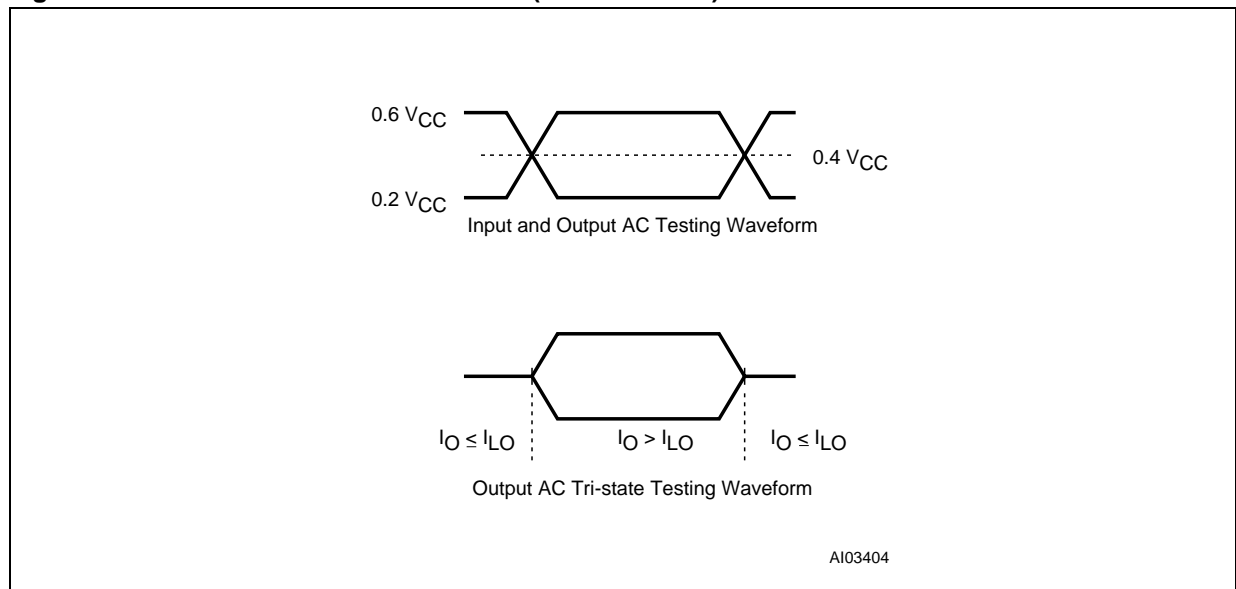
Table 17. AC Measurement Conditions (LPC Interface)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	10		pF
	Input Rise and Fall Times		1.4	ns
	Input Pulse Voltages	$0.2V_{CC}$ to $0.6V_{CC}$		V
	Input and Output Timing Reference Voltages	$0.4V_{CC}$		V

Figure 8. AC Measurement I/O Waveform (A/A Mux Interface)
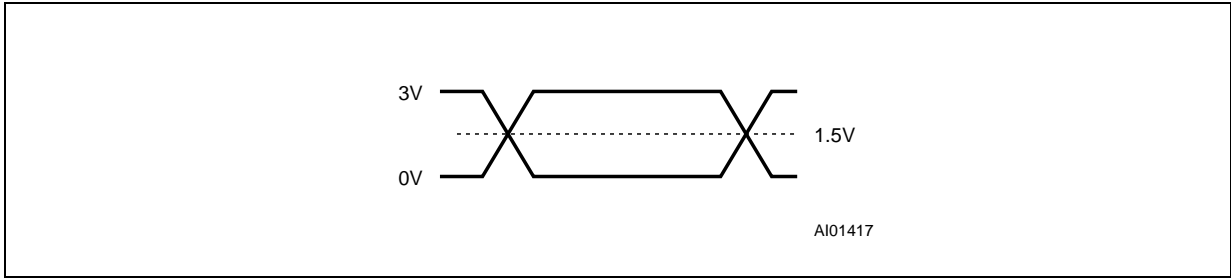
Table 18. AC Measurement Conditions (A/A Mux Interface)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		10	ns
	Input Pulse Voltages	0 to 3		V
	Input and Output Timing Reference Voltages	1.5		V

Table 19. Device Impedance

Symbol	Parameter [1]	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance [2]	$V_{IN} = 0V$		13	pF
C_{CLK}	Clock Capacitance [2]	$V_{IN} = 0V$	3	12	pF
L_{PIN}	Recommended Pin Inductance [3]			20	nH

Note: 1. T_A=25°C, f=1 MHz
2. Sampled only, not 100% tested
3. See PCI Specification

Table 20. DC Characteristics

Symbol	Parameter	Interface	Test Condition	Min	Max	Unit
V_{IH}	Input High Voltage	LPC		$0.5\ V_{CC}$	$V_{CC} + 0.5$	V
		A/A Mux		$0.7\ V_{CC}$	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	LPC		−0.5	$0.3\ V_{CC}$	V
		A/A Mux		-0.5	0.8	V
$V_{IH}(\overline{INIT})$	$\overline{INIT}$ Input High Voltage	LPC		1.35	$V_{CC} + 0.5$	V
$V_{IL}(\overline{INIT})$	$\overline{INIT}$ Input Low Voltage	LPC		−0.5	$0.2\ V_{CC}$	V
I_{LI}[2]	Input Leakage Current		$0V \leq V_{IN} \leq V_{CC}$		±10	µA
I_{LI2}	IC, IDx Input Leakage Current		IC, ID0, ID1, ID2, ID3 = V_{CC}		200	µA
R_{IL}	IC, IDx Input Pull Low Resistor			20	100	kΩ
V_{OH}	Output High Voltage	LPC	$I_{OH} = -500µA$	$0.9\ V_{CC}$		V
		A/A Mux	$I_{OH} = -100µA$	$V_{CC} - 0.4$		V
V_{OL}	Output Low Voltage	LPC	$I_{OL} = 1.5mA$		$0.1\ V_{CC}$	V
		A/A Mux	$I_{OL} = 1.8mA$		0.45	V
I_{LO}	Output Leakage Current		$0V \leq V_{OUT} \leq V_{CC}$		±10	µA
V_{PP1}	V_{PP} Voltage			3	3.6	V
V_{PPH}	V_{PP} Voltage (Fast Program/Fast Erase)			11.4	12.6	V
V_{PPLK}[1]	V_{PP} Lockout Voltage			1.5		V
V_{LKO}[1]	V_{CC} Lockout Voltage			1.8	2.3	V
I_{CC1}	Supply Current (Standby)	LPC	$\overline{LFRAME}$ = 0.9 V_{CC}, V_{PP} = V_{CC} All other inputs 0.9 V_{CC} to 0.1 V_{CC} V_{CC} = 3.6V, f(CLK) = 33MHz		100	µA
I_{CC2}	Supply Current (Standby)	LPC	$\overline{LFRAME}$ = 0.1 V_{CC}, V_{PP} = V_{CC} All other inputs 0.9 V_{CC} to 0.1 V_{CC} V_{CC} = 3.6V, f(CLK) = 33MHz		10	mA
I_{CC3}	Supply Current (Any internal operation active)	LPC	V_{CC} = V_{CC} max, V_{PP} = V_{CC} f(CLK) = 33MHz I_{OUT} = 0mA		60	mA
I_{CC4}	Supply Current (Read)	A/A Mux	$\overline{G}$ = V_{IH}, f = 6MHz		20	mA
I_{CC5}[1]	Supply Current (Program/Erase)	A/A Mux	Program/Erase Controller Active		20	mA
I_{PP}	V_{PP} Supply Current (Read/Standby)		$V_{PP} \geq V_{CC}$		400	µA
I_{PP1}[1]	V_{PP} Supply Current (Program/Erase active)		V_{PP} = V_{CC}		40	mA
			V_{PP} = 12V ± 5%		15	mA

Note: 1. Sampled only, not 100% tested.
2. Input leakage currents include High-Z output leakage for all bi-directional buffers with tri-state outputs.

Table 21. Clock Characteristics (LPC Interface)

Symbol	Parameter	Test Condition		Value	Unit
t_{CYC}	CLK Cycle Time[1]		Min	30	ns
t_{HIGH}	CLK High Time		Min	11	ns
t_{LOW}	CLK Low Time		Min	11	ns
	CLK Slew Rate	peak to peak	Min	1	V/ns
			Max	4	V/ns

Note: 1. Devices on the PCI Bus must work with any clock frequency between DC and 33MHz. Below 16MHz devices may be guaranteed by design rather than tested. Refer to PCI Specification.

Figure 9. Clock Waveform (LPC Interface)
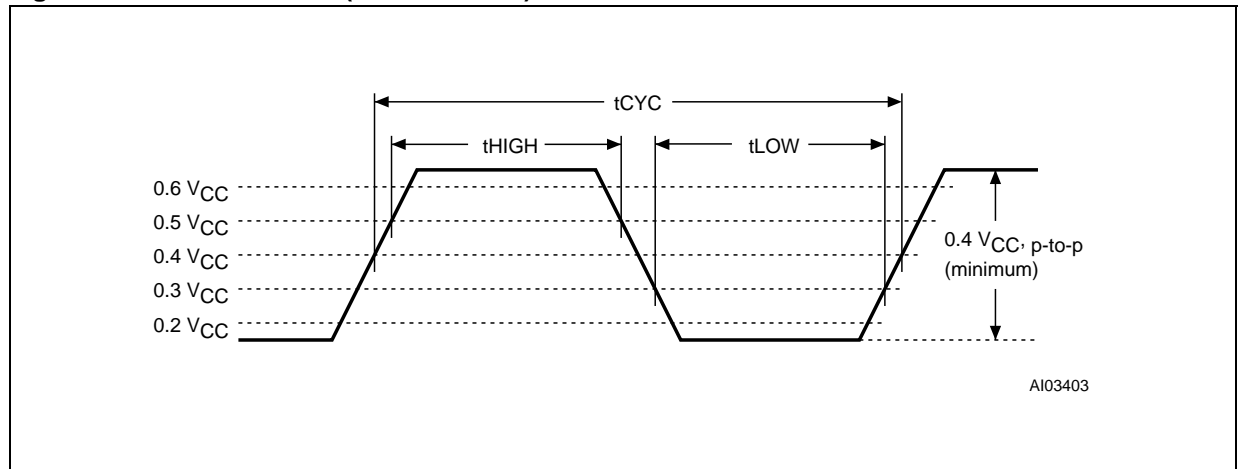
Table 22. AC Signal Timing Characteristics (LPC Interface)

Symbol	PCI Symbol	Parameter	Test Condition		Value	Unit
t_{CHQV}	t_{val}	CLK to Data Out		Min	2	ns
				Max	11	ns
t_{CHQX}[1]	t_{on}	CLK to Active (Float to Active Delay)		Min	2	ns
t_{CHQZ}	t_{off}	CLK to Inactive (Active to Float Delay)		Max	28	ns
t_{AVCH} t_{DVCH}	t_{su}	Input Set-up Time[2]		Min	7	ns
t_{CHAX} t_{CHDX}	t_h	Input Hold Time[2]		Min	0	ns

Note: 1. The timing measurements for Active/Float transitions are defined when the current through the pin equals the leakage current specification.
2. Applies to all inputs except CLK.

Figure 10. AC Signal Timing Waveforms (LPC Interface)
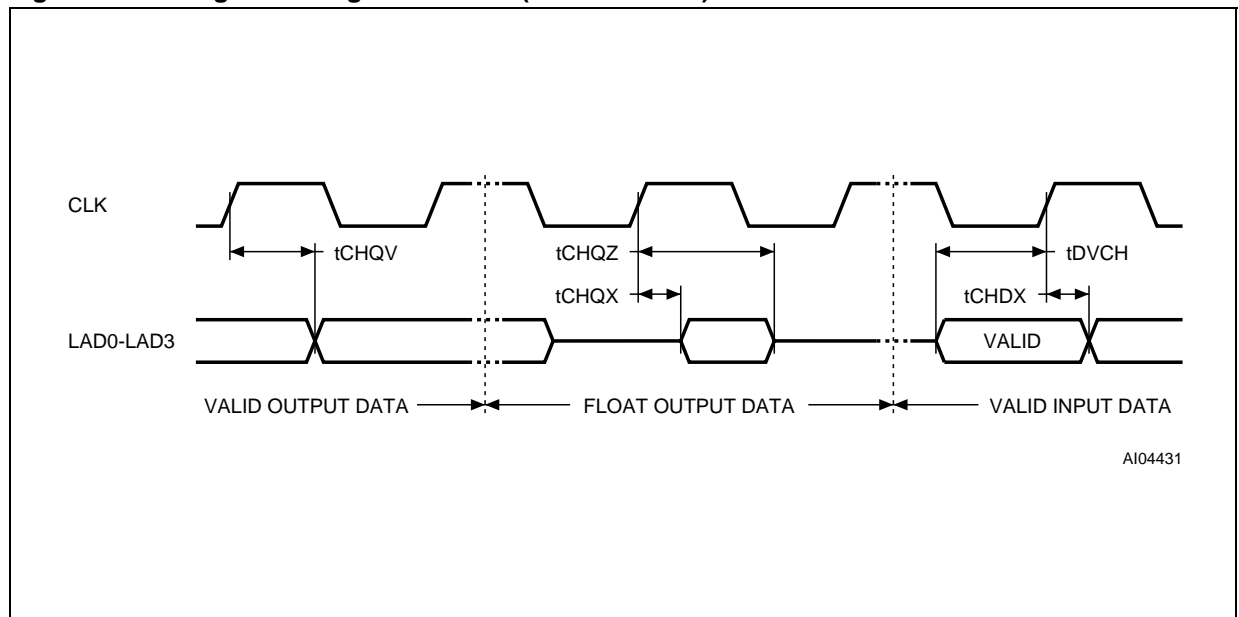
Table 23. Program and Erase Times

Parameter	Interface	Test Condition	Min	Typ [1]	Max	Unit
Byte Program				10	200	µs
Quadruple Byte Program	A/A Mux	V_{PP} = 12V ± 5%		10	200	µs
Chip Erase	A/A Mux	V_{PP} = 12V ± 5%		3		sec
Block Program (64 KBytes)	A/A Mux	V_{PP} = 12V ± 5%		0.1 [2]	5	sec
		V_{PP} = V_{CC}		0.4	5	sec
Block Erase (64 KBytes)		V_{PP} = 12V ± 5%		0.75	8	sec
		V_{PP} = V_{CC}		1	10	sec
Program/Erase Suspend to Program pause [3]					5	µs
Program/Erase Suspend to Block Erase pause [3]					30	µs

Note: 1. T_A = 25°C, V_{CC} = 3.3V
2. This time is obtained executing the Quadruple Byte Program Command.
3. Sampled only, not 100% tested.

Table 24. Reset AC Characteristics

Symbol	Parameter	Test Condition		Value	Unit
t_{PLPH}	$\overline{RP}$ or $\overline{INIT}$ Reset Pulse Width		Min	100	ns
t_{PLRH}	$\overline{RP}$ or $\overline{INIT}$ Low to Reset	Program/Erase Inactive	Max	100	ns
		Program/Erase Active	Max	30	µs
	$\overline{RP}$ or $\overline{INIT}$ Slew Rate[1]	Rising edge only	Min	50	mV/ns
t_{PHFL}	$\overline{RP}$ or $\overline{INIT}$ High to $\overline{LFRAME}$ Low	LPC Interface only	Min	30	µs
t_{PHWL} t_{PHGL}	$\overline{RP}$ High to Write Enable or Output Enable Low	A/A Mux Interface only	Min	50	µs

Note: 1. See Chapter 4 of the PCI Specification.

Figure 11. Reset AC Waveforms
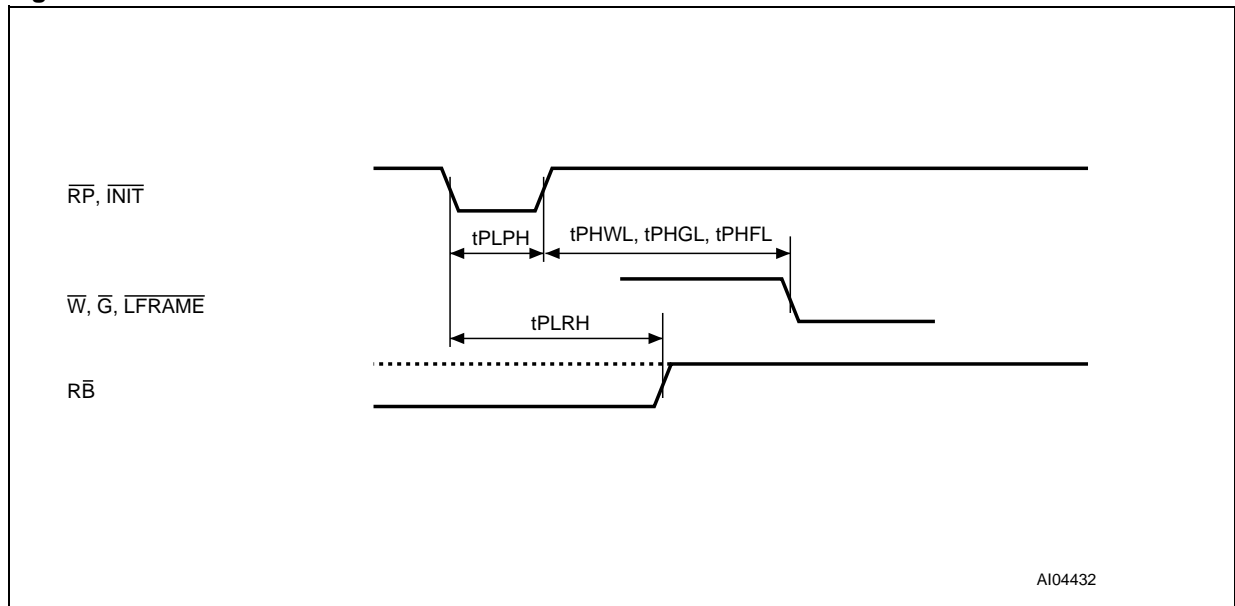
AI04432

Table 25. Read AC Characteristics (A/A Mux Interface)

Symbol	Parameter	Test Condition		Value	Unit
t$_{AVAV}$	Read Cycle Time		Min	250	ns
t$_{AVCL}$	Row Address Valid to R$\overline{C}$ Low		Min	50	ns
t$_{CLAX}$	R$\overline{C}$ Low to Row Address Transition		Min	50	ns
t$_{AVCH}$	Column Address Valid to R$\overline{C}$ high		Min	50	ns
t$_{CHAX}$	R$\overline{C}$ High to Column Address Transition		Min	50	ns
t$_{CHQV}$[1]	R$\overline{C}$ High to Output Valid		Max	150	ns
t$_{GLQV}$[1]	Output Enable Low to Output Valid		Max	50	ns
t$_{PHAV}$	$\overline{RP}$ High to Row Address Valid		Min	1	µs
t$_{GLQX}$	Output Enable Low to Output Transition		Min	0	ns
t$_{GHQZ}$	Output Enable High to Output Hi-Z		Max	50	ns
t$_{GHQX}$	Output Hold from Output Enable High		Min	0	ns

Note: 1. $\overline{G}$ may be delayed up to t$_{CHQV}$ – t$_{GLQV}$ after the rising edge of R$\overline{C}$ without impact on t$_{CHQV}$.

Figure 12. Read AC Waveforms (A/A Mux Interface)
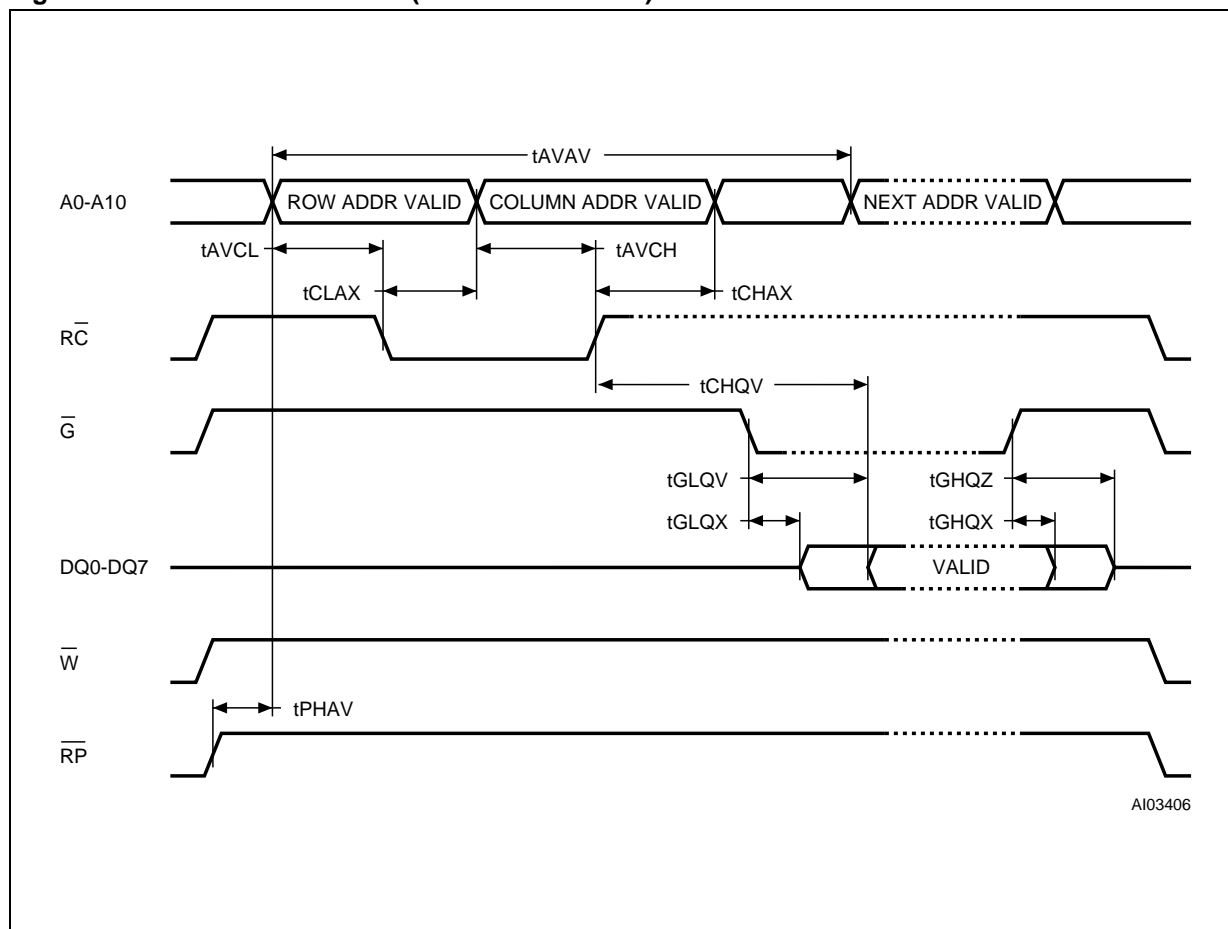
Table 26. Write AC Characteristics (A/A Mux Interface)

Symbol	Parameter	Test Condition		Value	Unit
t_{WLWH}	Write Enable Low to Write Enable High		Min	100	ns
t_{DVWH}	Data Valid to Write Enable High		Min	50	ns
t_{WHDX}	Write Enable High to Data Transition		Min	5	ns
t_{AVCL}	Row Address Valid to $R\overline{C}$ Low		Min	50	ns
t_{CLAX}	$R\overline{C}$ Low to Row Address Transition		Min	50	ns
t_{AVCH}	Column Address Valid to $R\overline{C}$ High		Min	50	ns
t_{CHAX}	$R\overline{C}$ High to Column Address Transition		Min	50	ns
t_{WHWL}	Write Enable High to Write Enable Low		Min	100	ns
t_{CHWH}	$R\overline{C}$ High to Write Enable High		Min	50	ns
t_{VPHWH}[1]	V_{PP} High to Write Enable High		Min	100	ns
t_{WHGL}	Write Enable High to Output Enable Low		Min	30	ns
t_{WHRL}	Write Enable High to $R\overline{B}$ Low		Min	0	ns
t_{QVVPL}[1,2]	Output Valid, $R\overline{B}$ High to V_{PP} Low		Min	0	ns

Note: 1. Sampled only, not 100% tested.
2. Applicable if V_{PP} is seen as a logic input ($V_{PP} < 3.6V$).

Figure 13. Write AC Waveforms (A/A Mux Interface)

Figure 14. Program Flowchart and Pseudo Code

Program command:
– write 40h or 10h
– write Address & Data
  (memory enters read status state after
  the Program command)

do:
–read Status Register if Program/Erase
  Suspend command given execute
  suspend program loop

while b7 = 1

If b3 = 1, V_{PP} invalid error:
– error handler

If b4 = 1, Program error:
– error handler

If b1 = 1, Program to protected block error:
– error handler

AI04433
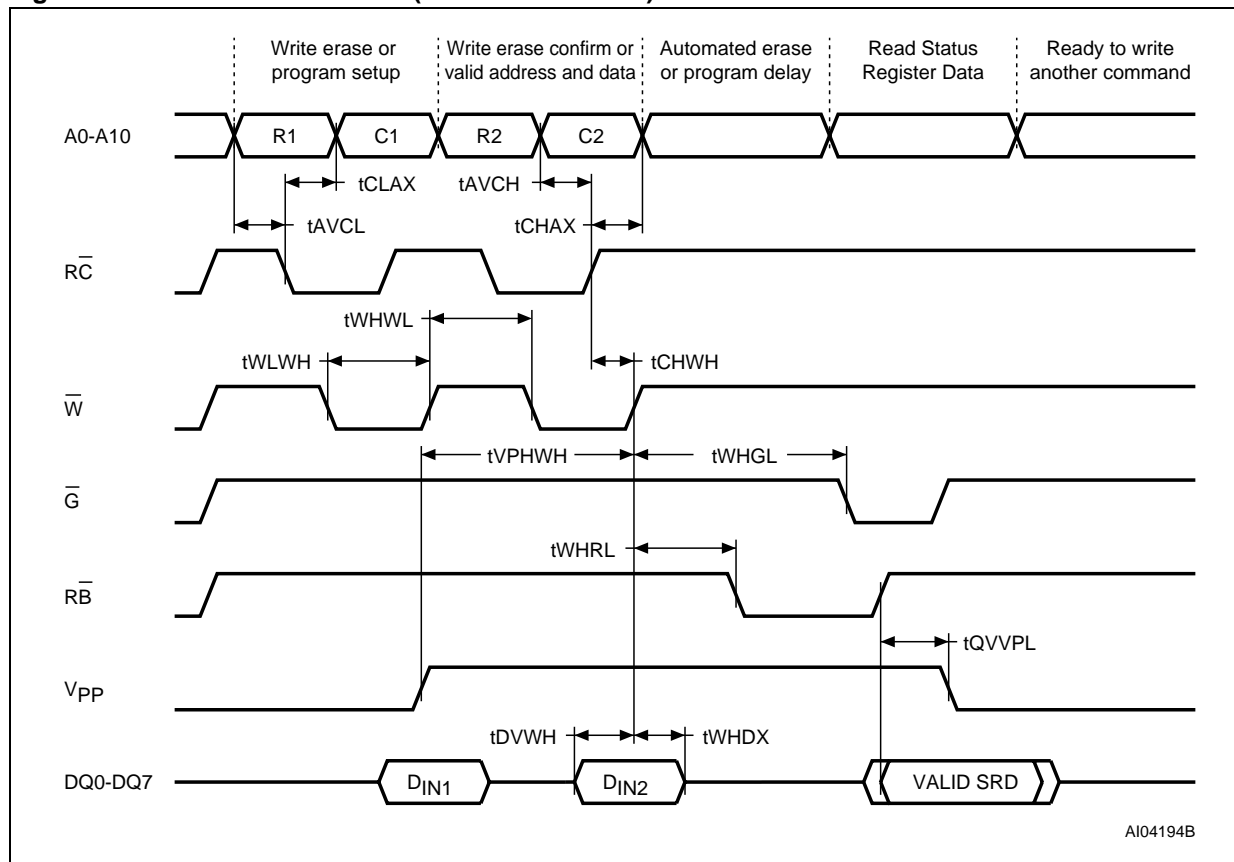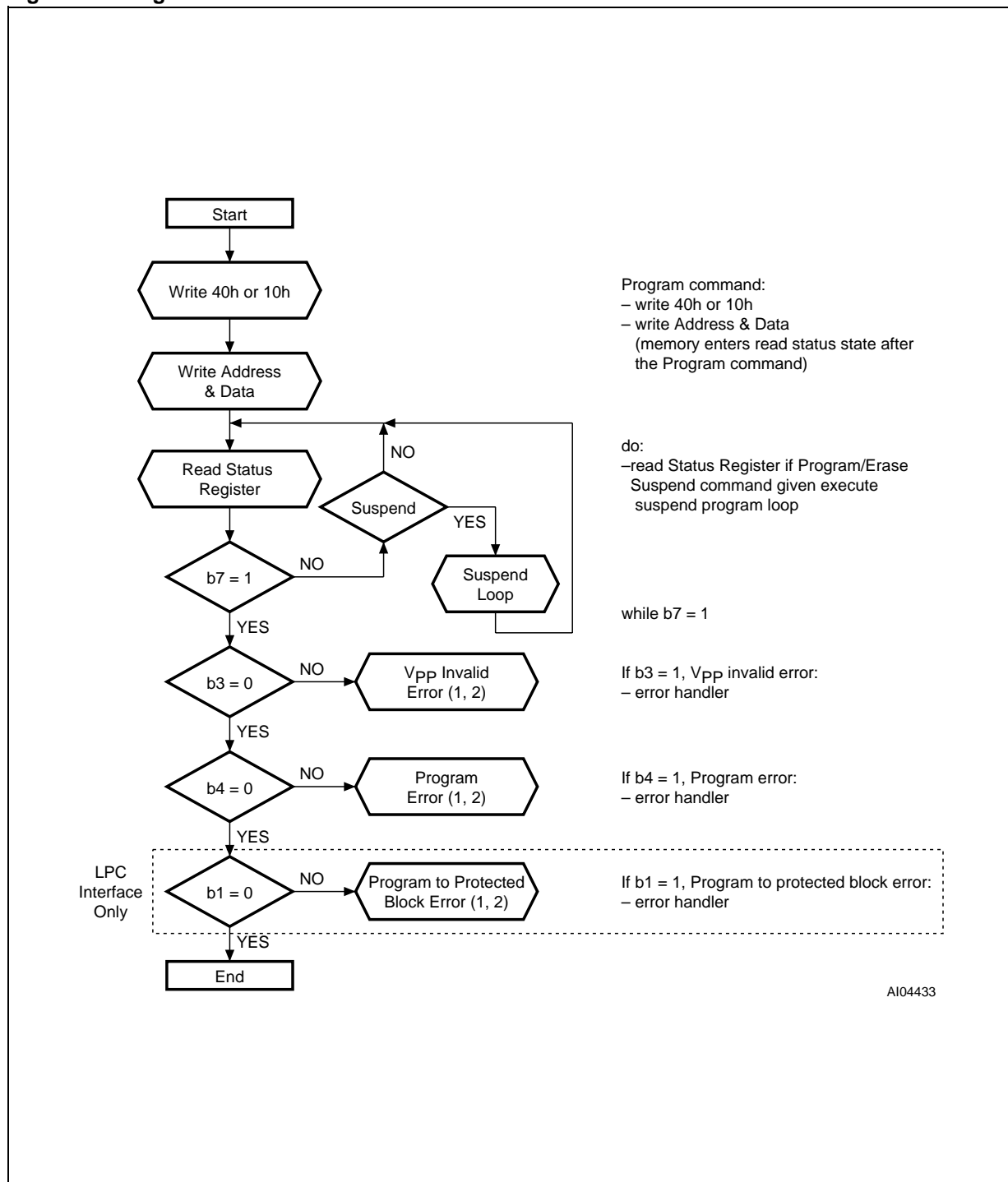
Note: 1. A Status check of b1 (Protected Block), b3 (V_{PP} invalid) and b4 (Program Error) can be made after each Program operation by following the correct command sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 15. Quadruple Byte Program Flowchart and Pseudo Code (A/A Mux Interface Only)

Quadruple Byte Program command:
– write 30h
– write Address 1 & Data 1 [3]
– write Address 2 & Data 2 [3]
– write Address 3 & Data 3 [3]
– write Address 4 & Data 4 [3]
  (memory enters read status state after
  the Quadruple Byte Program command)

do:
– read Status Register if Program/Erase
  Suspend command given execute
  suspend program loop

while b7 = 1

If b3 = 1, V_{PP} invalid error:
– error handler

If b4 = 1, Program error:
– error handler

AI03982
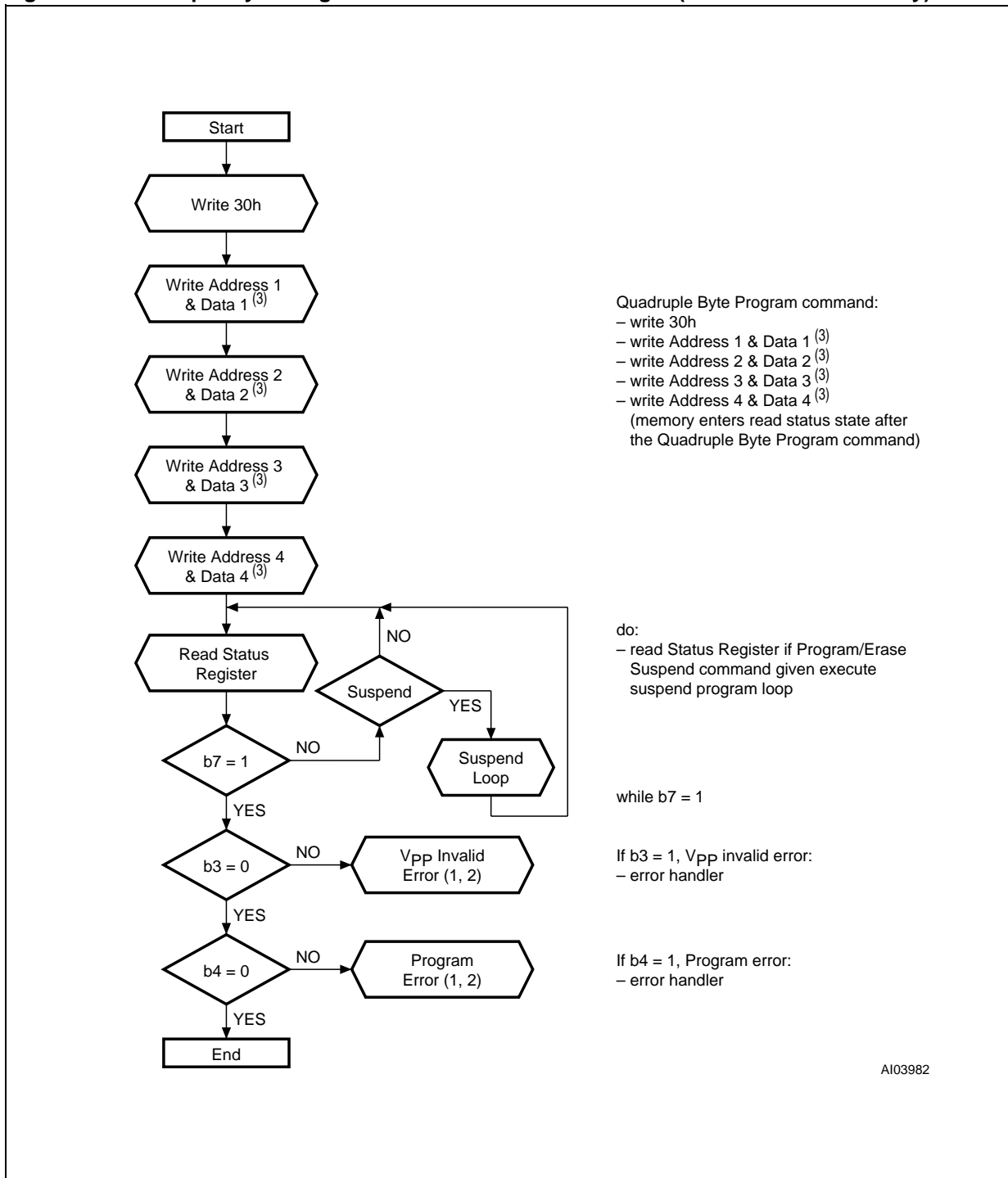
Note: 1. A Status check of b3 (V_{PP} invalid) and b4 (Program Error) can be made after each Program operation by following the correct command sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.
3. Address 1, Address 2, Address 3 and Address 4 must be consecutive addresses differing only for address bits A0 and A1.

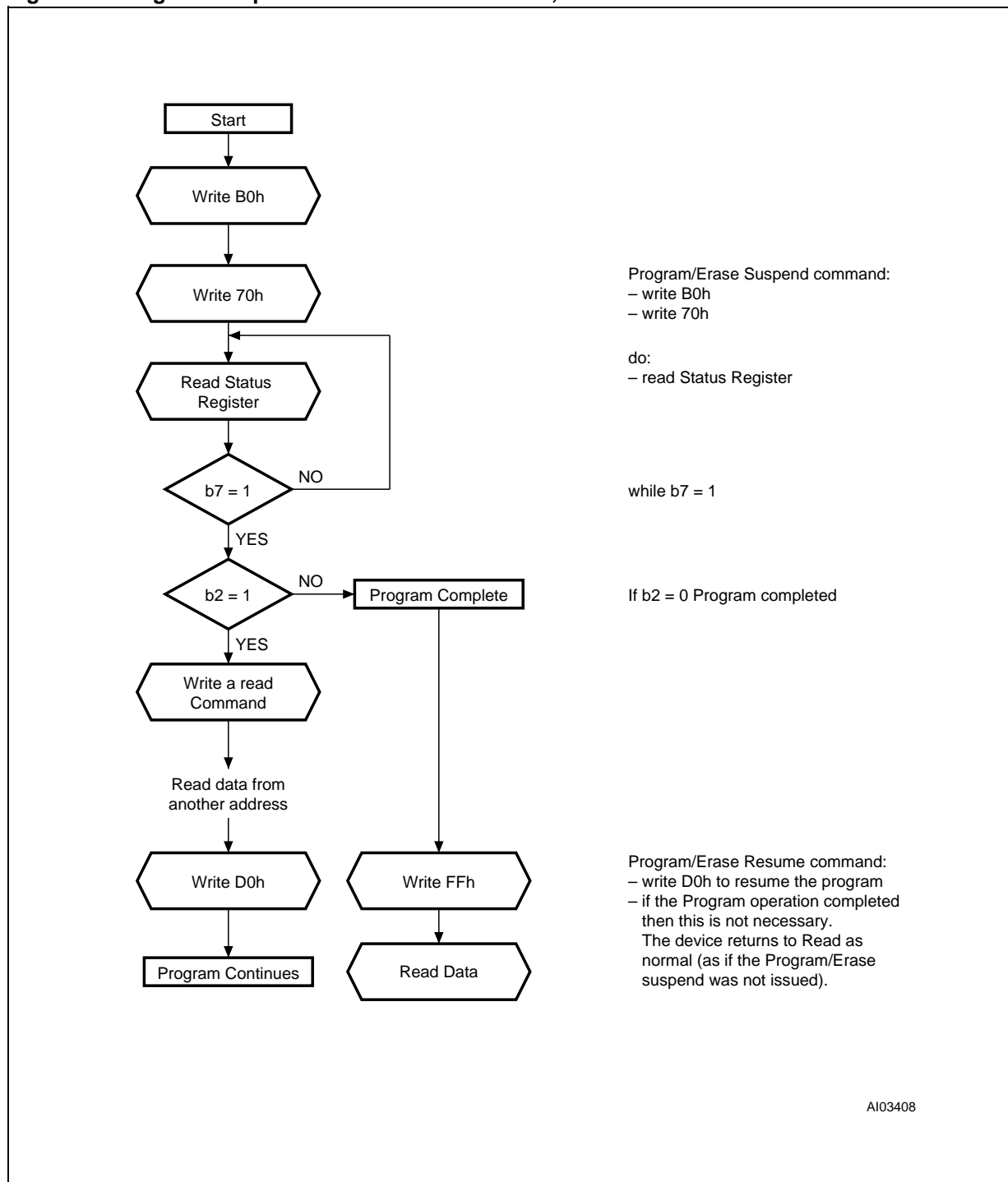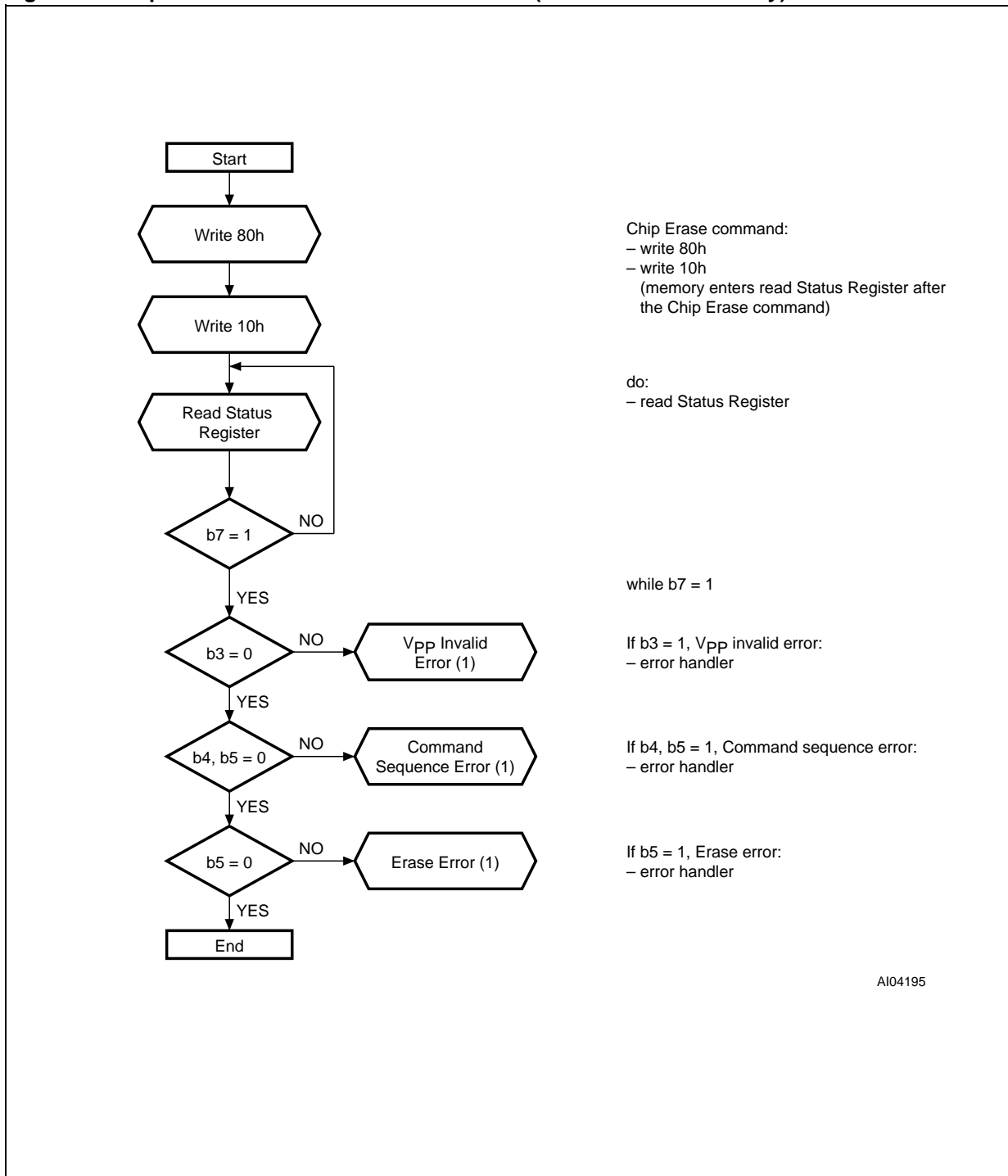**Figure 16. Program Suspend and Resume Flowchart, and Pseudo Code**

```
                    ┌──────────────┐
                    │    Start     │
                    └──────┬───────┘
                           │
                    ╱──────────────╲
                    │  Write B0h   │
                    ╲──────────────╱
                           │                    Program/Erase Suspend command:
                    ╱──────────────╲            – write B0h
                    │  Write 70h   │            – write 70h
                    ╲──────────────╱
                           │                    do:
                    ╱──────────────╲            – read Status Register
                    │ Read Status  │←───┐
                    │  Register    │    │
                    ╲──────────────╱    │
                           │            │
                        ╱──────╲   NO   │
                        │ b7=1 │────────┘       while b7 = 1
                        ╲──────╱
                           │ YES
                        ╱──────╲   NO    ┌─────────────────┐
                        │ b2=1 │────────→│ Program Complete│    If b2 = 0 Program completed
                        ╲──────╱         └────────┬────────┘
                           │ YES                  │
                    ╱──────────────╲              │
                    │ Write a read │              │
                    │   Command    │              │
                    ╲──────────────╱              │
                           │                      │
                    Read data from                │
                    another address               │
                           │                      │
                    ╱──────────────╲     ╱──────────────╲
                    │  Write D0h   │     │  Write FFh   │     Program/Erase Resume command:
                    ╲──────────────╱     ╲──────────────╱     – write D0h to resume the program
                           │                      │           – if the Program operation completed
                    ┌──────────────┐     ╱──────────────╲        then this is not necessary.
                    │  Program     │     │  Read Data   │        The device returns to Read as
                    │  Continues   │     ╲──────────────╱        normal (as if the Program/Erase
                    └──────────────┘                             suspend was not issued).

                                                       AI03408
```

Figure 17. Chip Erase Flowchart and Pseudo Code (A/A Mux Interface Only)


```
Start

Write 80h                          Chip Erase command:
                                   – write 80h
                                   – write 10h
Write 10h                            (memory enters read Status Register after
                                     the Chip Erase command)

Read Status                        do:
Register                           – read Status Register

b7 = 1    NO

YES                                while b7 = 1

b3 = 0    NO   VPP Invalid         If b3 = 1, VPP invalid error:
               Error (1)           – error handler

YES

b4, b5 = 0  NO   Command           If b4, b5 = 1, Command sequence error:
                 Sequence Error (1) – error handler

YES

b5 = 0    NO    Erase Error (1)    If b5 = 1, Erase error:
                                   – error handler

YES

End

                                   AI04195
```

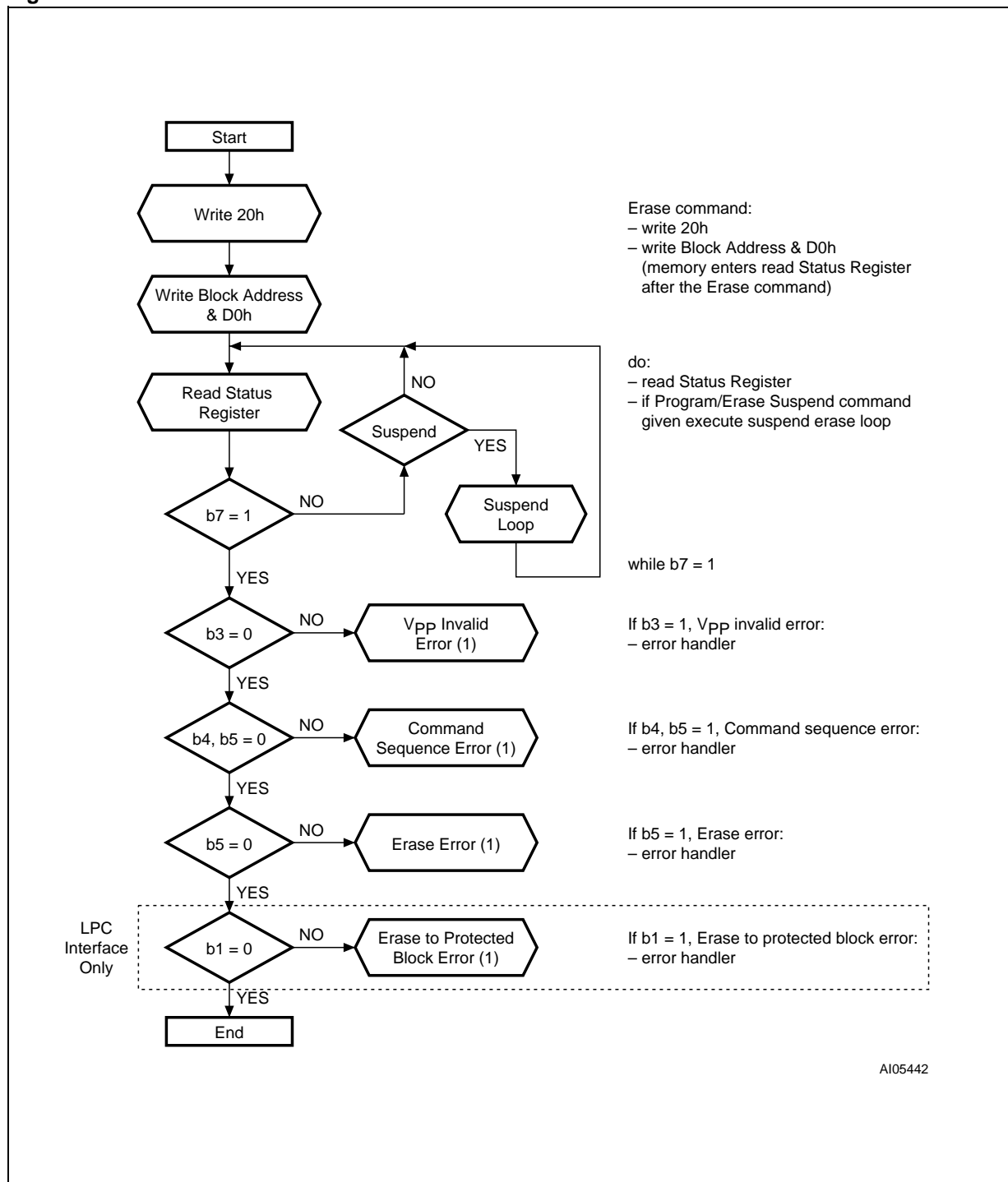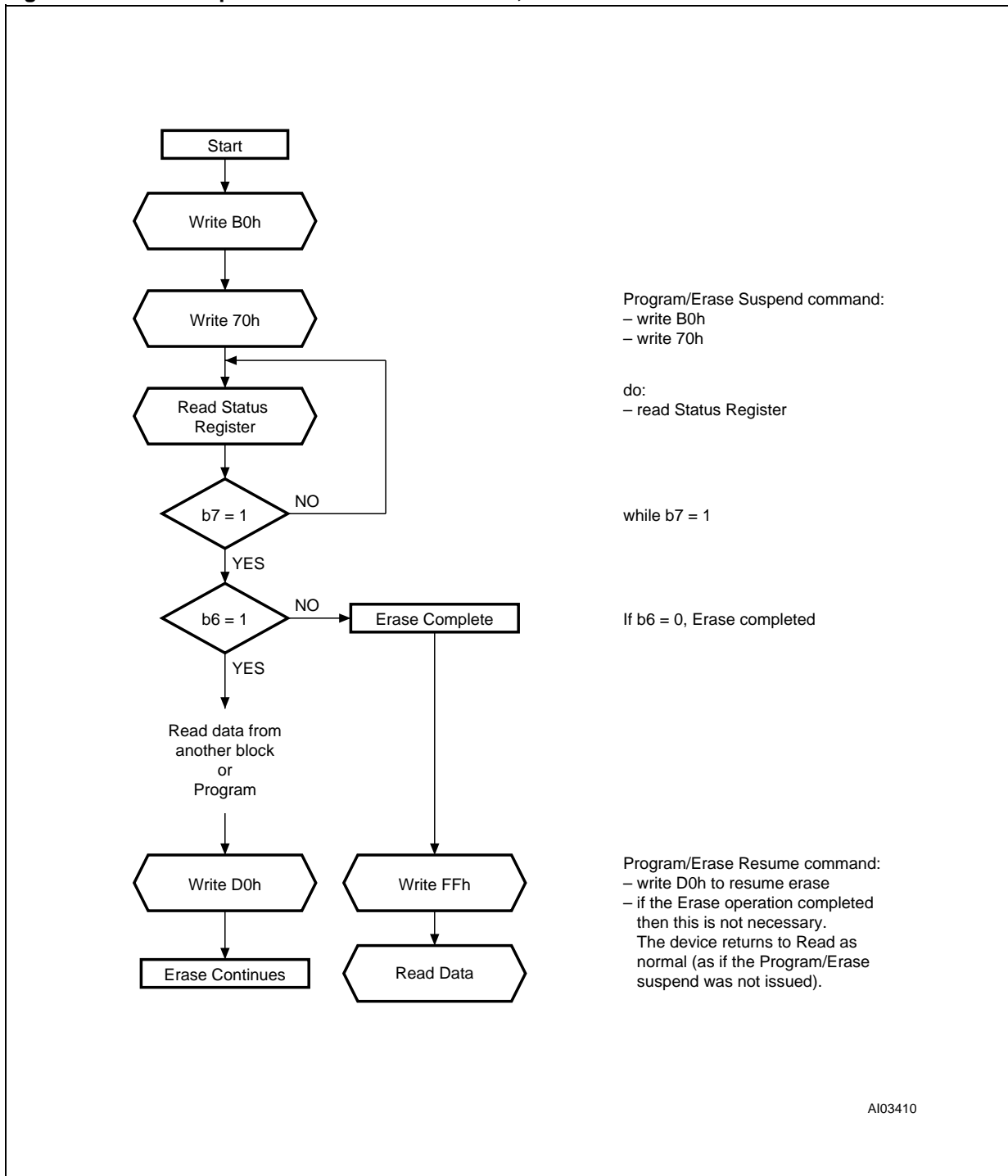Note: 1. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

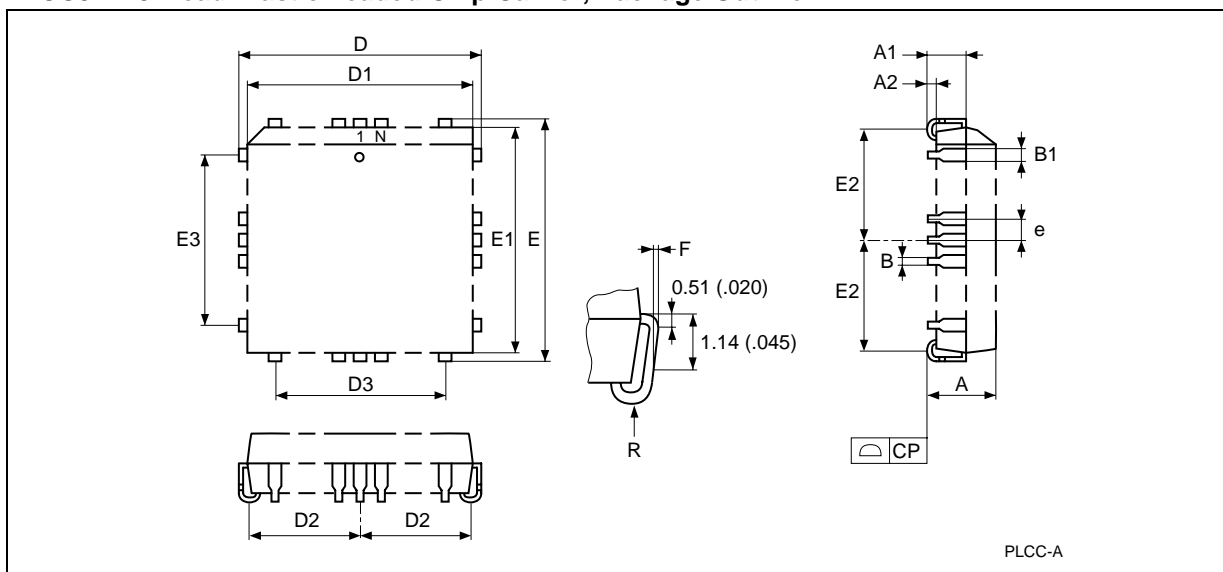**Figure 18. Block Erase Flowchart and Pseudo Code**

Note: 1. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 19. Erase Suspend and Resume Flowchart, and Pseudo Code

Program/Erase Suspend command:
– write B0h
– write 70h

do:
– read Status Register

while b7 = 1

If b6 = 0, Erase completed

Program/Erase Resume command:
– write D0h to resume erase
– if the Erase operation completed
  then this is not necessary.
  The device returns to Read as
  normal (as if the Program/Erase
  suspend was not issued).

AI03410

PACKAGE MECHANICAL

PLCC32 – 32 lead Plastic Leaded Chip Carrier, Package Outline

Note: Drawing is not to scale.

PLCC32 – 32 lead Plastic Leaded Chip Carrier, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.18	3.56		0.125	0.140
A1		1.53	2.41		0.060	0.095
A2		0.38	–		0.015	–
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
CP			0.10			0.004
D		12.32	12.57		0.485	0.495
D1		11.35	11.51		0.447	0.453
D2		4.78	5.66		0.188	0.223
D3	7.62	–	–	0.300	–	–
E		14.86	15.11		0.585	0.595
E1		13.89	14.05		0.547	0.553
E2		6.05	6.93		0.238	0.273
E3	10.16	–	–	0.400	–	–
e	1.27	–	–	0.050	–	–
F		0.00	0.13		0.000	0.005
N		32			32	
R	0.89	–	–	0.035	–	–

PART NUMBERING

Table 27. Ordering Information Scheme

Example: M50LPW002 K 1 T

Device Type
M50

Architecture
LP = Low Pin Count Interface

Operating Voltage
W = 3.0 to 3.6V

Device Function
002 = 2 Mbit (256Kb x8), Boot Block

Package
K = PLCC32

Temperature Range
1 = 0 to 70 °C
5 = –20 to 85°C

Option
T = Tape & Reel Packing
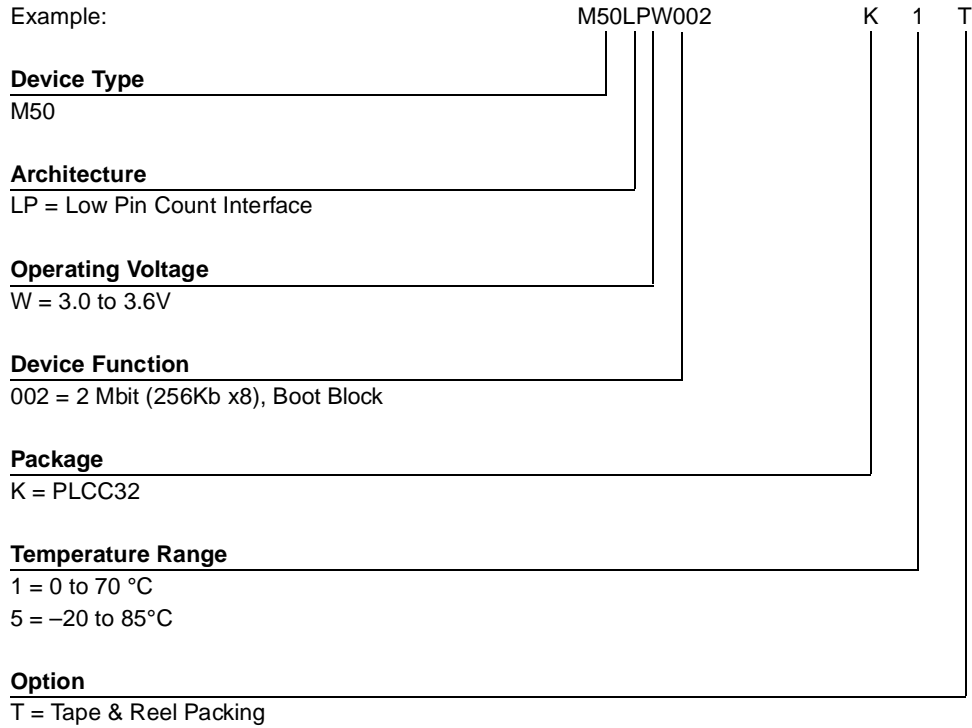
Devices are shipped from the factory with the memory content bits erased to 1. For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

M50LPW002

REVISION HISTORY

Table 28. Document Revision History

Date	Version	Revision Details
14-Dec-2001	-01	Document released
22-Jan-2002	-02	Details of Chip Erase command added
01-Mar-2002	-03	RFU pins must be left disconnected
12-Mar-2002	-04	Specification of PLCC32 package mechanical data revised
31-May-2002	-05	Document promoted from Product Preview to Preliminary Data

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