M6MGB/T160S2BVP

16,777,216-BIT (1,048,576 -WORD BY 16-BIT / 2,097,152-WORD BY 8-BIT) CMOS 3.3V-ONLY FLASH MEMORY &
2,097,152-BIT (131,072-WORD BY 16-BIT / 262,144-WORD BY 8-BIT) CMOS SRAM
Stacked-MCP (Multi Chip Package)

DESCRIPTION

The MITSUBISHI M6MGB/T160S2BVP is a Stacked Multi Chip Package (S-MCP) that contents 16M-bits flash memory and 2M-bits Static RAM in a 48-pin TSOP (TYPE-I).

16M-bits Flash memory is a 2097152 bytes /1048576 words, 3.3V-only, and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR(DIvided bit-line NOR) architecture for the memory cell.
2M-bits SRAM is a 262144 bytes / 131072 words unsynchronous SRAM fabricated by silicon-gate CMOS technology.

M6MGB/T160S2BVP is suitable for the application of the mobile-communication-system to reduce both the mount space and weight .

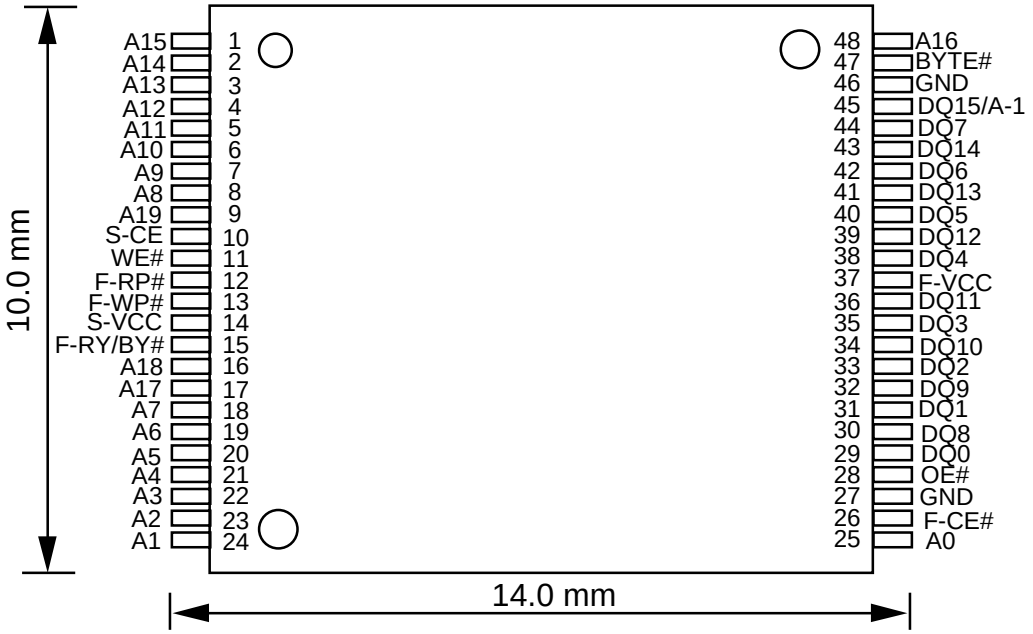
FEATURES

- Access time
  - Flash Memory 90ns (Max.)
  - SRAM 85ns (Max.)
- Supply voltage Vcc=2.7 ~ 3.6V
- Ambient temperature
  - W version Ta=-20 ~ 85°C
- Package : 48-pin TSOP (Type-I) , 0.4mm lead pitch

APPLICATION

Mobile communication products

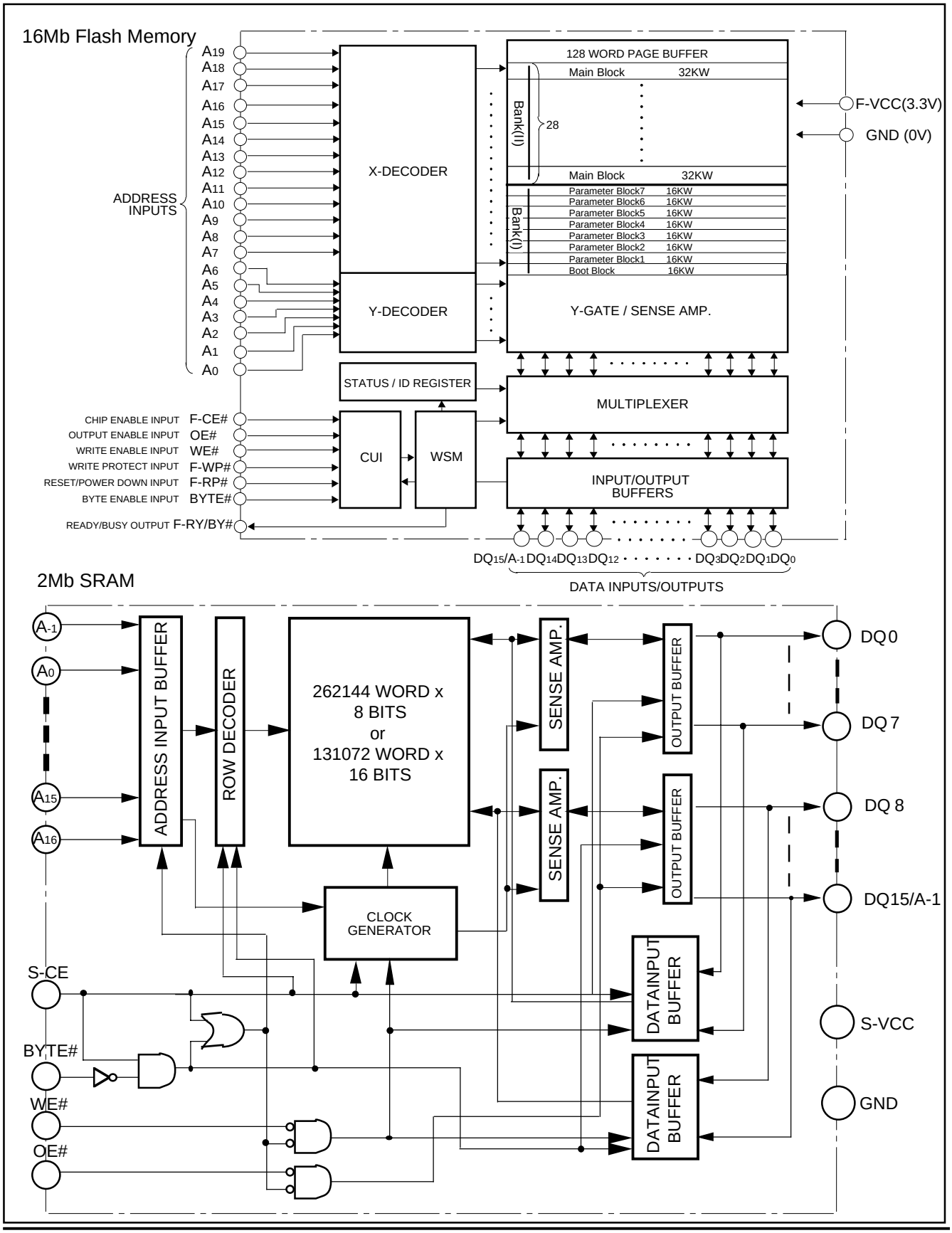
PIN CONFIGURATION (TOP VIEW)



F-VCC	:Vcc for Flash
S-VCC	:Vcc for SRAM
GND	:GND for Flash/SRAM
A-1-A16	:Flash/SRAM common Address
A17-A19	:Address for Flash
DQ0-DQ15	:Data I/O
F-CE#	:Flash Chip Enable
S-CE	:SRAM Chip Enable
OE#	:Flash/SRAM Output Enable
WE#	:Flash/SRAM Write Enable
F-WP#	:Flash Write Protect
F-RP#	:Flash Reset Power Down
F-RY/BY#	:Flash Ready /Busy
BYTE#	:Flash/SRAM Byte Enable

NC:Non Connection

BLOCK DIAGRAM



1. Flash Memory

DESCRIPTION

The Flash Memory of M6MGB/T160S2BVP is 3.3V-only high speed 16,777,216-bit CMOS boot block Flash Memories with alternating BGO (Back Ground Operation) feature. The BGO feature of the device allows Program or Erase operations to be performed in one bank while the device simultaneously allows Read operations to be performed on the other bank. This BGO feature is suitable for mobile and personal computing, and communication products. The Flash Memory of M6MGB/T160S2BVP is fabricated by CMOS technology for the peripheral circuits and DINOR(Divided bit line NOR) architecture for the memory cells.

FEATURES

- Organization ..... 1048,576 word x 16bit
  ..... 2,097,152 word x 8 bit
- Supply voltage ..... V_{CC} = 2.7~3.6V
- Access time ..... 90ns (Max.)
- Power Dissipation
  - Read ..... 54 mW (Max. at 5MHz)
  - (After Automatic Power saving) ..... 0.33μW (typ.)
  - Program/Erase ..... 126 mW (Max.)
  - Standby ..... 0.33μW (typ.)
  - Deep power down mode ..... 0.33μW (typ.)
- Auto program for Bank(I)
  - Program Time ..... 4ms (typ.)
  - Program Unit
    - (Byte Program) 1word/1byte
    - (Page Program) 128word/256byte
- Auto program for Bank(II)
  - Program Time ..... 4ms (typ.)
  - Program Unit 128word/256byte
- Auto Erase
  - Erase time ..... 40 ms (typ.)
  - Erase Unit
    - Bank(I) Boot Block ..... 16Kword/32Kbyte x 1
    - Parameter Block ..... 16Kword/32Kbyte x 7
    - Bank(II) Main Block ..... 32Kword/64Kbyte x 28
- Program/Erase cycles 100Kcycles
- Boot Block
  - M6MGB160S2BVP ..... Bottom Boot
  - M6MGT160S2BVP ..... Top Boot
- Other Functions
  - Soft Ware Command Control
  - Selective Block Lock
  - Erase Suspend/Resume
  - Program Suspend/Resume
  - Status Register Read
  - Alternating Back Ground Program/Erase Operation Between Bank(I) and Bank(II)

FUNCTION

The Flash Memory of M6MGB/T160S2BVP includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and byte/page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.
A Deep Powerdown mode is enabled when the F-RP# pin is at GND, minimizing power consumption.

Read
The Flash Memory of M6MGB/T160S2BVP has three read modes, which accesses to the memory array, the Device Identifier and the Status Register. The appropriate read command are required to be written to the CUI. Upon initial device powerup or after exit from deep powerdown, the Flash Memory automatically resets to read array mode. In the read array mode, low level input to F-CE# and OE#, high level input to WE# and F-RP#, and address signals to the address inputs (A19-A-1:Byte Mode, A19-A0:Word Mode) output the data of the addressed location to the data input/output (D7-D0:Byte Mode, D15-D0:Word Mode).

Write
Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing WE# to low level, while F-CE# is at low level and OE# is at high level. Address and data are latched on the earlier rising edge of WE# and F-CE#. Standard micro-processor write timings are used.

Alternating Background Operation (BGO)
The Flash Memory of M6MGB/T160S2BVP allows to read array from one bank while the other bank operates in software command write cycling or the erasing / programming operation in the background. Read array operation with the other bank in BGO is performed by changing the bank address without any additional command. When the bank address points the bank in software command write cycling or the erasing / programming operation, the data is read out from the status register. The access time with BGO is the same as the normal read operation.

Output Disable
When OE# is at VIH, output from the devices is disabled. Data input/output are in a high-impedance(High-Z) state.

Standby
When F-CE# is at VIH, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance(High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consume normal active power until the operation completes.

Deep Power-Down
When F-RP# is at VIL, the device is in the deep powerdown mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance(High-Z) state. After return from powerdown, the CUI is reset to Read Array , and the Status Register is cleared to value 80H.
During block erase or program modes, F-RP# low will abort either operation. Memory array data of the block being altered become invalid.

Automatic Power-Saving (APS)
The Automatic Power-Saving minimizes the power consumption during read mode. The device automatically turns to this mode when any addresses or F-CE# isn't changed more than 200ns after the last alternation. The power consumption becomes the same as the stand-by mode. While in this mode, the output data is latched and can be read out. New data is read out correctly when addresses are changed.

SOFTWARE COMMAND DEFINITIONS

The device operations are selected by writing specific software command into the Command User Interface.

Read Array Command (FFH)

The device is in Read Array mode on initial device power up and after exit from deep powerdown, or by writing FFH to the Command User Interface. After starting the internal operation the device is set to the read status register mode automatically.

Read Device Identifier Command (90H)

It can normally read device identifier codes when Read Device Identifier Code Command(90H) is written to the command latch. Following the command write, the manufacturer code and the device code can be read from address 0000H and 0001H, respectively.

Read Status Register Command (70H)

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface. Also, after starting the internal operation the device is set to the Read Status Register mode automatically.
The contents of Status Register are latched on the later falling edge of OE# or F-CE#. So F-CE# or OE# must be toggled every status read.

Clear Status Register Command (50H)

The Erase Status, Program Status and Block Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicates various failure conditions.

Block Erase / Confirm Command (20H/D0H)

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

Program Commands

A)Word/Byte Program (40H)

Word/Byte program is executed by a two-command sequence. The Word/Byte Program Setup command of 40H is written to the Command Interface, followed by a second write specifying the address and data to be written. The WSM controls the program pulse application and verify operation. The Word/Byte Program Command is Valid for only Bank(I).

B)Page Program for Data Blocks (41H)

Page Program for Bank(I) and Bank(II) allows fast programming of 128words/256bytes of data. Writing of 41H initiates the page program operation for the Data area. From 2nd cycle to 257th cycle (Byte Mode)129th cycle (Word Mode), write data must be serially inputted. Address A6-A0,A-1 (Byte Mode) / A6-A0 (Word Mode) have to be incremented from 00H to 7FH/FFH. After completion of data loading, the WSM controls the program pulse application and verify operation.

C)Single Data Load to Page Buffer (74H) / Page Buffer to Flash (0EH/D0H)

Single data load to the page buffer is performed by writing 74H followed by a second write specifying the column address and data. Distinct data up to 256byte/128word can be loaded to the page buffer by this two-command sequence. On the other hand, all of the loaded data to the page buffer is programed simultaneously by writing Page Buffer to Flash command of 0EH followed by the confirm command of D0H. After completion of programing the data on the page buffer is cleared automatically.
This command is valid for only Bank(I) alike Word/Byte Program.

Clear Page Buffer Command (55H)

Loaded data to the page buffer is cleared by writing the Clear Page Buffer command of 55H followed by the Confirm command of D0H. This command is valid for clearing data loaded by Single Data Load to Page Buffer command.

Suspend/Resume Command (B0H/D0H)

Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The Bank address is required when writing the Suspend/Resume Command. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

DATA PROTECTION

The Flash Memory of M6MGB/T160S2BVP provides selectable block locking of memory blocks. Each block has an associated nonvolatile lock-bit which determines the lock status of the block. In addition, the Flash Memory has a master Write Protect pin (F-WP#) which prevents any modifications to memory blocks whose lock-bits are set to "0", when F-WP# is low. When F-WP# is high, all blocks can be programmed or erased regardless of the state of the lock-bits, and the lock-bits are cleared to "1" by erase. See the BLOCK LOCKING table on P.9 for details.

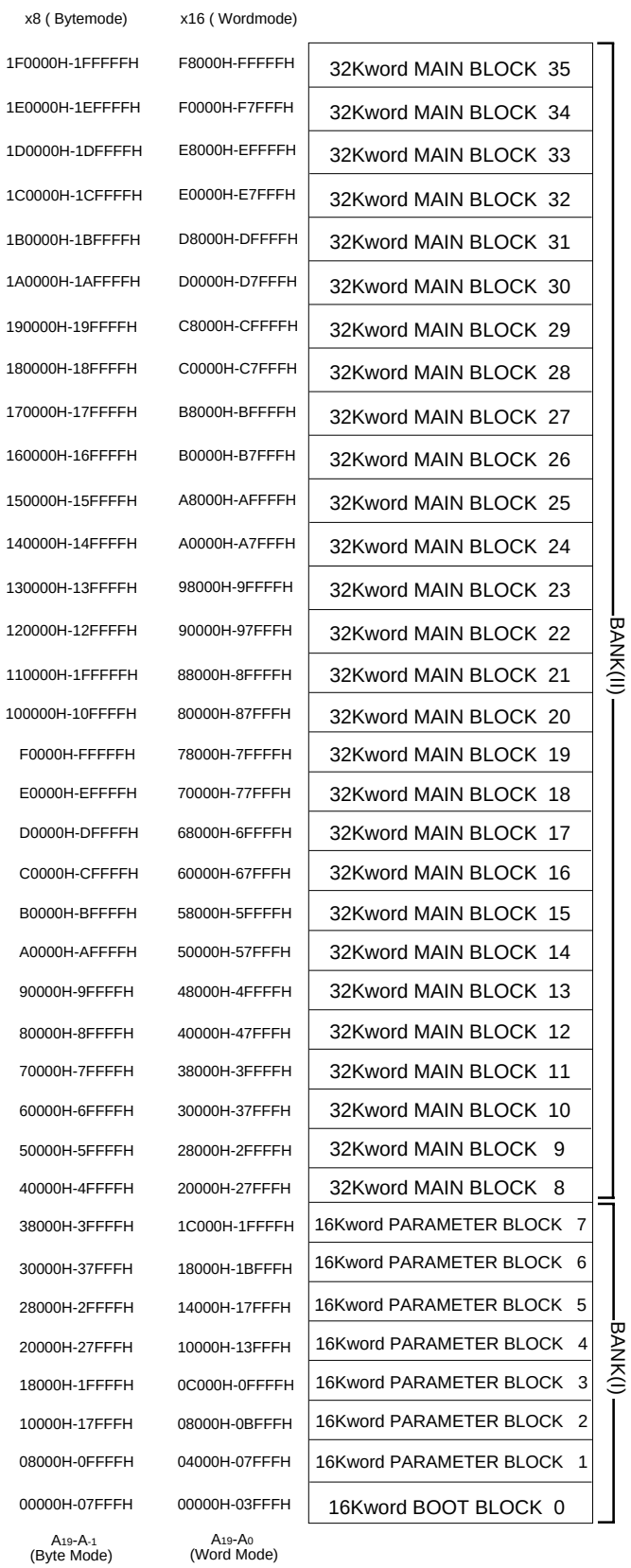
Power Supply Voltage

When the power supply voltage (F-VCC) is less than V_{LKO}, Low V_{CC} Lock-Out voltage, the device is set to the Read-only mode. Regarding DC electrical characteristics of V_{LKO}, see P.10.
A delay time of 2 us is required before any device operation is initiated. The delay time is measured from the time F-Vcc reaches F-Vccmin (2.7V).
During power up, F-RP#=GND is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

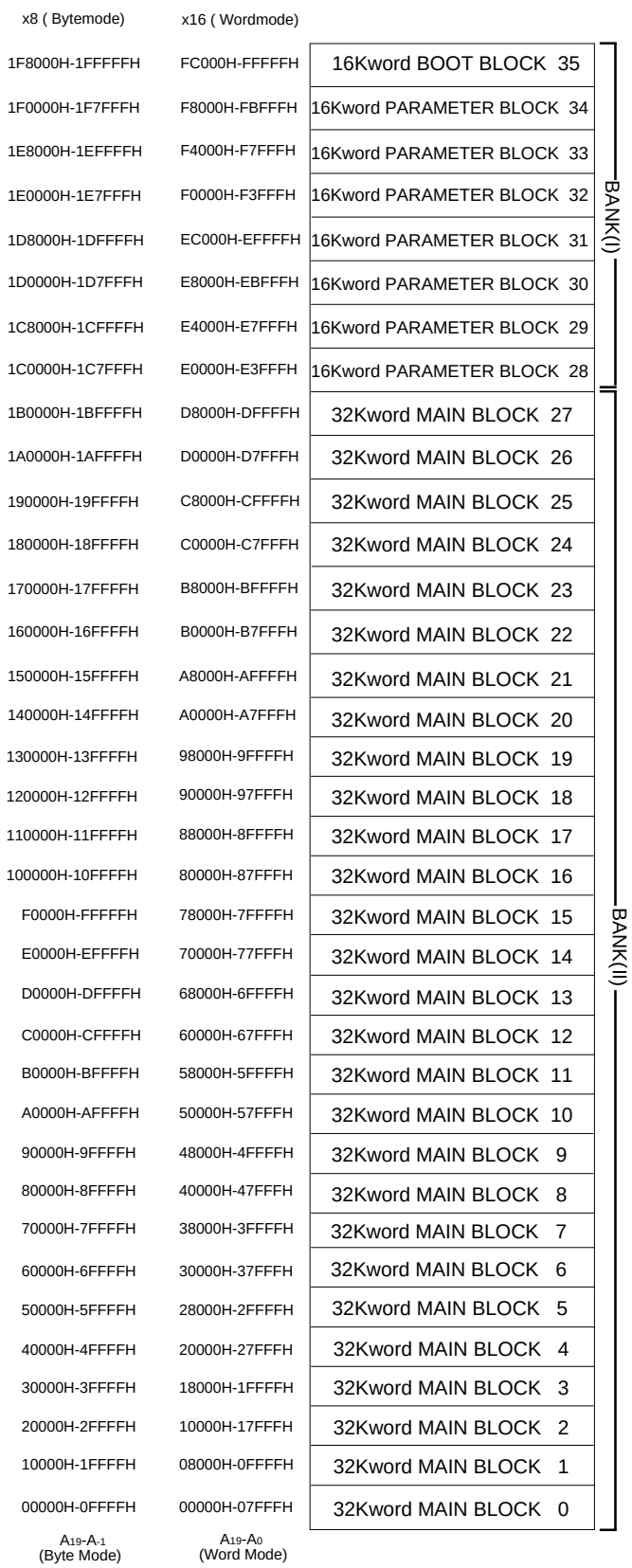
MEMORY ORGANIZATION

The Flash Memory of M6MGB/T160S2BVP has one 32Kbyte boot block, seven 32Kbyte parameter blocks, for Bank(I) and twenty-eight 64Kbyte main blocks for Bank(II). A block is erased independently of other blocks in the array.

MEMORY ORGANIZATION



Flash Memory of M6MGB160S2BVP Memory Map



Flash Memory of M6MGT160S2BVP Memory Map

BUS OPERATIONS

Bus Operations for Word-Wide Mode

Mode \ Pins		F-CE#	OE#	WE#	F-RP#	DQ0-15	F-RY/BY#
Read	Array	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data out	V_{OH} (Hi-Z)
	Status Register	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Status Register Data	X [1]
	Lock Bit Status	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Lock Bit Data (DQ6)	X
	Identifier Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Identifier Code	V_{OH} (Hi-Z)
Output disable		V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	X
Stand by		V_{IH}	X [2]	X	V_{IH}	Hi-Z	X
Write	Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command/Data in	X
	Erase	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command	X
	Others	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command	X
Deep Power Down		X	X	X	V_{IL}	Hi-Z	V_{OH} (Hi-Z)

Bus Operations for Byte-Wide Mode

Mode \ Pins		F-CE#	OE#	WE#	F-RP#	DQ0-7	F-RY/BY#
Read	Array	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Data out	V_{OH} (Hi-Z)
	Status Register	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Status Register Data	X [1]
	Lock Bit Status	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Lock Bit Data (DQ6)	X
	Identifier Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Identifier Code	V_{OH} (Hi-Z)
Output disable		V_{IL}	V_{IH}	V_{IH}	V_{IH}	Hi-Z	X
Stand by		V_{IH}	X [2]	X	V_{IH}	Hi-Z	X
Write	Program	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command/Data in	X
	Erase	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command	X
	Others	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command	X
Deep Power Down		X	X	X	V_{IL}	Hi-Z	V_{OH} (Hi-Z)

1) X at F-RY/BY# is V_{OL} or V_{OH}(Hi-Z).
*The F-RY/BY# is an open drain output pin and indicates status of the internal WSM. When low,it indicates that the WSM is Busy performing an operation. A pull-up resistor of 10K-100K Ohms is required to allow the F-RY/BY# signal to transition high indicating a Ready WSM condition.
2) X can be V_{IH} or V_{IL} for control pins.

SOFTWARE COMMAND DEFINITION

Command List

Command	1st bus cycle			2nd bus cycle			3rd ~257th bus cycles (Byte Mode) 3rd ~129th bus cycles (Word Mode)		
	Mode	Address	Data (DQ7-0) (DQ15-0) 1)	Mode	Address	Data (DQ7-0) (DQ15-0)	Mode	Address	Data (DQ7-0) (DQ15-0)
Read Array	Write	X	FFH						
Device Identifier	Write	X	90H	Read	IA 2)	ID 2)			
Read Status Register	Write	Bank3)	70H	Read	Bank	SRD4)			
Clear Status Register	Write	X	50H						
Clear Page Buffer	Write	X	55H	Write	X	D0H 1)			
Byte/Word Program 5)	Write	Bank(I) 5)	40H	Write	WA 6)	WD 6)			
Page Program 7)	Write	Bank	41H	Write	WA0 7)	WD0 7)	Write	WAn 7)	WDn 7)
Single Data Load to Page Buffer 5)	Write	Bank(I) 5)	74H	Write	WA	WD			
Page Buffer to Flash 5)	Write	Bank(I) 5)	0EH	Write	WA 8)	D0H 1)			
Block Erase / Confirm	Write	Bank	20H	Write	BA 9)	D0H 1)			
Suspend	Write	Bank	B0H						
Resume	Write	Bank	D0H						
Read Lock Bit Status	Write	X	71H	Read	BA	DQ6 10)			
Lock Bit Program / Confirm	Write	Bank	77H	Write	BA	D0H 1)			
Erase All Unlocked Blocks	Write	X	A7H	Write	X	D0H 1)			

1) In the word-wide version(Byte#=H), upper byte data (DQ8-DQ15) is ignored.
2) IA=ID Code Address : A0=VIL (Manufacturer's Code) : A0=VIH (Device Code), ID=ID Code
3) Bank = Bank Address (Bank(I) or Bank(II)) : A19-A17.
4) SRD = Status Register Data
5) Byte/Word Program, Single Data Load and Page Buffer to Flash Command is valid for only Bank(I).
6) WA = Write Address,WD = Write Data
7) WA0,WAn=Write Address, WD0,WDn=Write Data.
Byte Mode : Write Address and Write Data must be provided sequentially from 00H to FFH for A6-A0,A-1. Page size is 256Byte (256byte x 8bit), and also A19-A7(Block Address, Page Address) must be valid.
Word Mode : Write Address and Write Data must be provided sequentially from 00H to 7FH for A6-A0. Page size is 128word (128word x 16bit). and also A19-A7(Block Address, Page Address) must be valid.
8) WA = Write Address : Upper page address, A19-A7(Block Address, Page Address) must be valid.
9) BA = Block Address : BA = Block Address : A19-A14(Bank1) A19-A15(Bank2)
10) DQ6 provides Block Lock Status, DQ6 = 1 : Block Unlock, DQ6 = 0 : Block Locked.

BLOCK LOCKING

		Lock Bit (Internally)	Write Protection Provided				Note
			BANK(I)		BANK(II)	Lock Bit	
F-RP#	F-WP#		Boot	Parameter	Data		
V_{IL}	X	X	Locked	Locked	Locked	Locked	Deep Power Down Mode
V_{IH}	V_{IL}	0	Locked	Locked	Locked	Locked	
		1	Locked	Unlocked	Unlocked	Locked	
	V_{IH}	X	Unlocked	Unlocked	Unlocked	Unlocked	All Blocks Unlocked

1) DQ_6 provides Lock Status of each block after writing the Read Lock Status command (71H).
F-WP# pins must not be switched during performing Erase / Write operations or WSM Busy (WSMS = 0).
2) Erase/Write command for locked blocks is aborted. At this time read mode is not array read mode but status read mode and 00B0H is read. Please issue Clear Status Register command plus Read Array command to change the mode from status read mode to array read mode.

STATUS REGISTER

Symbol	Status	Definition	
		"1"	"0"
SR.7 (DQ_7)	Write State Machine Status	Ready	Busy
SR.6 (DQ_6)	Suspend Status	Suspended	Operation in Progress / Completed
SR.5 (DQ_5)	Erase Status	Error	Successful
SR.4 (DQ_4)	Program Status	Error	Successful
SR.3 (DQ_3)	Block Status after Program	Error	Successful
SR.2 (DQ_2)	*Reserved*	-	-
SR.1 (DQ_1)	*Reserved*	-	-
SR.0 (DQ_0)	*Reserved*	-	-

*The F-RY/BY# is an open drain output pin and indicates status of the internal WSM. When low,it indicates that the WSM is Busy performing an operation. A pull-up resistor of 10K-100K Ohms is required to allow the F-RY/BY# signal to transition high indicating a Ready WSM condition.
*DQ3 indicates the block status after the page programming, byte/word programming and page buffer to flash. When DQ3 is "1", the page has the over-programed cell . If over-program occurs, the device is block fail. However if DQ3 is "1", please try the block erase to the block. The block may revive.

DEVICE IDENTIFIER CODE

Code \ Pins	A_0	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0	Hex. Data
Manufacturer Code	V_{IL}	0	0	0	1	1	1	0	0	1CH
Device Code (-T160S2BVP)	V_{IH}	1	0	1	0	0	0	0	0	A0H
Device Code (-B160S2BVP)	V_{IH}	1	0	1	0	0	0	0	1	A1H

In the word-wide mode, the upper data(D_{15-8}) is "0".

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
F-V_{CC}	Flash V_{CC} voltage	With respect to Ground	-0.2	4.6	V
V_{I1}	All input or output voltage 1)		-0.6	4.6	V
T_a	Ambient temperature		-20	85	°C
T_{bs}	Temperature under bias		-50	95	°C
T_{stg}	Storage temperature		-65	125	°C
I_{OUT}	Output short circuit current			100	mA

1) Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is F-V_{CC}+0.5V which, during transitions, may overshoot to F-V_{CC}+1.5V for periods <20ns.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, Control Pins)	Ta = 25°C, f = 1MHz, V_{in} = V_{out} = 0V			8	pF
C_{OUT}	Output capacitance				12	pF

Note: The value of common pins to Flash Memory is the sum of Flash Memory and SRAM.

DC ELECTRICAL CHARACTERISTICS (Ta = -20~ 85°C, F-Vcc = 2.7V ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ1)	Max	
I_{LI}	Input leakage current	0V≤V_{IN}≤F-V_{CC}				±2.0	μA
I_{LO}	Output leakage current	0V≤V_{OUT}≤F-V_{CC}				±11	μA
I_{SB1}	F-V_{CC} standby current	F-VCC = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP# = VIH			50	200	μA
I_{SB2}		F-V_{CC} = 3.6V, V_{IN}=GND or F-V_{CC}, F-CE# = F-RP# = F-WP# = F-V_{CC}±0.3V			0.1	5	μA
I_{SB3}	F-V_{CC} deep powerdown current	F-V_{CC} = 3.6V, V_{IN}=V_{IL}/V_{IH}, F-RP# = V_{IL}			5	15	μA
I_{SB4}		F-VCC = 3.6V, VIN=GND or VCC, F-RP# =GND±0.3V			0.1	5	μA
I_{CC1}	F-V_{CC} read current for Word or Byte	F-V_{CC} = 3.6V, V_{IN}=V_{IL}/V_{IH}, F-CE# = V_{IL}, F-RP#=OE#=V_{IH}, I_{OUT} = 0mA	5MHz		8	15	mA
			1MHz		2	4	
I_{CC2}	F-V_{CC} Write current for Word or Byte	F-V_{CC} = 3.6V,V_{IN}=V_{IL}/V_{IH}, F-CE# =WE#= V_{IL}, F-RP#=OE#=V_{IH}				15	mA
I_{CC3}	F-V_{CC} program current	F-VCC = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP# = VIH				35	mA
I_{CC4}	F-V_{CC} erase current	F-VCC = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP# = VIH				35	mA
I_{CC5}	F-V_{CC} suspend current	F-VCC = 3.6V, VIN=VIL/VIH, F-CE# = F-RP# =F-WP# = VIH				200	μA
V_{IL}	Input low voltage			– 0.5		0.8	V
V_{IH}	Input high voltage			2.0		F-Vcc+0.5	V
V_{OL}	Output low voltage	I_{OL} = 4.0mA				0.45	V
V_{OH1}	Output high voltage	I_{OH} = –2.0mA		0.85(F-Vcc)			V
V_{OH2}		I_{OH} = –100μA		F-Vcc–0.4			V
V_{LKO}	Low V_{CC} Lock-Out voltage 2)			1.5		2.2	V

All currents are in RMS unless otherwise noted.
1) Typical values at F-Vcc=3.3V, Ta=25°C
2) To protect against initiation of write cycle during Vcc power-up/ down, a write cycle is locked out for Vcc less than V_{LKO}.
If Vcc is less than V_{LKO}, Write State Machine is reset to read mode. When the Write State Machine is in Busy state, if Vcc is less than V_{LKO}, the alteration of memory contents may occur.

AC ELECTRICAL CHARACTERISTICS (Ta = -20 ~85°C)

Read-Only Mode

Symbol		Parameter	Limits			Unit
			Speed Item: -90			
			F-Vcc=2.7~3.6V			
			Min	Typ	Max	
t_{RC}	t_{AVAV}	Read cycle time	90			ns
$t_{a\ (AD)}$	t_{AVQV}	Address access time			90	ns
$t_{a\ (CE)}$	t_{ELQV}	Chip enable access time			90	ns
$t_{a\ (OE)}$	t_{GLQV}	Output enable access time			30	ns
t_{CLZ}	t_{ELQX}	Chip enable to output in low-Z	0			ns
$t_{DF(CE)}$	t_{EHQZ}	Chip enable high to output in high Z			25	ns
t_{OLZ}	t_{GLQX}	Output enable to output in low-Z	0			ns
$t_{DF(OE)}$	t_{GHQZ}	Output enable high to output in high Z			25	ns
t_{PHZ}	t_{PLQZ}	F-RP# low to output high-Z			150	ns
$t_{a(BYTE)}$	$t_{FL/HQV}$	BYTE# access time			90	ns
t_{BHZ}	t_{FLQZ}	BYTE# low to output high-Z			25	ns
t_{OH}	t_{OH}	Output hold from CE#, OE#, addresses	0			ns
t_{BCD}	$t_{ELFL/H}$	F-CE# low to BYTE# high or low			5	ns
t_{BAD}	$t_{AVFL/H}$	Address to BYTE# high or low			5	ns
t_{OEH}	t_{WHGL}	OE# hold from WE# high	10			ns
t_{PS}	t_{PHEL}	F-RP# recovery to F-CE# low	150			ns

Timing measurements are made under AC waveforms for read operations.

AC ELECTRICAL CHARACTERISTICS (Ta = -20 ~85°C)

Write Mode (WE# control)

Symbol		Parameter	Limits			Unit
			Speed Item: -90			
			F-Vcc=2.7~3.6V			
			Min	Typ	Max	
t_{WC}	t_{AVAV}	Write cycle time	90			ns
t_{AS}	t_{AVWH}	Address set-up time	50			ns
t_{AH}	t_{WHAX}	Address hold time	0			ns
t_{DS}	t_{DVWH}	Data set-up time	50			ns
t_{DH}	t_{WHDX}	Data hold time	0			ns
t_{OEH}	t_{WHGL}	OE# hold from WE# high	10			ns
t_{RE}	-	Latency between Read and Write FFH or 71H	30			ns
t_{CS}	t_{ELWL}	Chip enable set-up time	0			ns
t_{CH}	t_{WHEH}	Chip enable hold time	0			ns
t_{WP}	t_{WLWH}	Write pulse width	60			ns
t_{WPH}	t_{WHWL}	Write pulse width high	30			ns
t_{BS}	$t_{FL/HWH}$	Byte enable high or low set-up time	50			ns
t_{BH}	$t_{WHFL/H}$	Byte enable high or low hold time	90			ns
t_{GHWL}	t_{GHWL}	OE# hold to WE# Low	0			ns
t_{BLS}	t_{PHHWH}	Block Lock set-up to write enable high	90			ns
t_{BLH}	t_{QVPH}	Block Lockhold from valid SRD	0			ns
t_{DAP}	t_{WHRH1}	Duration of auto-program operation		4	80	ms
t_{DAE}	t_{WHRH2}	Duration of auto-block erase operation		40	600	ms
t_{WHRL}	t_{WHRL}	WE# high to F-RY/BY# low			90	ns
t_{PS}	t_{PHWL}	F-RP# high recovery to write enable low	150			ns

Read timing parameters during command write operations mode are the same as during read-only operations mode.
Typical values at F-Vcc=3.3V, Ta=25°C

AC ELECTRICAL CHARACTERISTICS (Ta = -20 ~ 85°C)

Write Mode (CE# control)

Symbol		Parameter	Limits			Unit
			Speed Item: -90			
			F-Vcc=2.7~3.6V			
			Min	Typ	Max	
t_{WC}	t_{AVAV}	Write cycle time	90			ns
t_{AS}	t_{AVWH}	Address set-up time	50			ns
t_{AH}	t_{EHAX}	Address hold time	0			ns
t_{DS}	t_{DVWH}	Data set-up time	50			ns
t_{DH}	t_{EHDX}	Data hold time	0			ns
t_{OEH}	t_{EHGL}	OE# hold from F-CE# high	10			ns
t_{RE}	-	Latency between Read and Write FFH or 71H	30			ns
t_{WS}	t_{WLEL}	Write enable set-up time	0			ns
t_{WH}	t_{EHWH}	Write enable hold time	0			ns
t_{CEP}	t_{ELEH}	F-CE# pulse width	60			ns
t_{CEPH}	t_{EHEL}	F-CE# pulse width high	30			ns
t_{BS}	$t_{FL/HWH}$	Byte enable high or low set-up time	50			ns
t_{BH}	$t_{WHFL/H}$	Byte enable high or low hold time	90			ns
t_{GHEL}	t_{GHEL}	OE# hold to F-CE# Low	90			ns
t_{BLS}	t_{PHHEH}	Block Lock set-up to write enable high	90			ns
t_{BLH}	t_{QVPH}	Block Lockhold from valid SRD	0			ns
t_{DAP}	t_{EHRH1}	Duration of auto-program operation		4	80	ms
t_{DAE}	t_{EHRH2}	Duration of auto-block erase operation		40	600	ms
t_{EHRL}	t_{EHRL}	F-CE# high to F-RY/BY# low			90	ns
t_{PS}	t_{PHWL}	F-RP# high recovery to write enable low	150			ns

Read timing parameters during command write operation mode are the same as during read-only operation mode.
Typical values at F-Vcc=3.3V, Ta=25°C

Erase and Program Performance

Parameter	Min	Typ	Max	Unit
Block Erase Time		40	600	ms
Main Block Write Time (Page Mode)		1.0	1.8	sec
Page Write Time		4	80	ms

Program Suspend Latency / Erase Suspend Time

Parameter	Min	Typ	Max	Unit
Program Suspend Latency			15	μs
Erase Suspend Time			15	μs

Please see page 19.

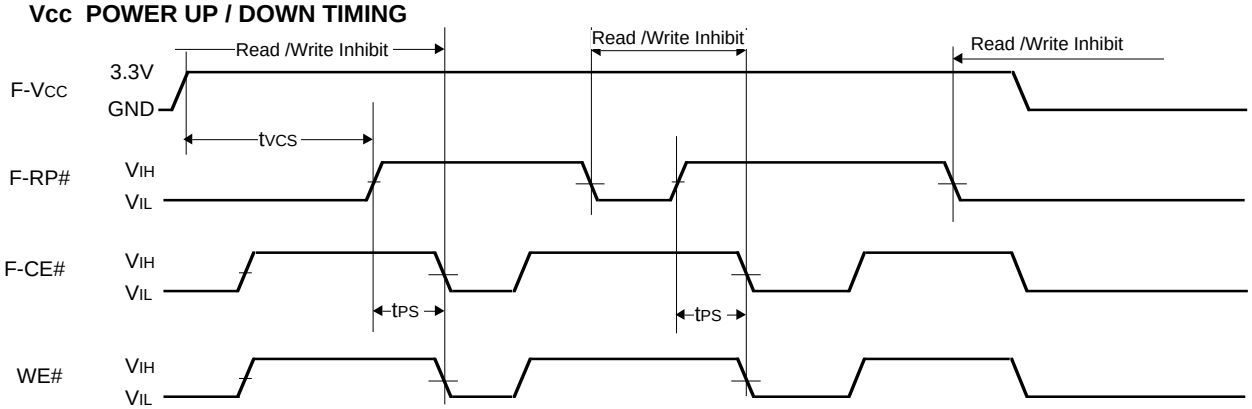
Vcc Power Up / Down Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{VCS}	RP# =V_{IH} set-up time from Vccmin	2			μs

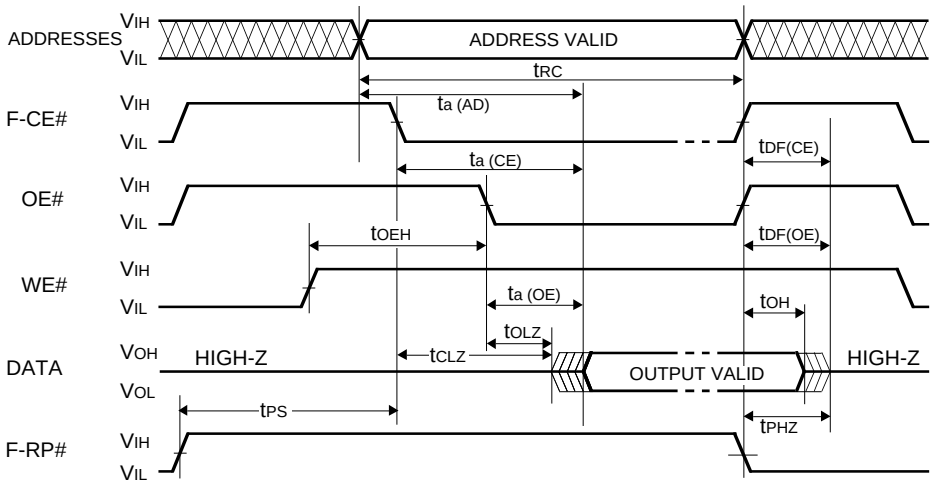
Please see page 12.

During power up/down, by the noise pulses on control pins, the device has possibility of accidental erasure or programming.
The device must be protected against initiation of write cycle for memory contents during power up/down.
The delay time of min.2μsec is always required before read operation or write operation is initiated from the time F-Vcc reaches F-Vccmin during power up/down.
By holding F-RP# VIL, the contents of memory is protected during F-Vcc power up/down.
During power up, F-RP# must be held VIL for min.2μs from the time F-Vcc reaches F-Vccmin.
During power down, F-RP# must be held VIL until Vcc reaches GND.
F-RP# doesn't have latch mode ,therefore F-RP# must be held VIH during read operation or erase/program operation.

Vcc POWER UP / DOWN TIMING



AC WAVEFORMS FOR READ OPERATION AND TEST CONDITIONS

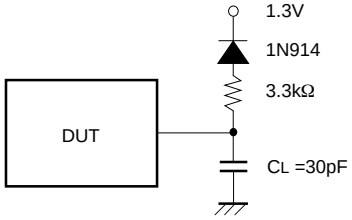


*: When BYTE#=V_{IL} , A_{-1} must be applied.

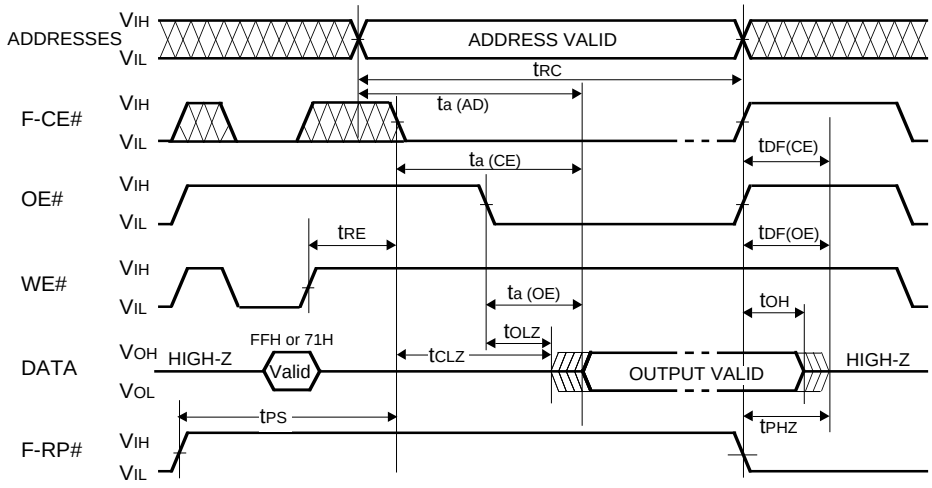
TEST CONDITIONS
FOR AC CHARACTERISTICS

Input voltage : V_{IL} = 0V, V_{IH} = 3.0V
Input rise and fall times : ≤5ns
Reference voltage
at timing measurement : 1.5V

Output load : 1TTL gate +
CL(30pF)
or

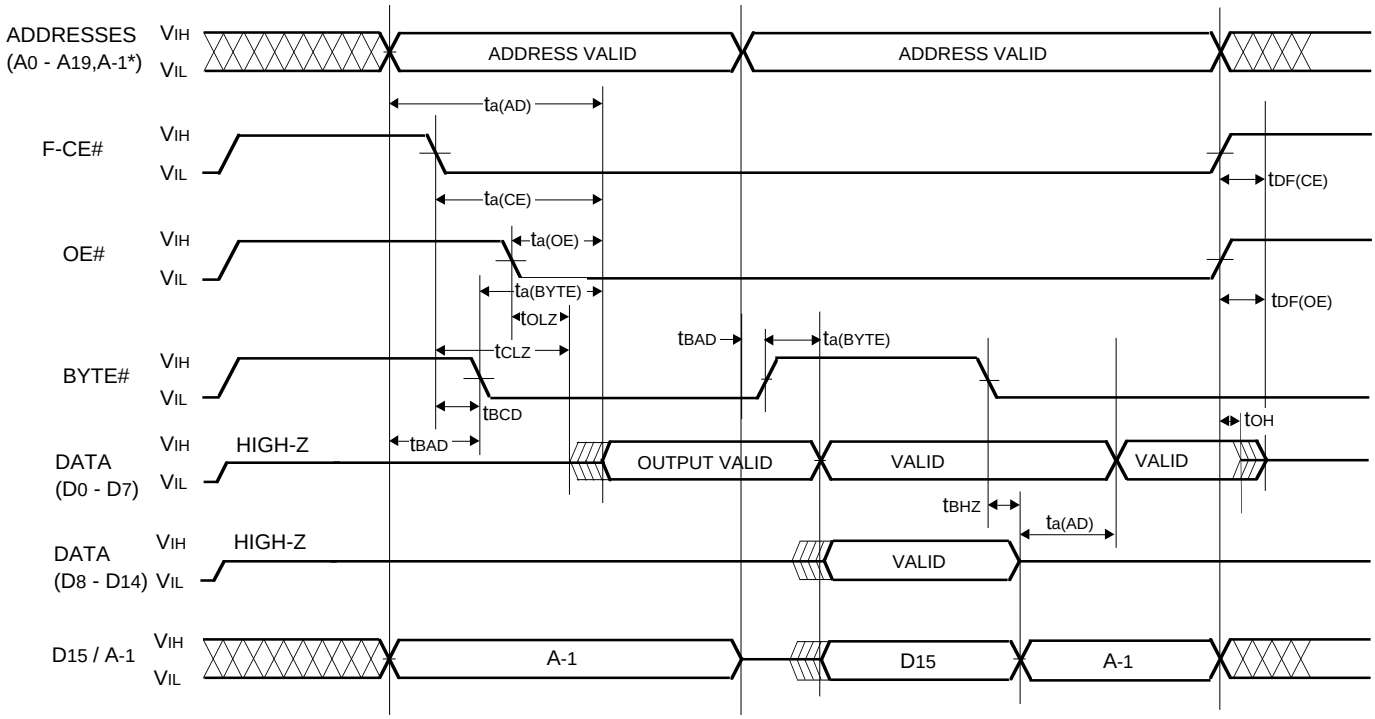


AC WAVEFORMS FOR WRITE FFH or 71H AND READ OPERATION



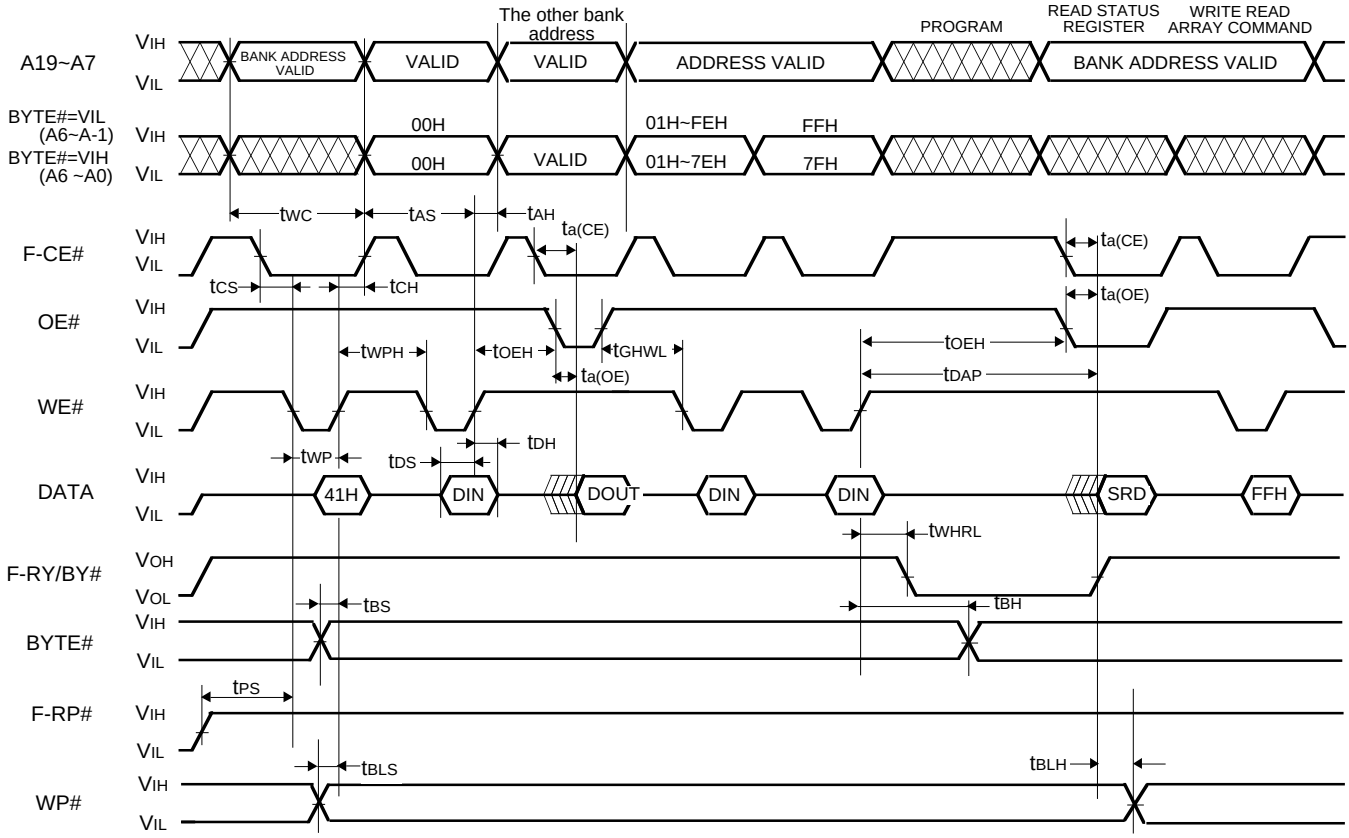
In the case of use F-CE# is Low fixed, it is allowed to define a timming specification of tRE from rising edge of WE# to falling edge of OE#, and valid data is read after spec of tRE+ta(CE). (This is only for FFH,71H program and read)

BYTE AC WAVEFORMS FOR READ OPERATION

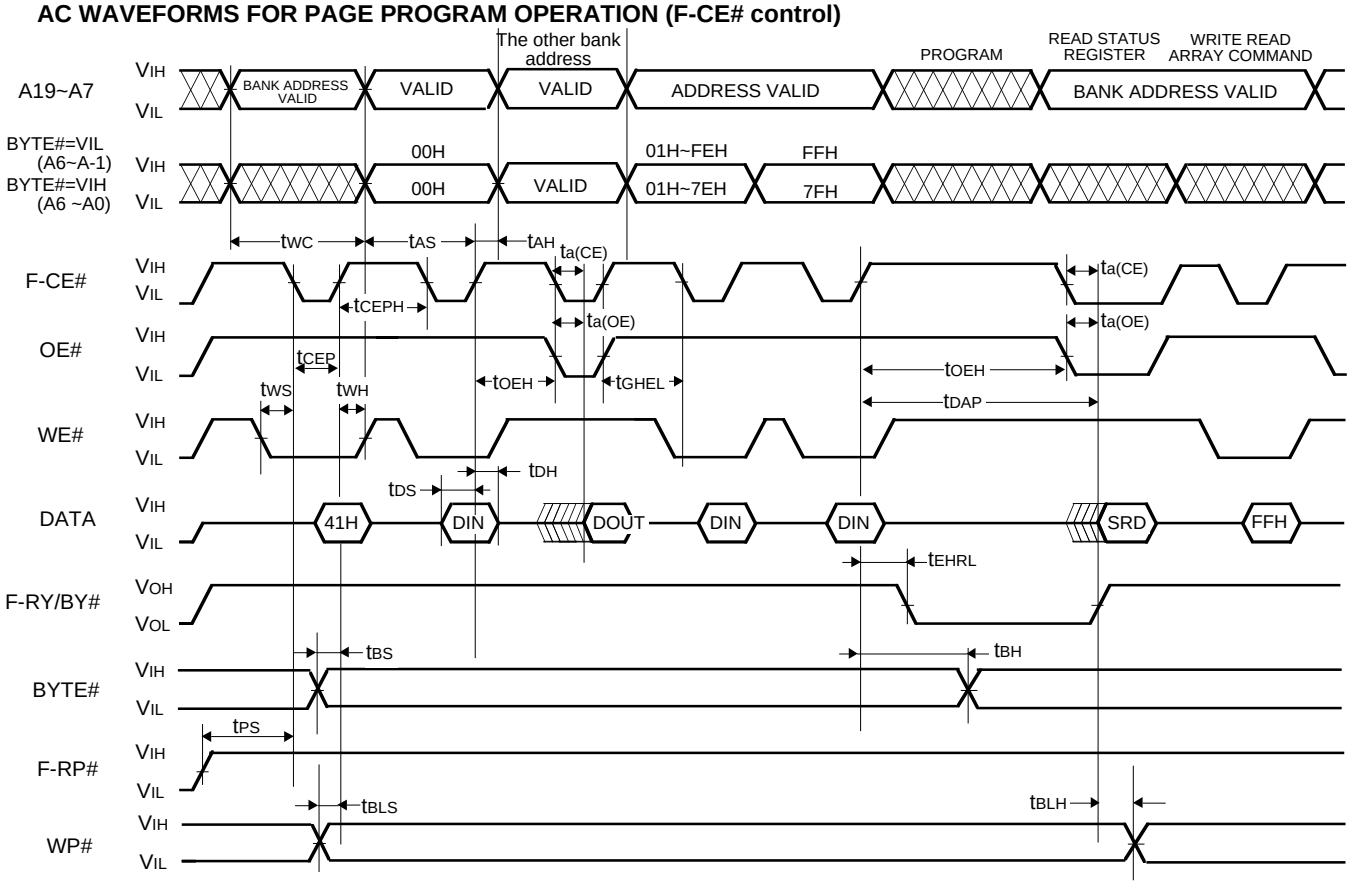


When BYTE#=V_{IH}, F-CE#=OE#=V_{IL} , D_{15}/A_{-1} is output status. At this time, input signal must not be applied.

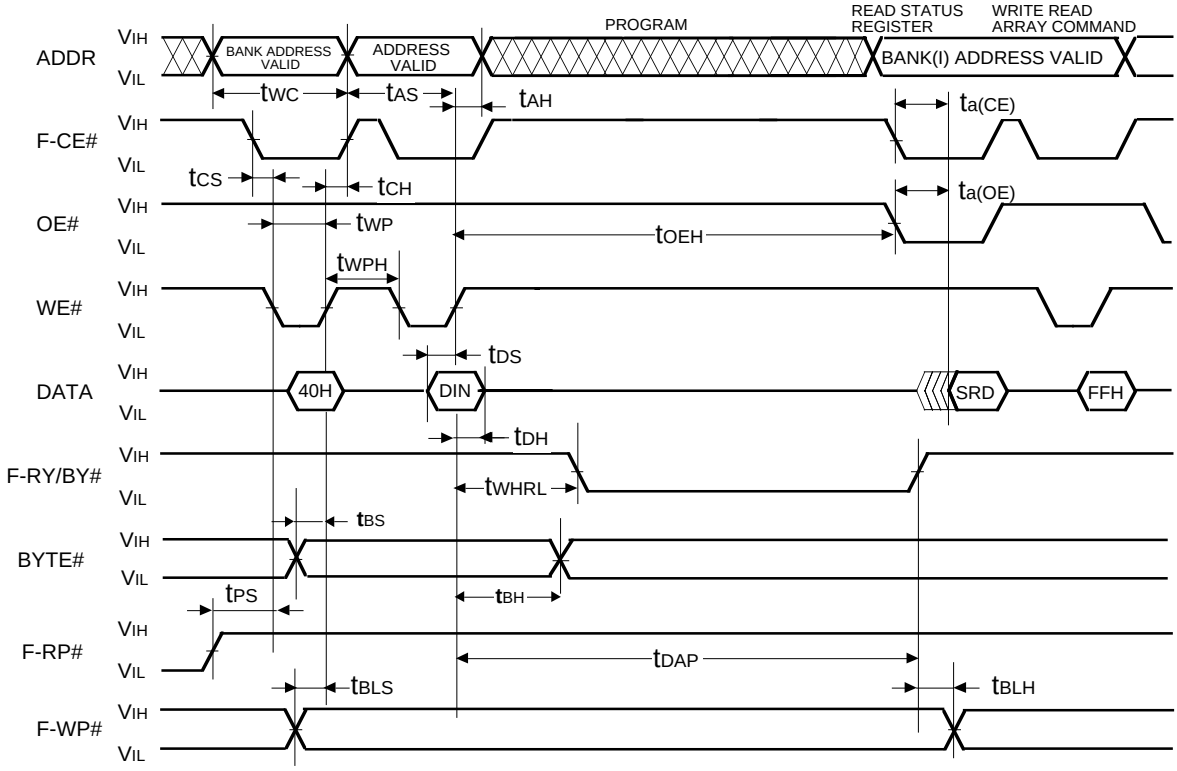
AC WAVEFORMS FOR PAGE PROGRAM OPERATION (WE# control)



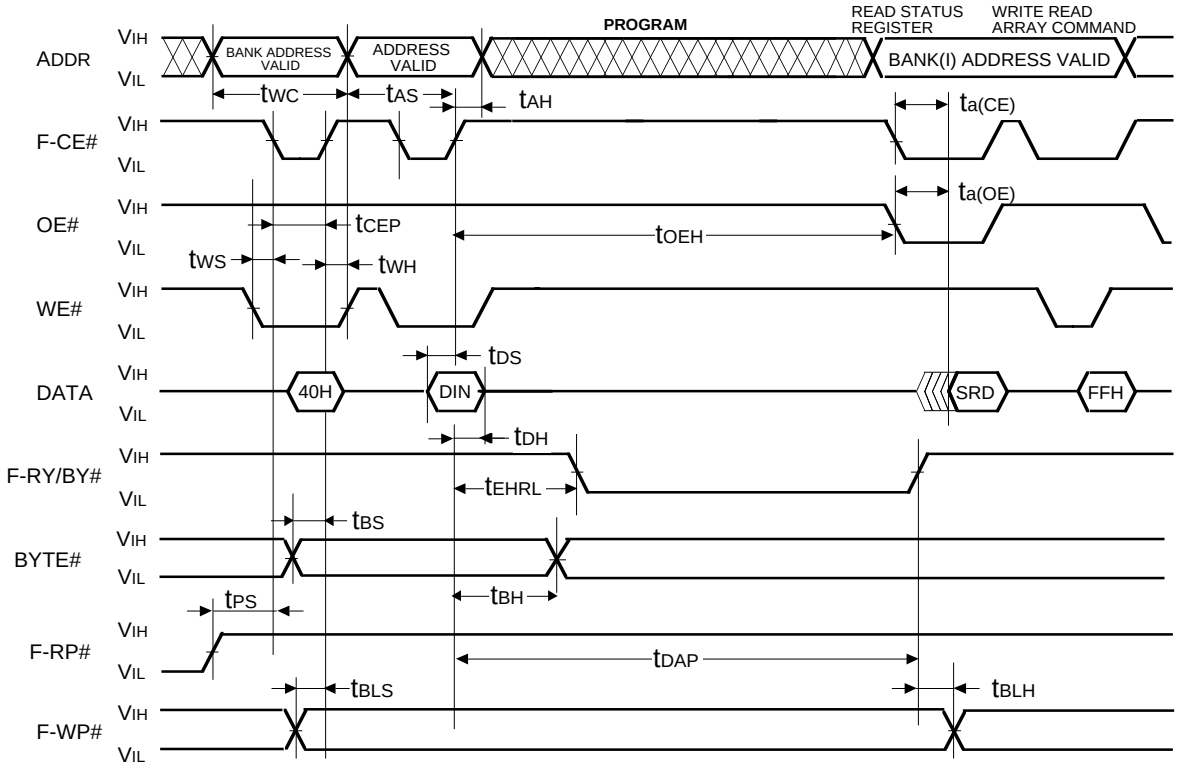
AC WAVEFORMS FOR PAGE PROGRAM OPERATION (F-CE# control)



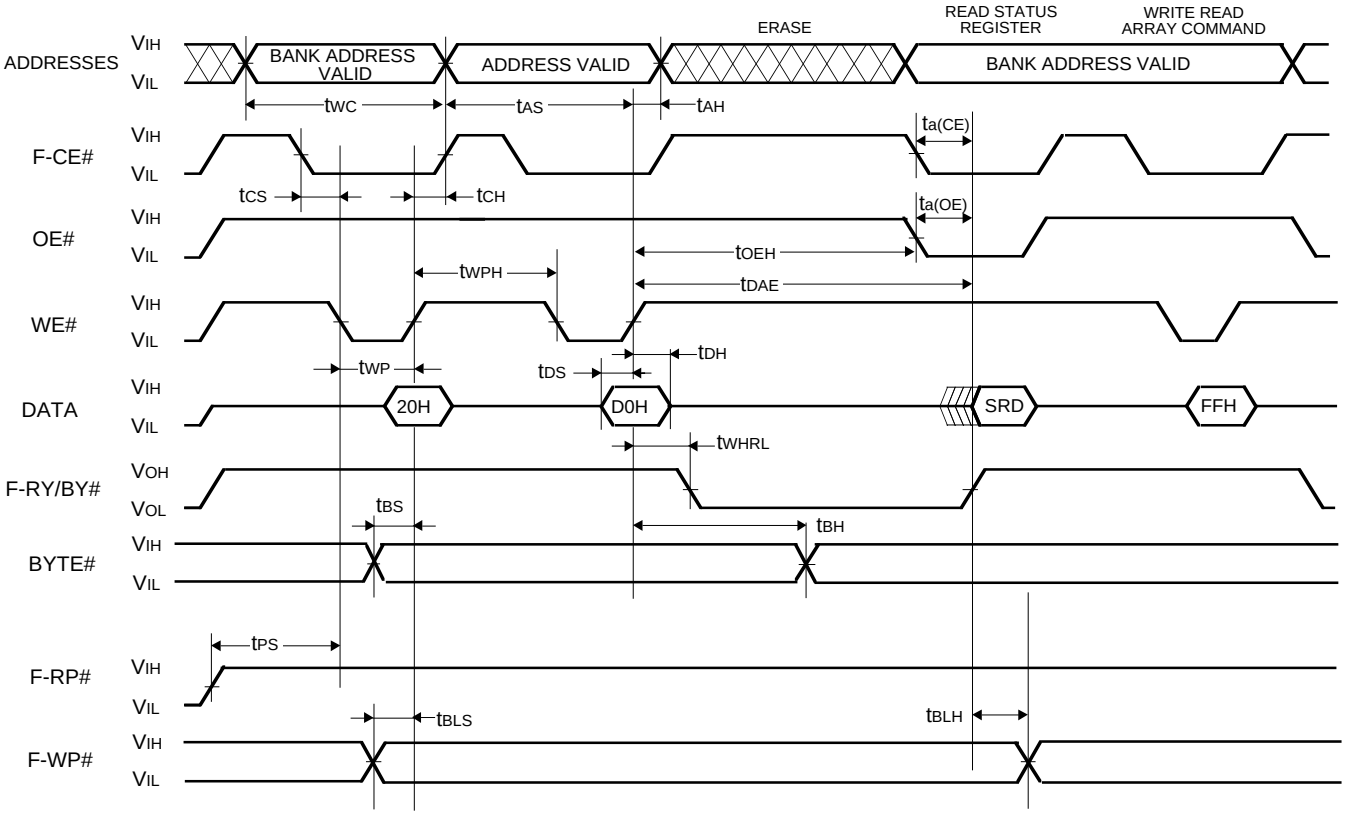
AC WAVEFORMS FOR BYTE / WORD PROGRAM OPERATION (WE# control) (to only BANK(I))



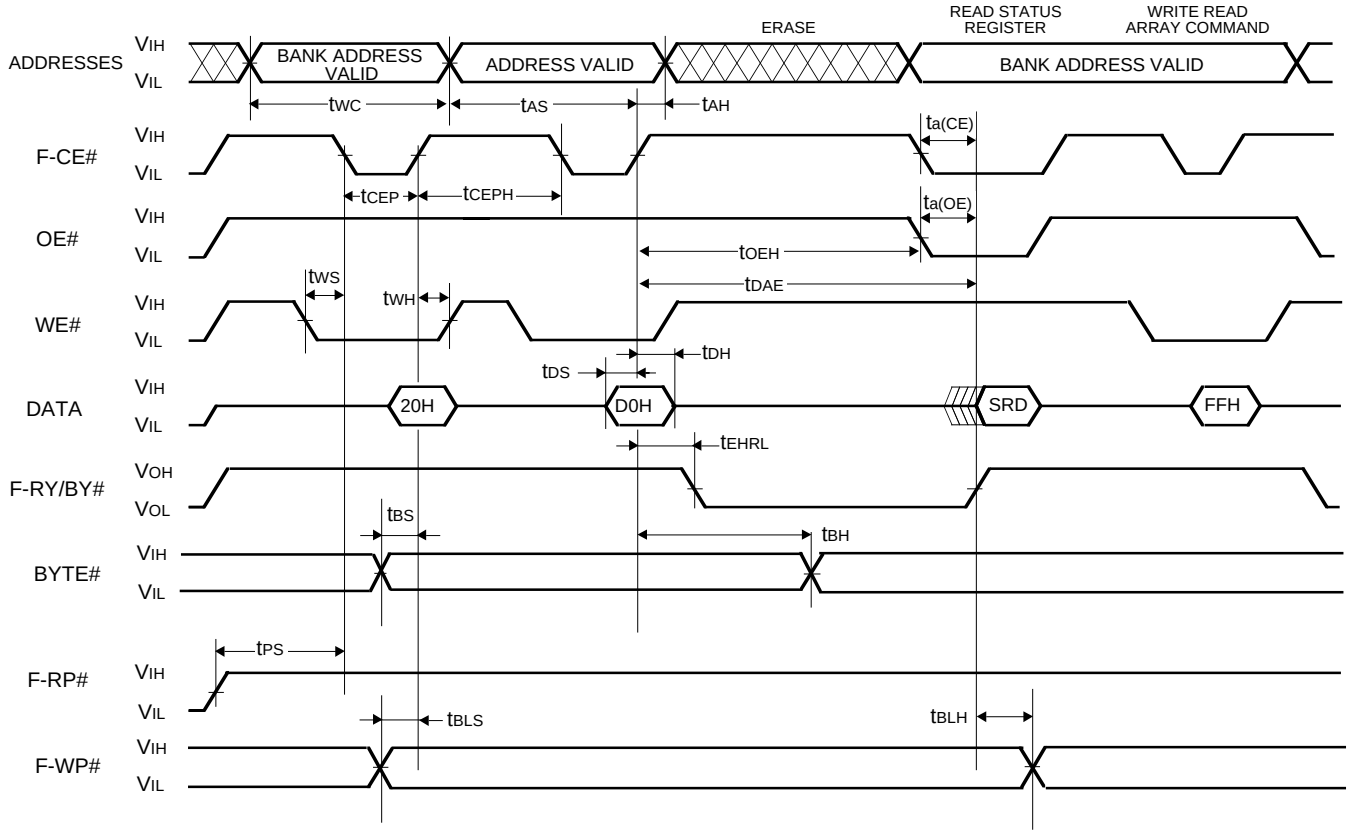
AC WAVEFORMS FOR BYTE / WORD PROGRAM OPERATION (F-CE# control) (to only BANK(I))



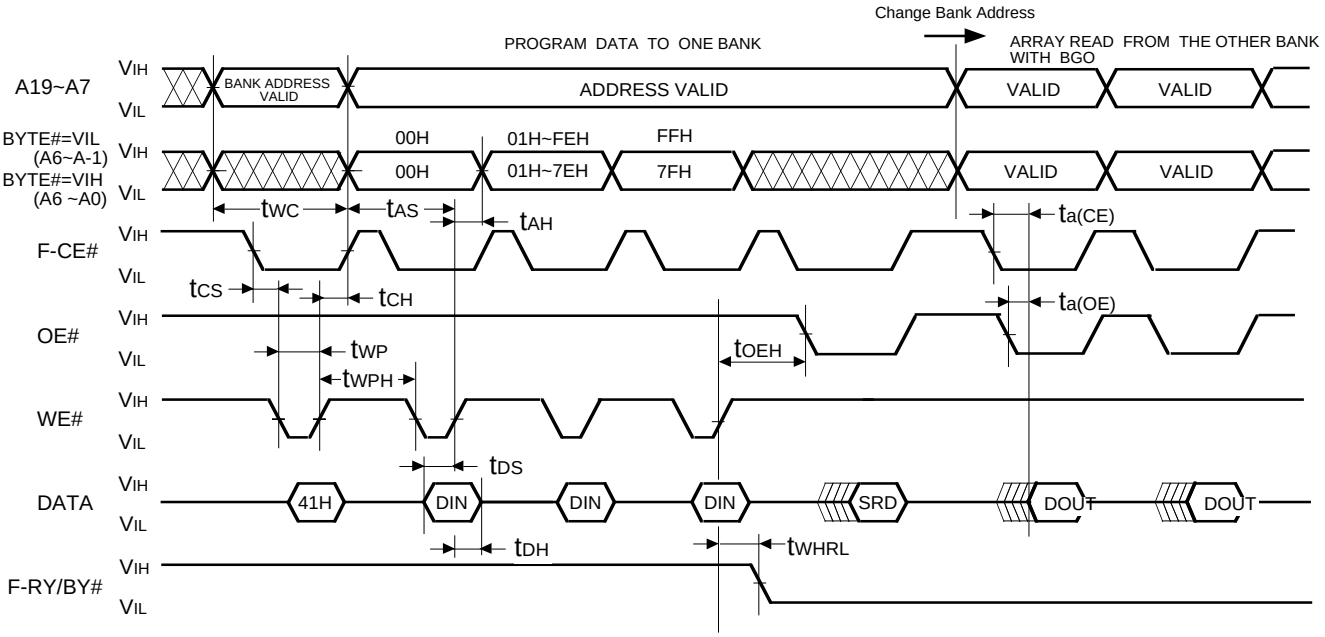
AC WAVEFORMS FOR ERASE OPERATIONS (WE# control)



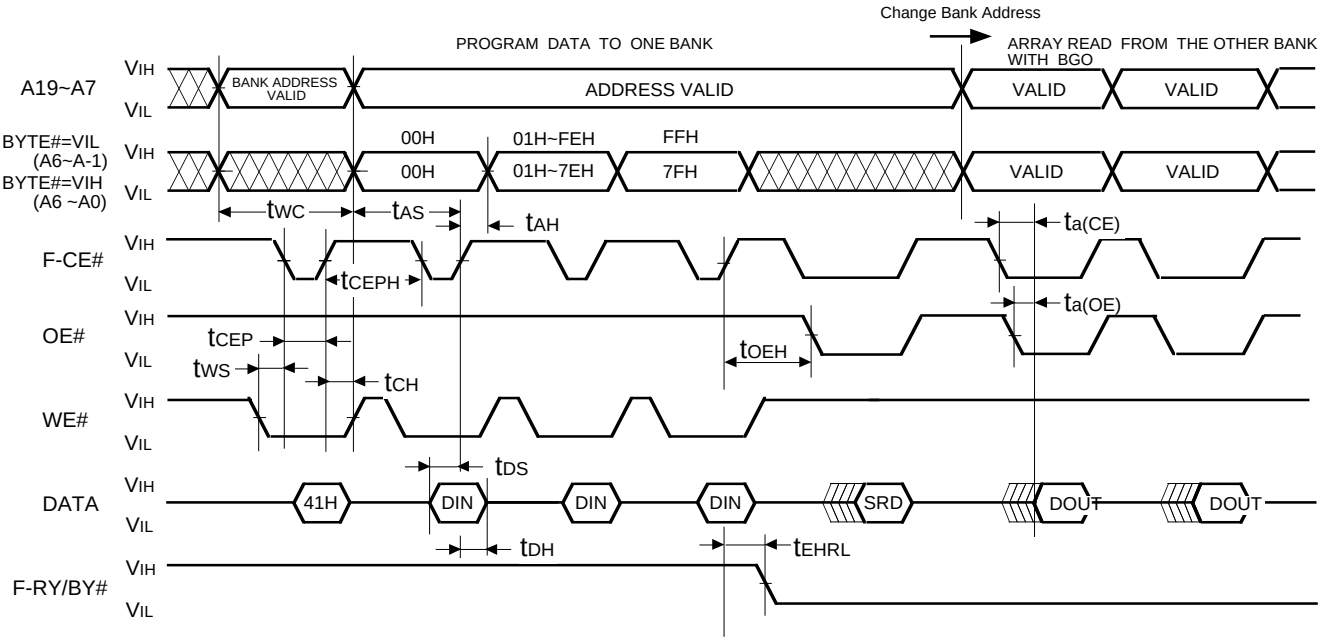
AC WAVEFORMS FOR ERASE OPERATIONS (F-CE# control)



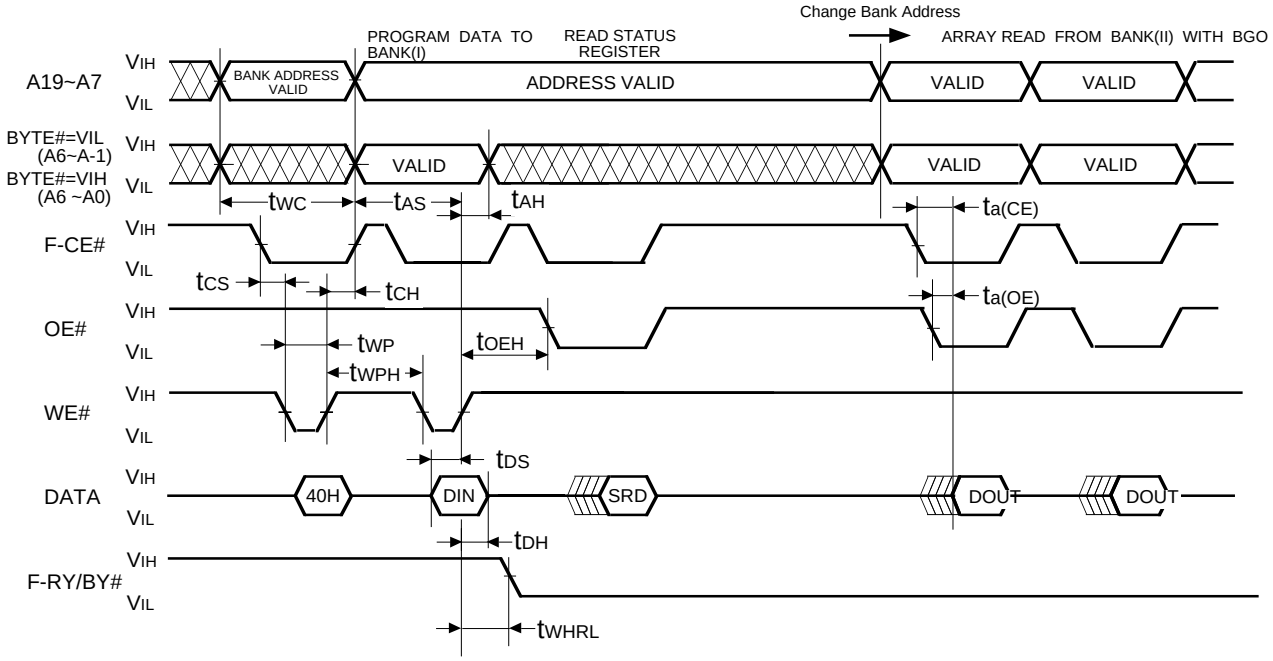
AC WAVEFORMS FOR PAGE PROGRAM OPERATION WITH BGO (WE# control)



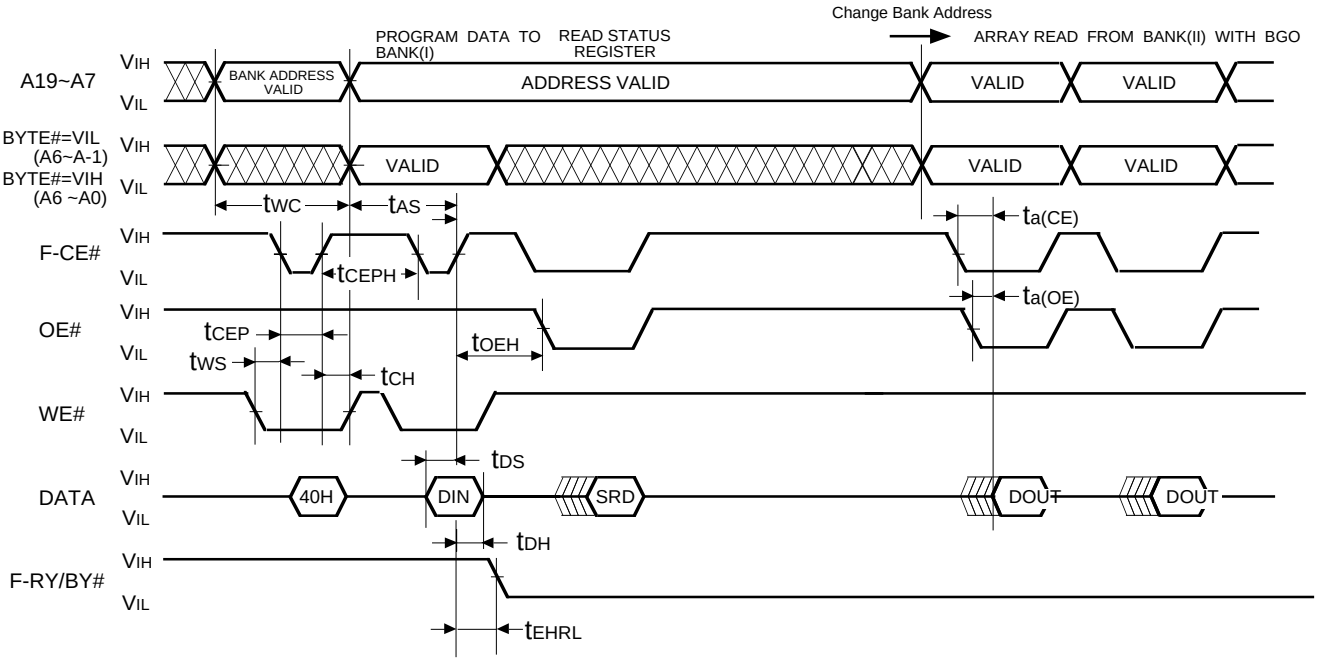
AC WAVEFORMS FOR PAGE PROGRAM OPERATION WITH BGO (F-CE# control)



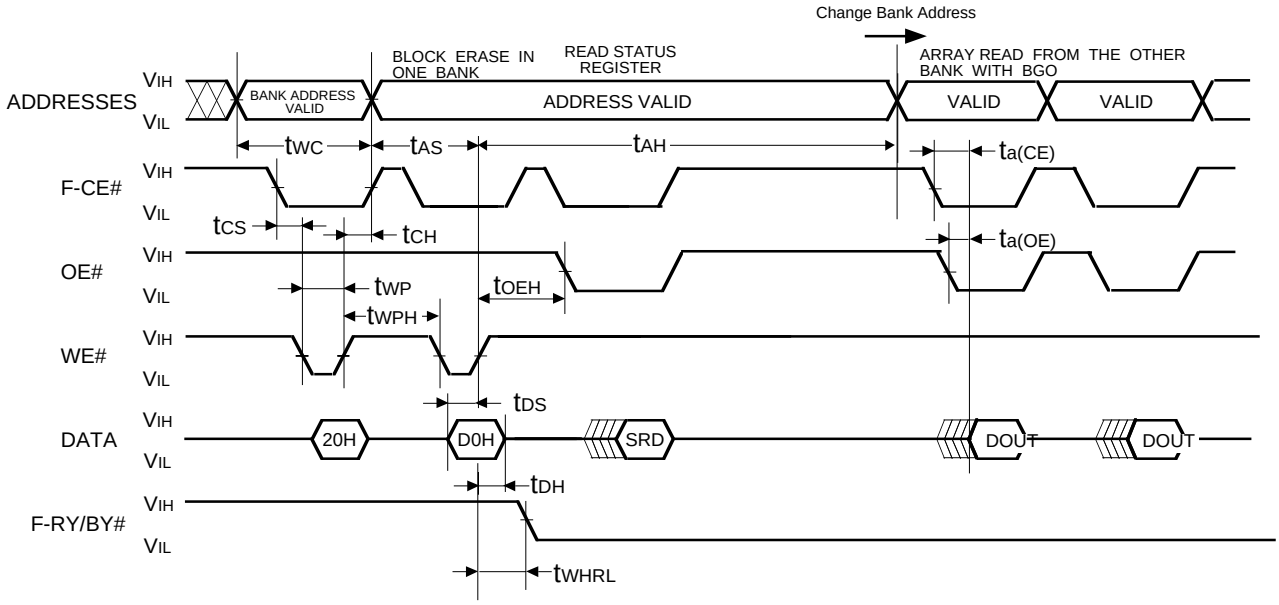
AC WAVEFORMS FOR BYTE / WORD PROGRAM OPERATION WITH BGO (WE# control)



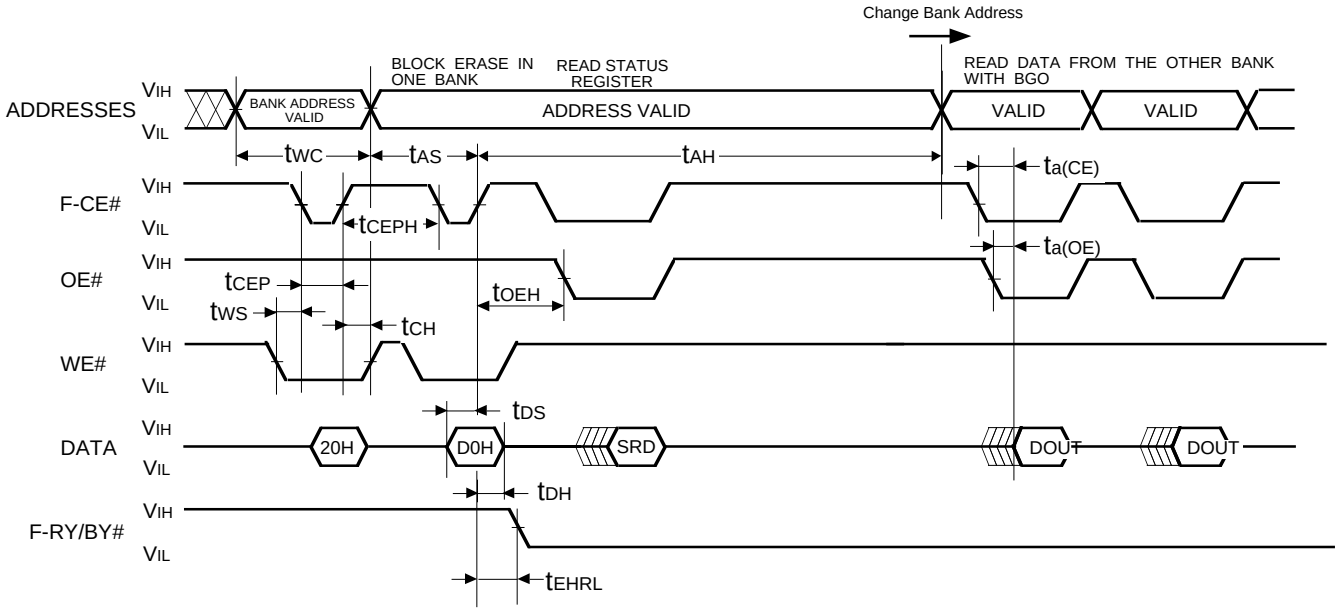
AC WAVEFORMS FOR BYTE / WORD PROGRAM OPERATION WITH BGO (F-CE# control)



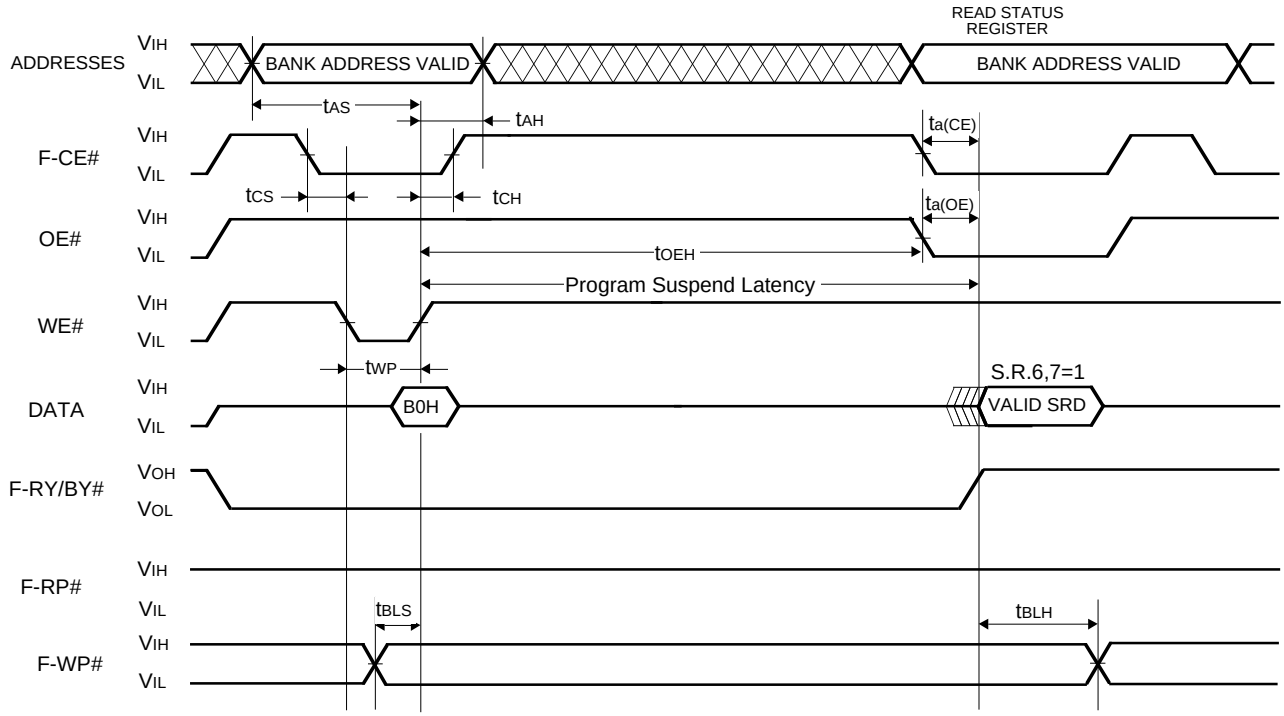
AC WAVEFORMS FOR BLOCK ERASE OPERATION WITH BGO (WE# control)



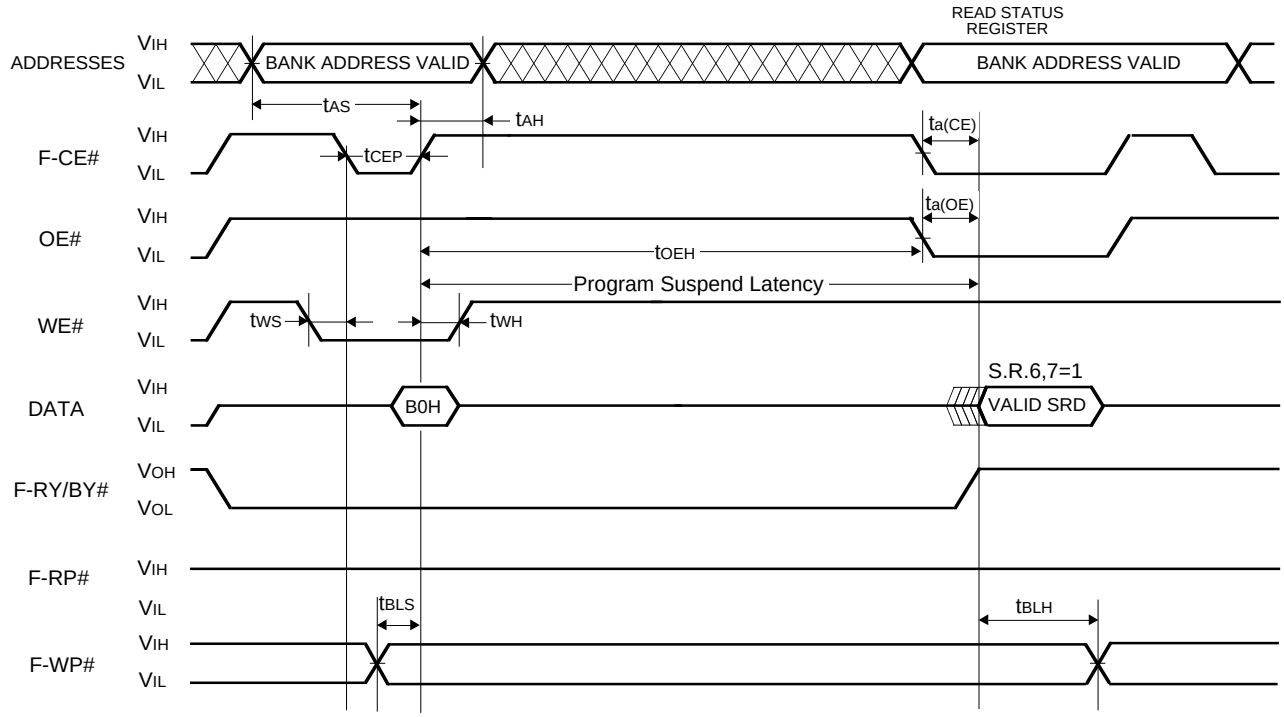
AC WAVEFORMS FOR BLOCK ERASE OPERATION WITH BGO (F-CE# control)



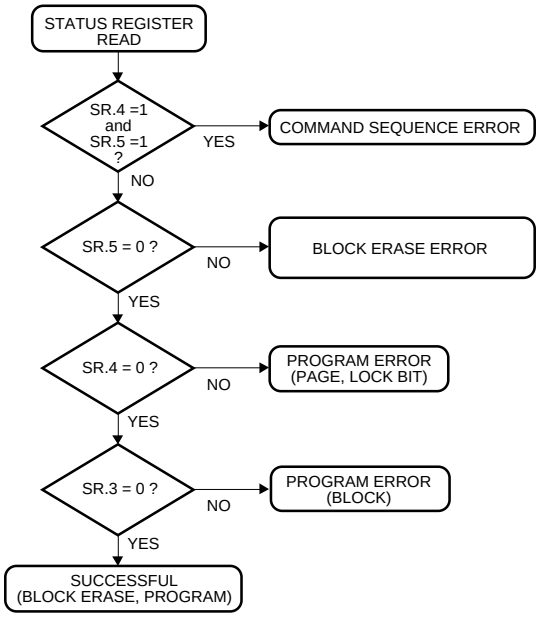
AC WAVEFORMS FOR SUSPEND OPERATION (WE# control)



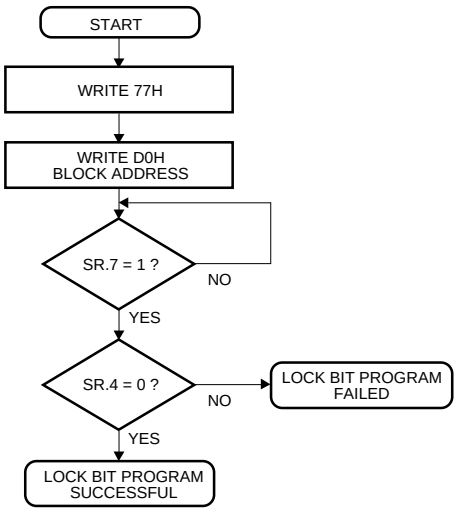
AC WAVEFORMS FOR SUSPEND OPERATION (F-CE# control)



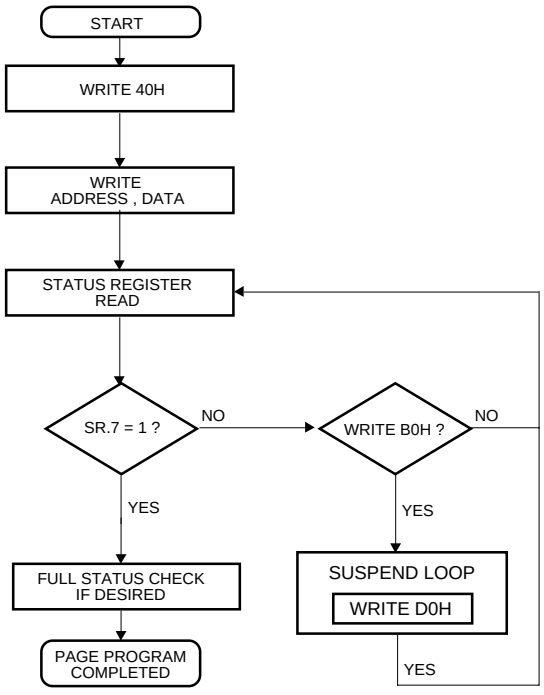
FULL STATUS CHECK PROCEDURE



LOCK BIT PROGRAM FLOW CHART

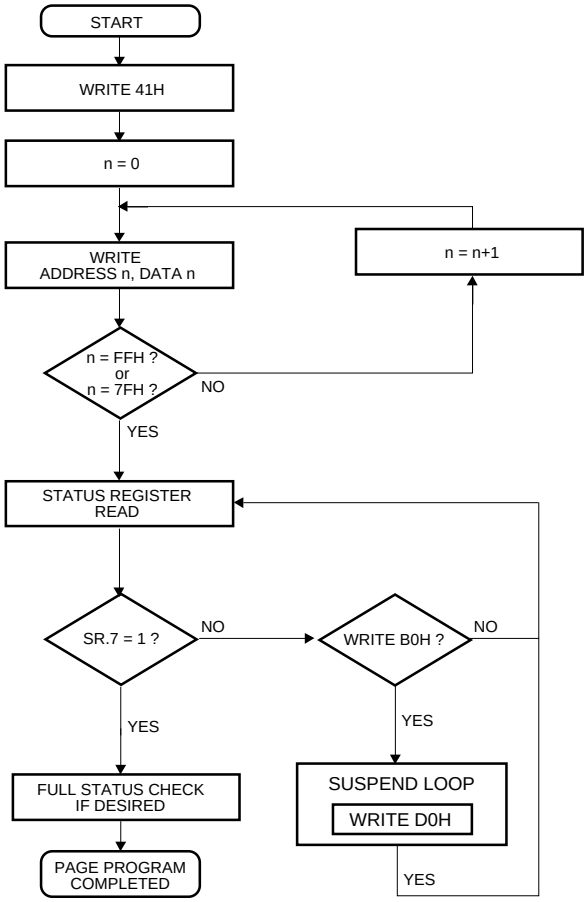


BYTE PROGRAM FLOW CHART

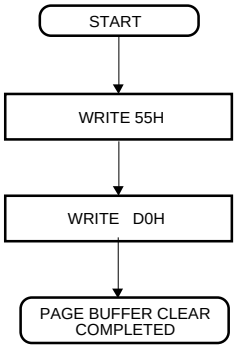


* Byte/Word program is admitted to only BANK(I).

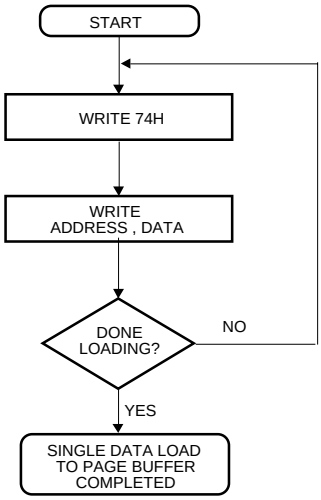
PAGE PROGRAM FLOW CHART



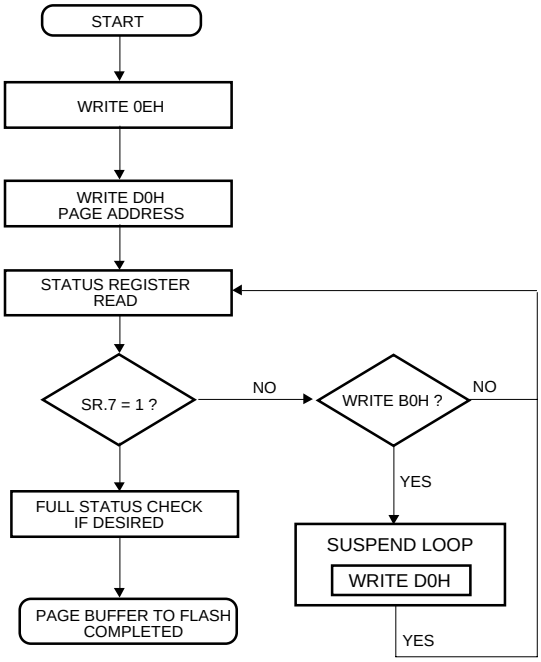
CLEAR PAGE BUFFER



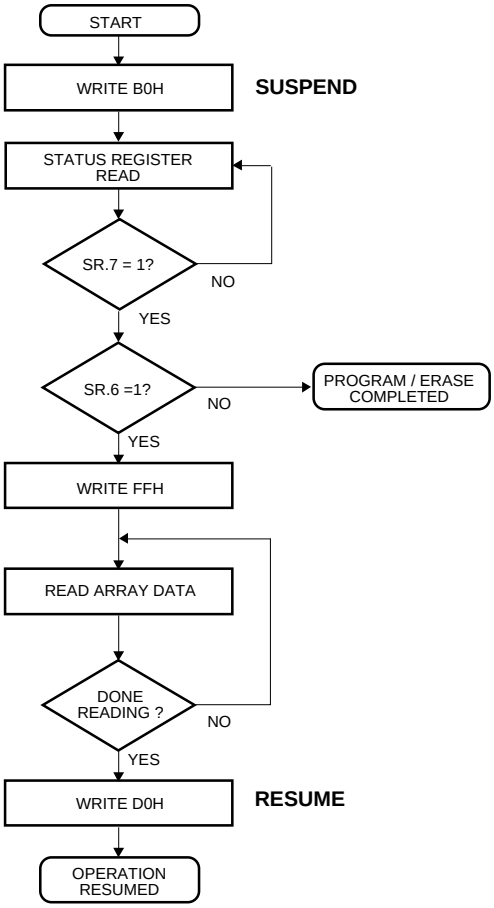
SINGLE DATA LOAD TO PAGE BUFFER



PAGE BUFFER TO FLASH

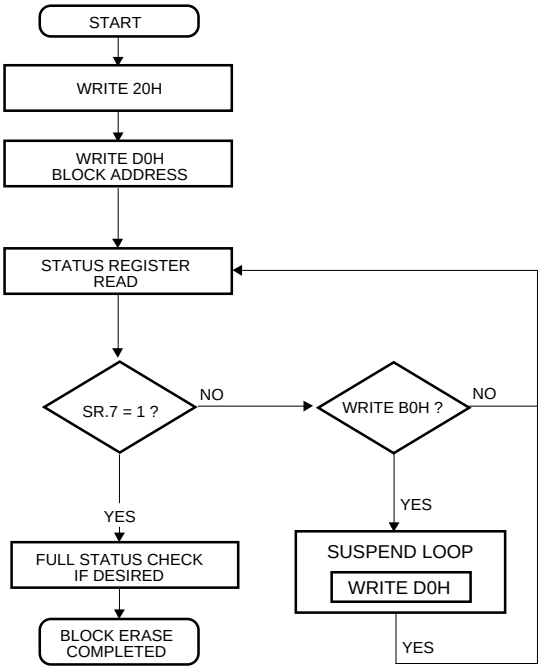


SUSPEND / RESUME FLOW CHART

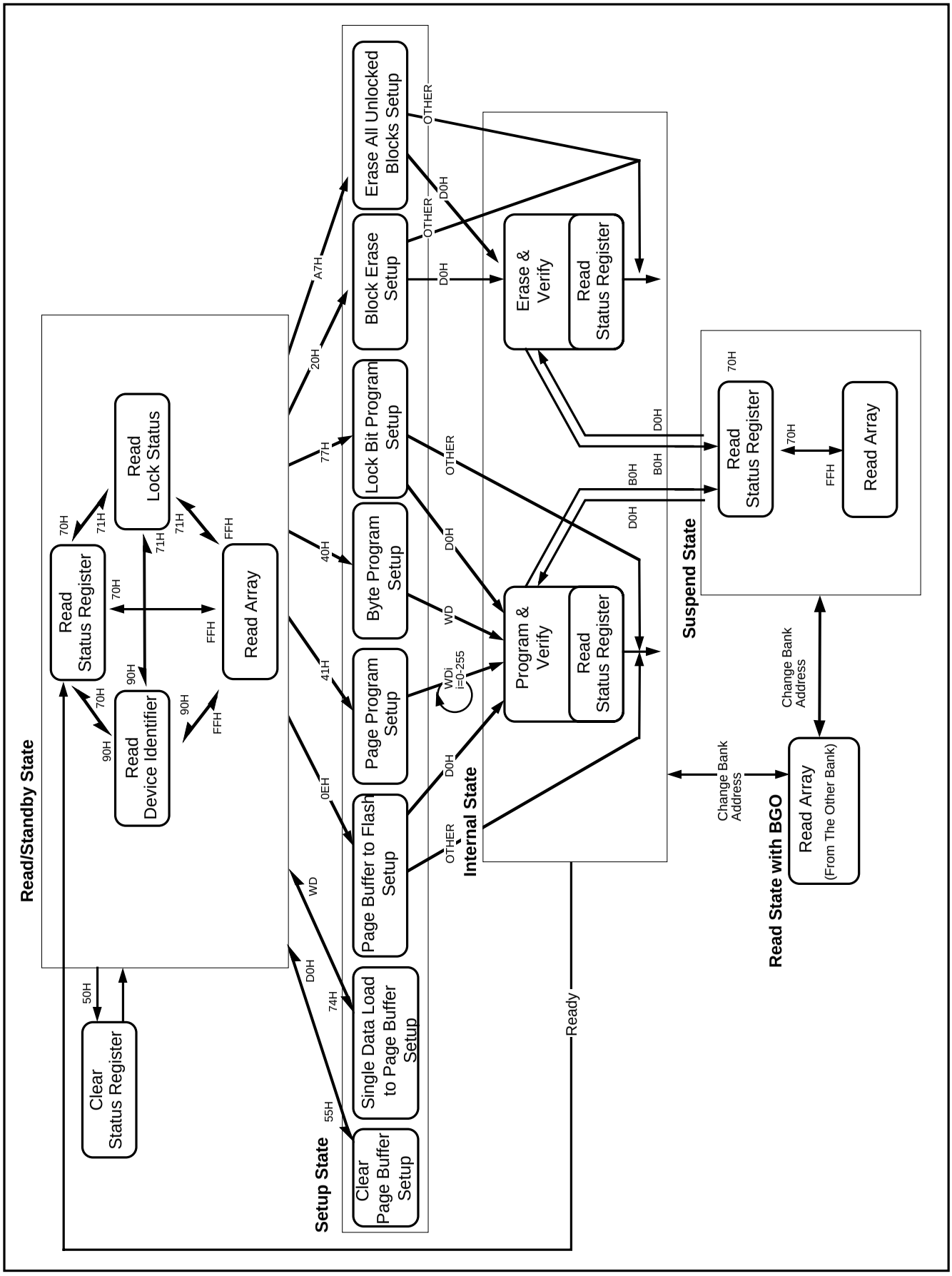


* The bank address is required when writing this command. Also, there is no need to suspend the erase or program operation when reading data from the other bank. Please use BGO function.

BLOCK ERASE FLOW CHART



OPERATION STATUS and EFFECTIVE COMMAND



2. SRAM

The SRAM of M6MGB/T160S2BVP is organized as 131,072-word by 16-bit/ 262,144-byte by 8-bit. These devices operate on a single +2.7~3.6V powersupply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

The operation mode are determined by a combination of the device control inputs BYTE#, S-CE , WE# and OE#. Each mode is summarized in the function table.

A write operation is executed whenever the low level WE# overlaps with the high level S-CE. The address(A-1~A16:byte mode, A0~A16:word mode) must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting WE# at a high level and OE# at a low level while S-CE are in an active state(S-CE=H).

When setting BYTE# at the low level and other pins are in anactive stage , lower-byte I/O are in a selesctable mode in whichboth reading and writing are enabled, and upper-byte are in anon-selectable mode.

When setting S-CE at a low level,the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in ahigh-impedance state, allowing OR-tie with other chips and memory expansion by S-CE.

The power supply current is reduced as low as 0.3μA(25 ˚C,typical), and the memory data can be held at +2V powersupply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

S-CE	BYTE#	WE#	OE#	Mode	DQ0~7	DQ8~15	Icc
L	X	X	X	Non selection	High-Z	High-Z	Standby
H	H	L	X	Write	Din	Din	Active
H	H	H	L	Read	Dout	Dout	Active
H	H	H	H	———	High-Z	High-Z	Active
H	L	L	X	Write	Din	High-Z	Active
H	L	H	L	Read	Dout	High-Z	Active
H	L	H	H	———	High-Z	High-Z	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
S-Vcc	Supply voltage	With respect to GND	-0.5* ~ +4.6	V
V_I	Input voltage	With respect to GND	-0.5* ~ S-Vcc + 0.5	
V_O	Output voltage	With respect to GND	0 ~ S-Vcc	
P_d	Power dissipation	Ta=25°C	700	mW
T_a	Operating temperature	W-version	- 20 ~ +85	°C
T_{stg}	Storage temperature		- 65 ~ +150	°C

* -3.0V in case of AC (Pulse width≦ 30ns)

DC ELECTRICAL CHARACTERISTICS

(S-Vcc=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Units
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.0		S-Vcc+0.3V	V
V_{IL}	Low-level input voltage			-0.3 *		0.6	
V_{OH1}	High-level output voltage 1	I_{OH}= -0.5mA		2.4			
V_{OH2}	High-level output voltage 2	I_{OH}= -0.05mA		S-Vcc-0.5V			
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4	
I_I	Input leakage current	V_I =0 ~ S-Vcc				±1	µA
I_O	Output leakage current	S-CE=V_{IL} or OE#=V_{IH}, $V_{I/O}$=0 ~ S-Vcc				±1	
Icc1	Active supply current (AC,MOS level)	S-CE ≧S-Vcc-0.2V other inputs ≦ 0.2V or ≧ S-Vcc-0.2V Output - open (duty 100%)	f= 10MHz	-	45	60	mA
			f= 1MHz	-	5	15	
Icc2	Active supply current (AC,TTL level)	S-CE=V_{IH} other pins =V_{IH} or V_{IL} Output - open (duty 100%)	f= 10MHz	-	45	60	
			f= 1MHz	-	5	15	
Icc3	Stand by supply current (AC,MOS level)	S-CE ≦ 0.2V Other inputs=0~S-Vcc	-W, +70 ~ +85°C	-	-	30	µA
			-W, +40 ~ +70°C	-	-	10	
			-W, +25 ~ +40°C	-	1	5	
			-W, - 20 ~ +25°C	-	0.3	2	
Icc4	Stand by supply current (AC,TTL level)	S-CE=V_{IL} Other inputs= 0 ~ S-Vcc		-	-	0.5	mA

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

Note 2: Typical value is for S-Vcc=3.0V and Ta=25° C

* -3.0V in case of AC (Pulse width≦ 30ns)

CAPACITANCE

(S-Vcc=2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			8	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			10	

Note: The value of common pins to SRAM is the sum of Flash Memory and SRAM.

AC ELECTRICAL CHARACTERISTICS (S-Vcc=2.7 ~ 3.6V, unless otherwise noted)

(1) TEST CONDITIONS

Supply voltage	2.7V~3.6V
Input pulse	V_{IH}=2.2V,V_{IL}=0.4V
Input rise time and fall time	5ns
Reference level	V_{OH}=V_{OL}=1.5V Transition is measured ±500mV from steady state voltage.(for t_{en},t_{dis})
Output loads	Fig.1,CL=30pF CL=5pF (for ten,tdis)

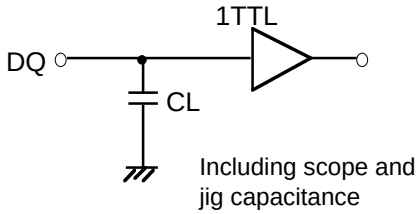


Fig.1 Output load

(2) READ CYCLE

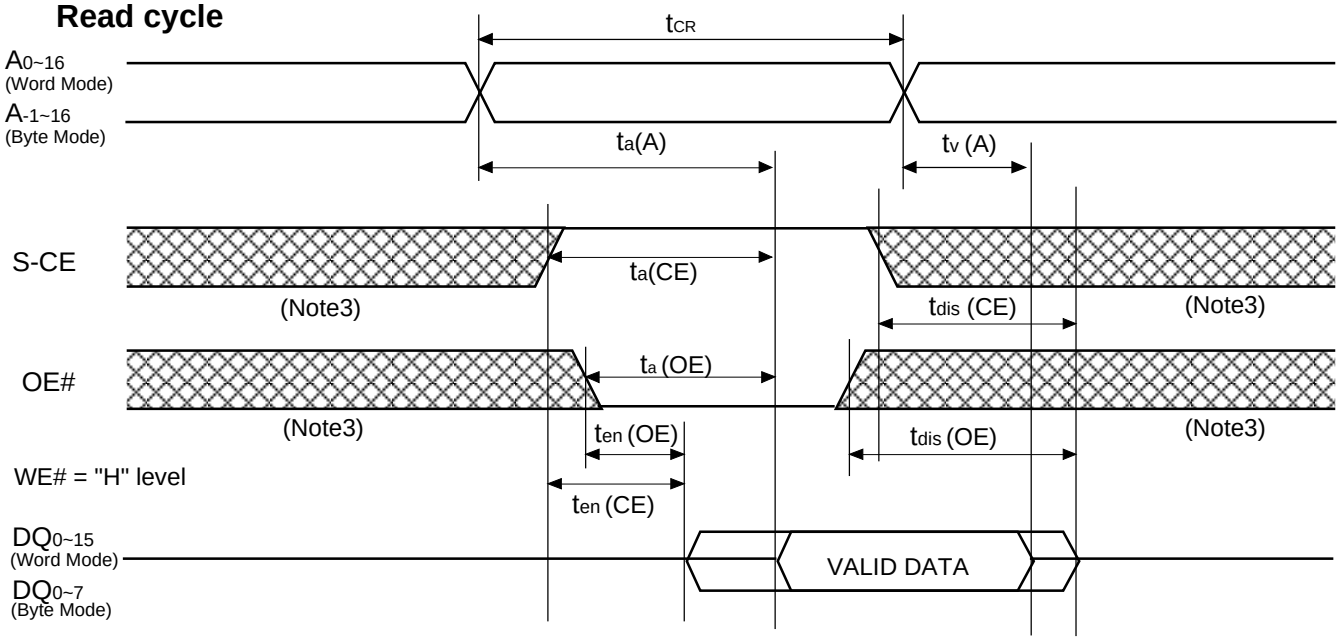
Symbol	Parameter	Limits SRAM Min	Limits SRAM Max	Units
t_{CR}	Read cycle time	85		ns
t_a(A)	Address access time		85	ns
t_a(CE)	Chip select access time		85	ns
t_a(OE)	Output enable access time		45	ns
t_{dis}(CE)	Output disable time after S-CE low		30	ns
t_{dis}(OE)	Output disable time after OE# high		30	ns
t_{en}(CE)	Output enable time after S-CE high	10		ns
t_{en}(OE)	Output enable time after OE# low	5		ns
t_V(A)	Data valid time after address	10		ns

(3) WRITE CYCLE

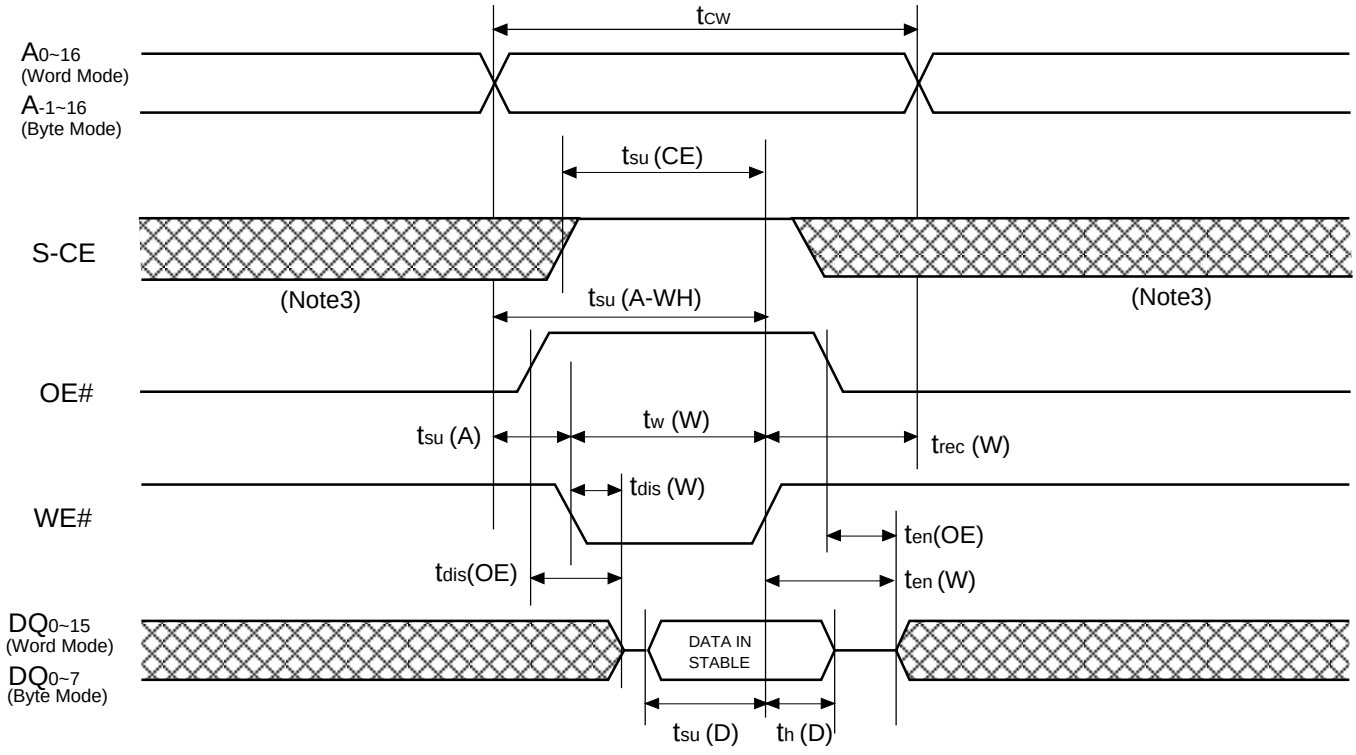
Symbol	Parameter	Limits SRAM Min	Limits SRAM Max	Units
t_{CW}	Write cycle time	85		ns
t_w(W)	Write pulse width	60		ns
t_{su}(A)	Address setup time	0		ns
t_{su}(A-WH)	Address setup time with respect to WE#	70		ns
t_{su}(CE)	Chip select setup time	70		ns
t_{su}(D)	Data setup time	35		ns
t_h(D)	Data hold time	0		ns
t_{rec}(W)	Write recovery time	0		ns
t_{dis}(W)	Output disable time from WE# low		30	ns
t_{dis}(OE)	Output disable time from OE# high		30	ns
t_{en}(W)	Output enable time from WE# high	5		ns
t_{en}(OE)	Output enable time from OE# low	5		ns

(4)TIMING DIAGRAMS

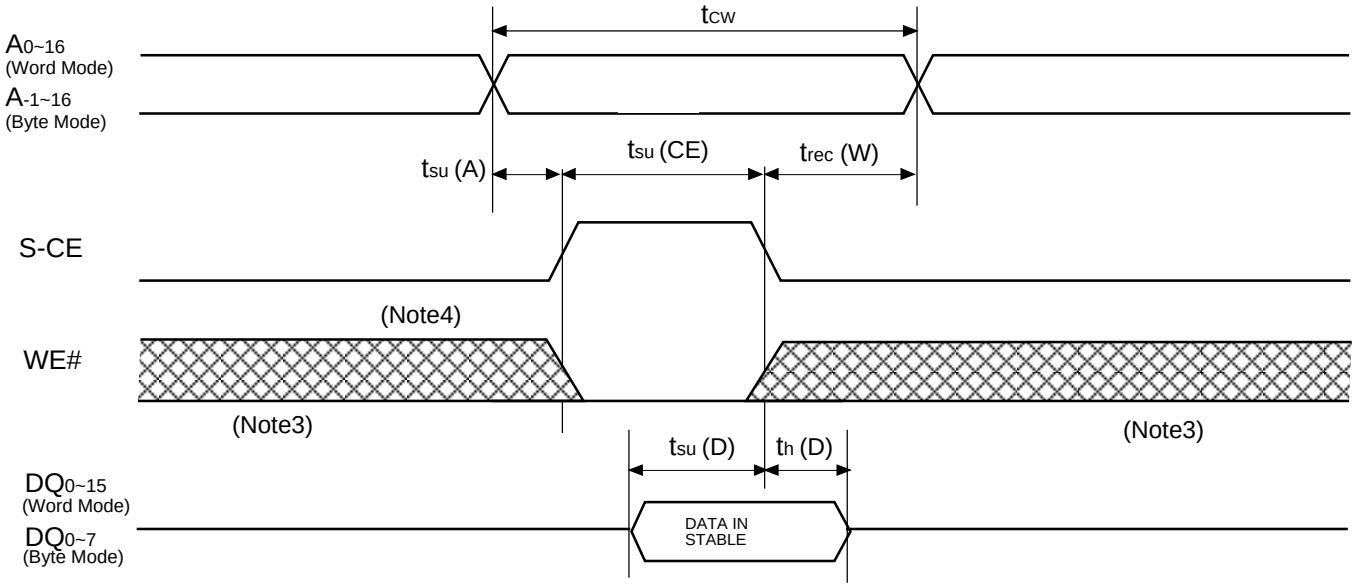
Read cycle



Write cycle (WE# control mode)



Write cycle (S-CE control mode)



Note 3: Hatching indicates the state is "don't care".

Note 4: When the falling edge of WE# is simultaneously or priorto the rising edge of S- CE, the outputs are maintained in the high impedance state.

Note 5: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions			Limits			Units
					Min	Typ	Max	
S-Vcc (PD)	Power down supply voltage				2.0			V
VI (CE)	Chip select input S-CE						0.2	V
Icc (PD)	Power down supply current	S-Vcc=3.0V S-CE≦0.2V other inputs=0~3V	-W	+70 ~ +85°C	-	-	24	μA
				+40 ~ +70°C	-	-	8	μA
				+25 ~ +40°C	-	1	3	μA
				-20 ~ +25°C	-	0.3	1	μA

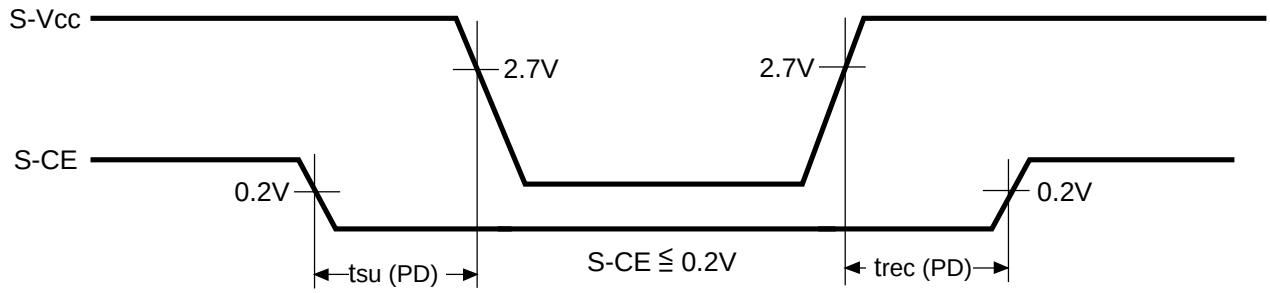
Typical value is for Ta=25°C

(2) TIMING REQUIREMINTS

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		5			ms

(3) TIMING DIAGRAM

S-CE control mode



BYTE# TIMING DIAGRAM

(1) TIMING REQUIREMINTS

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
$t_{su\ (BYTE)}$	BYTE# set up time		5			ms
$t_{rec\ (BYTE)}$	BYTE# recovery time		5			ms

(2) TIMING DIAGRAM