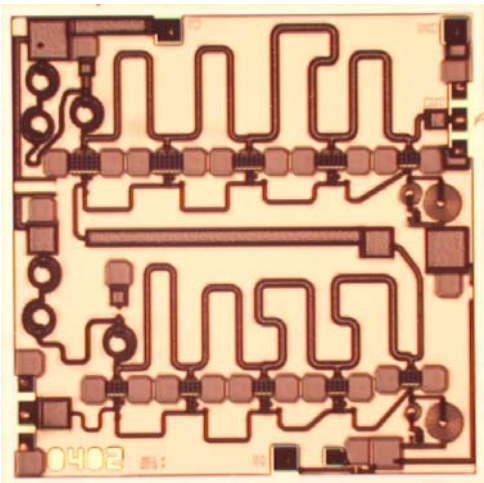
Amplifier, Distributed Power 4.0—18.0 GHz

MAAPGM0052-DIE
903210 —
Preliminary Information

Features

- **0.5 Watt Saturated Output Power Level**
- **Variable Drain Voltage (5-10V) Operation**
- **GaAs MSAG™ Process**
- **Proven Manufacturability and Reliability**
  - **No Airbridges**
  - **Polyimide Scratch Protection**
  - **No Hydrogen Poisoning Susceptibility**



Primary Applications

Description

The MAAPGM0052-Die is a 2-stage distributed power amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG™) Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Electrical Characteristics: T_B = 40°C[1], Z_0 = 50Ω, V_{DD} = 8V, I_{DQ} ≈ 500 mA[2], P_{in} = 17 dBm, Rg ≈ 100Ω

Parameter	Symbol	Typical	Units
Bandwidth	f	4.0-18.0	GHz
Output Power	P_{OUT}	26.0	dBm
1dB Compression Point	P1dB	25	dBm
Small Signal Gain	G	13	dB
Noise Figure	NF	6.0	dB
Input VSWR	VSWR	1.4:1	
Output VSWR	VSWR	1.5:1	
Gate Supply Current	I_{GG}	4	mA
Drain Supply Current	I_{DD}	600	mA

1. **T_B = MMIC Base Temperature**
2. **Adjust V_{GG} between –2.4 and –1.0V to achieve I_{DQ} indicated.**

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Maximum Operating Conditions [3]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	22.0	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF, 40% Idss)	I_{DQ}	630	mA
Quiescent DC Power Dissipated (No RF)	P_{DISS}	4.8	W
Junction Temperature	T_J	180	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Die Attach Temperature		310	°C

3. Operation outside of these ranges may reduce product reliability. Operation at other than the typical values may result in performance outside the guaranteed limits.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	V_{DD}	4.0	8.0	10.0	V
Gate Supply Voltage	V_{GG}	-2.4	-1.8	-1.0	V
Input Power	P_{IN}		17.0	20.0	dBm
Junction Temperature	T_J			150	°C
Thermal Resistance	Θ_{JC}		18.6		°C/W
MMIC Base Temperature	T_B			Note 4	°C

4. Maximum MMIC Base Temperature = 150°C —Θ_{JC}* V_{DD} * I_{DQ}

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -2 V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 8 V.
3. Adjust V_{GG} to set I_{DQ}.
4. Set RF input.
5. Power down sequence in reverse. Turn V_{GG} off last.

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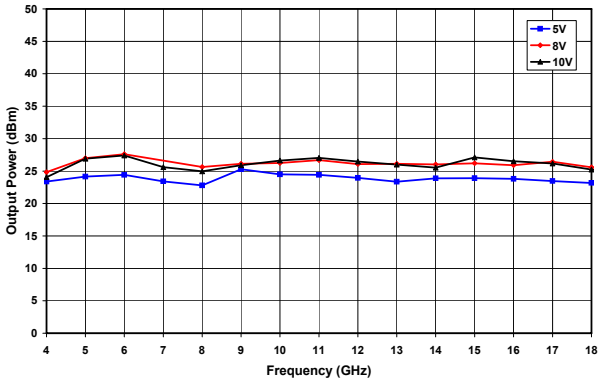

Figure 1. Output Power vs. Frequency and Drain Voltage at P_{in}=15dBm.

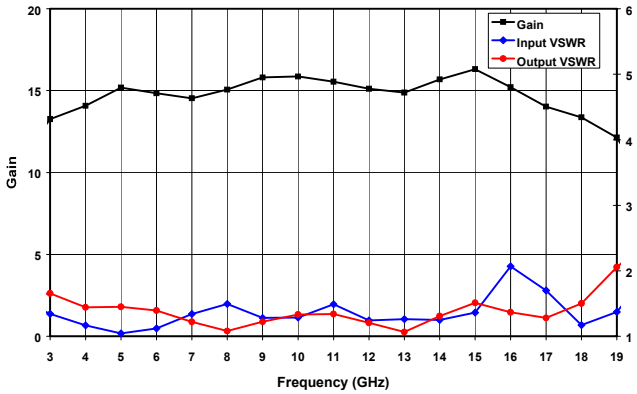

Figure 2. Small Signal Gain and VSWR at V_D=5V.

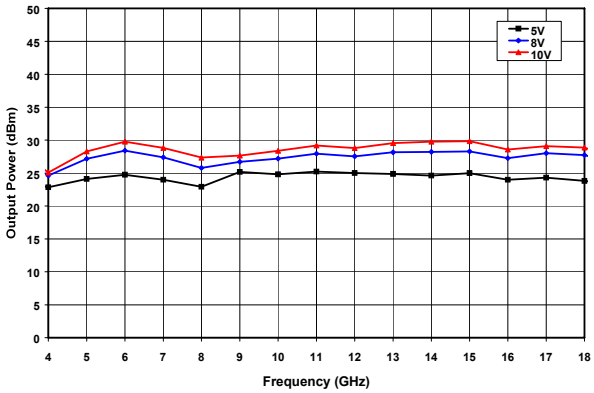

Figure 3. Saturated Output Power vs. Frequency and Drain Voltage.

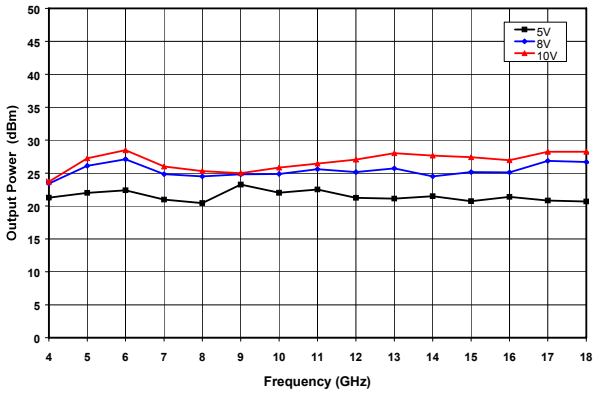

Figure 4. 1dB Compression Point vs. Frequency and Drain Voltage.

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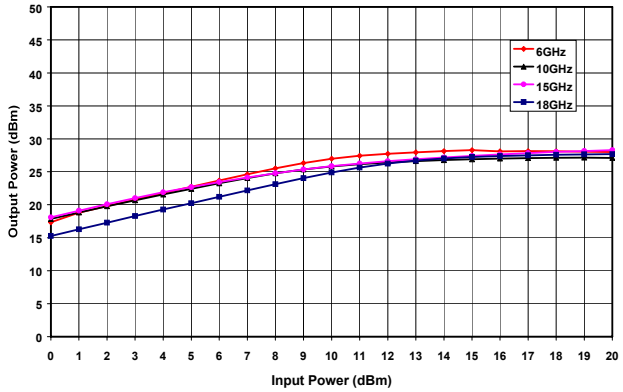

Figure 5. Output Power vs. Input Power and Frequency at V_D=8V.

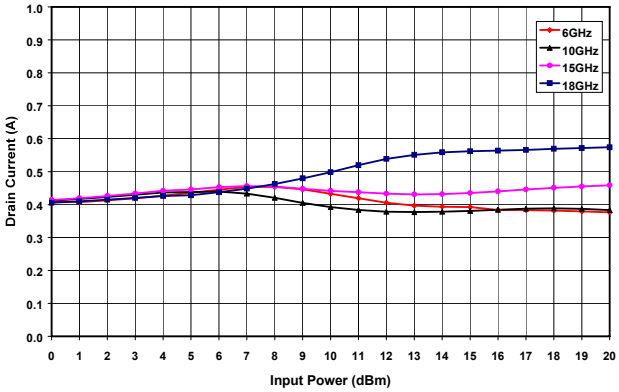

Figure 6. RF Drain Current vs. Input Power and Frequency at V_D=8V.

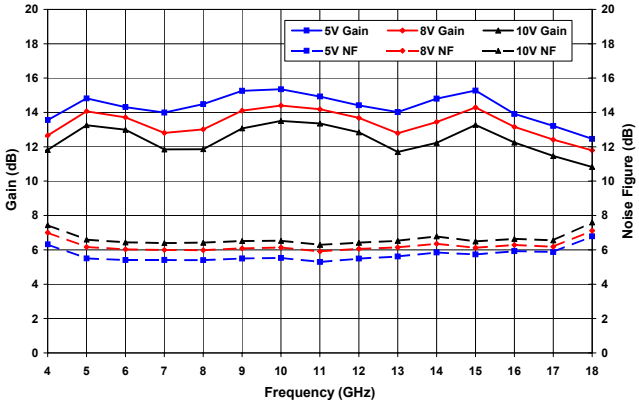

Figure 7. Gain and Noise Figure vs. Frequency and Drain Voltage at 25% I_{DSS}.

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Mechanical Information

Chip Size: 3.000 x 3.000 x 0.075 mm (118 x 118 x 3 mils)

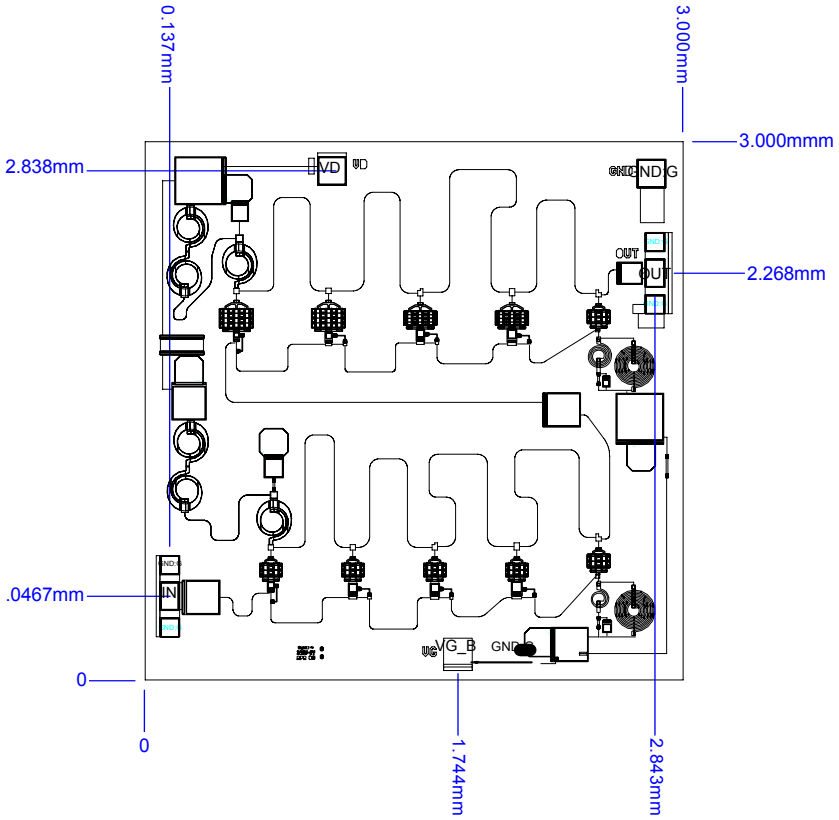

Figure 8. Die Layout

Chip edge to bond pad dimensions are shown to the center of the bond pad.

Bond Pad Dimensions

Pad	Size (µm)	Size (mils)
RF In and Out	100 x 150	4 x 6
DC Drain Supply Voltage VDD	150 x 150	6 x 6
DC Gate Supply Voltage VG_B	150 x 150	6 x 6

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Assembly and Bonding Diagram

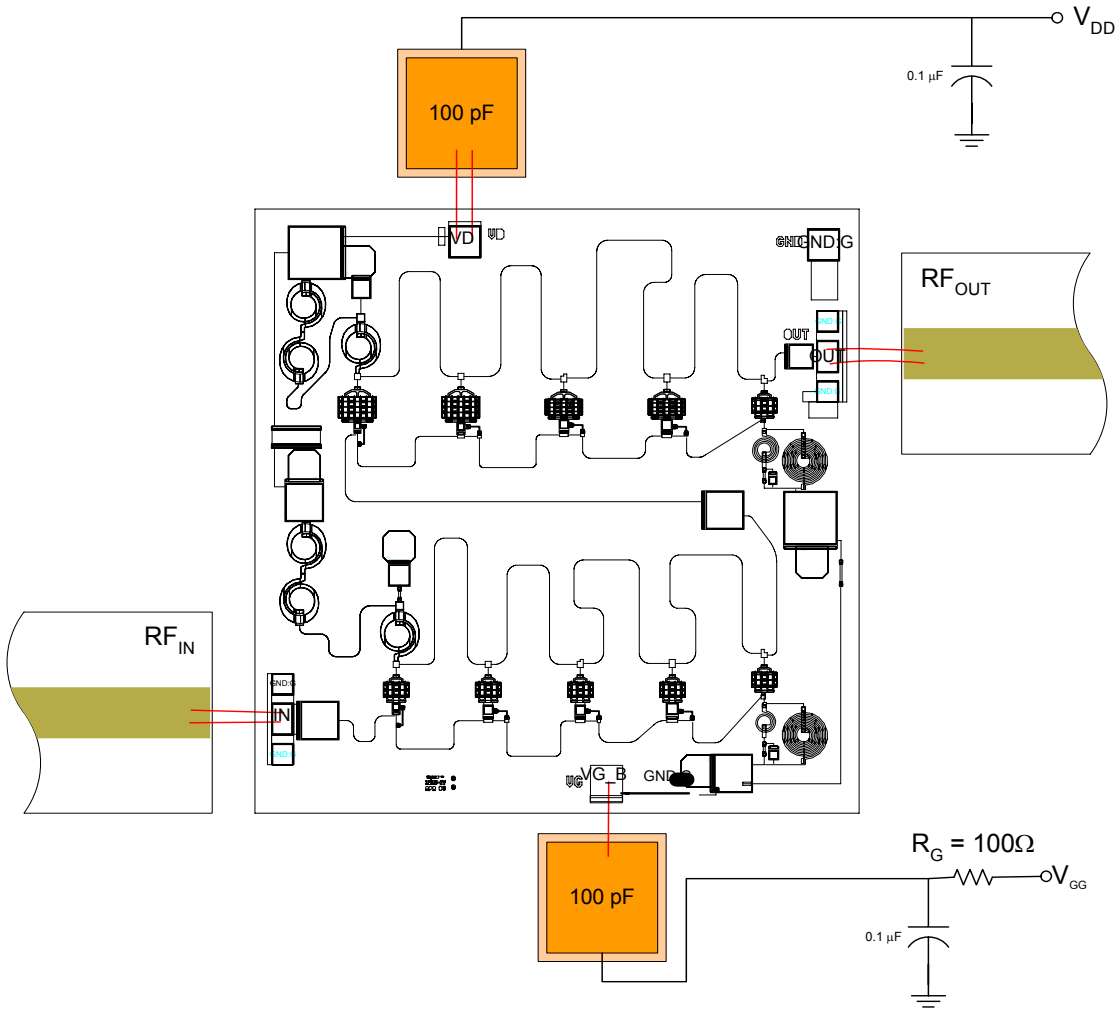

Figure 9. Recommended bonding diagram for pedestal mount.
Support circuitry typical of MMIC characterization fixture for CW testing.

Assembly Instructions:

Die attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

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