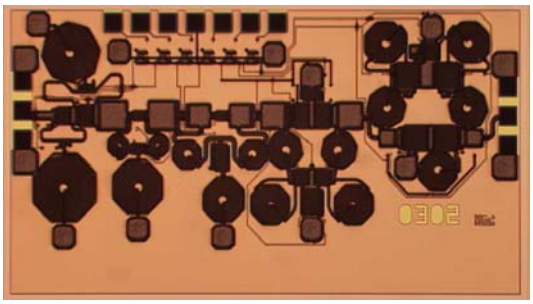
Phase Shifter
1.0-1.9 GHz

MAPCGM0001-DIE
903215 —
Preliminary Information

Features

- 6 Bit Phase Shifter
- 360º Coverage, LSB = 5.6º
- TTL Control Inputs
- MSAG™ Process



Description

The MAPCGM0001-Die is a 6-bit Phase Shifter with Parallel TTL Input Control. This product is fully matched to 50 ohms on both the input and output. The part has 360º of phase coverage with LSB of 5.6º.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG™) Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- Satellite Communication
- Phased Array Radar

Absolute Maximum Conditions [1]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	36	dBm
Digital Supply Voltage	V_{EE}	-6.0	V
Digital Supply Current	I_{EE}	20	mA
Junction Temperature	T_j	180	°C
Storage Temperature	T_{STG}	-55 to +150	°C

1. Operation outside of these ranges may reduce product reliability. Operation at other than the typical values may result in performance outside the guaranteed limits.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Digital Supply Voltage	V_{EE}	-5.2	-5	-4.8	V
Control Voltage	$V_{control\ pads}$				
Logic High		2.8	5	5	V
Logic Low		0	0	0.4	V

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Electrical Characteristics: $T_B = 25°C^2$, $Z_0 = 50\Omega$, $V_{EE} = -5V$

Parameter	Symbol	Typical	Units
Bandwidth	f	1.0-1.9	GHz
Insertion Loss	IL	5.3	dB
Input VSWR (At Reference)	VSWR	1.3:1	
Output VSWR (At Reference)	VSWR	1.2:1	
RMS Phase Error	RMS	6.6	°
Phase Range	$\Delta\Phi$	354	°
Gain Variation over all Phase Shifter settings	ΔG	< 2	dB
Digital Supply Current	I_{EE}	< 10	mA
Input Third Order Intercept	ITOI	37	dBm
Input 1-dB Compression Point	P_{1dB}	27	dBm

2. T_B = MMIC Base Temperature

Operating Instructions

This device is static and light sensitive. The digital circuitry operation can be impaired under high intensity light, e.g. microscope light. Please handle with care. To operate the device, follow these steps.

1. Power Up: Apply V_{EE} = -5 V.
2. Apply Logic Voltages to control Circuits as listed in Recommended Operating Conditions.
3. Power Down: Set V_{EE} = 0.

ATTENTION
Static-Sensitive Devices
Handling Precautions Required

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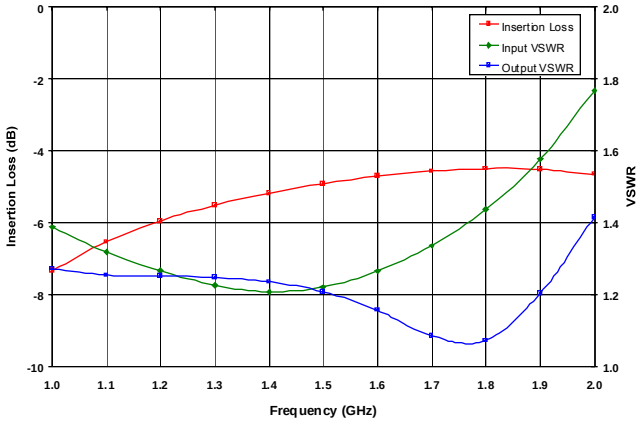

Figure 1. Reference State Insertion Loss, Input and Output VSWR vs. Frequency

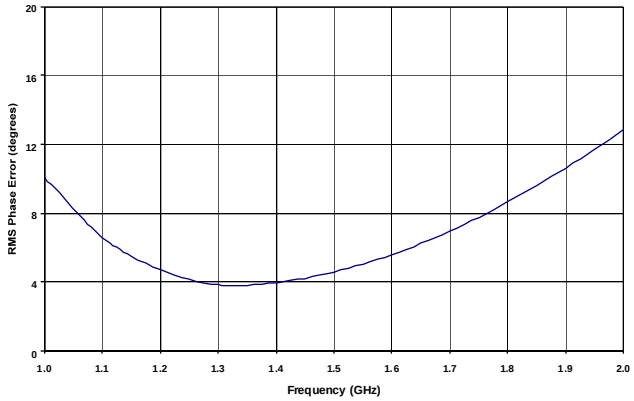

Figure 2. Corrected RMS Phase Error Over All Phase States

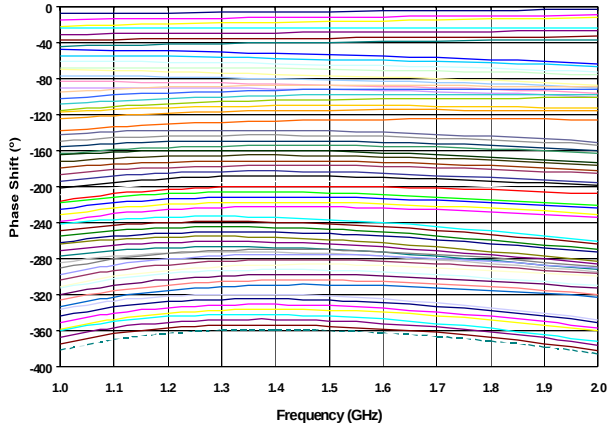

Figure 3. Phase Shift Over All Phase States

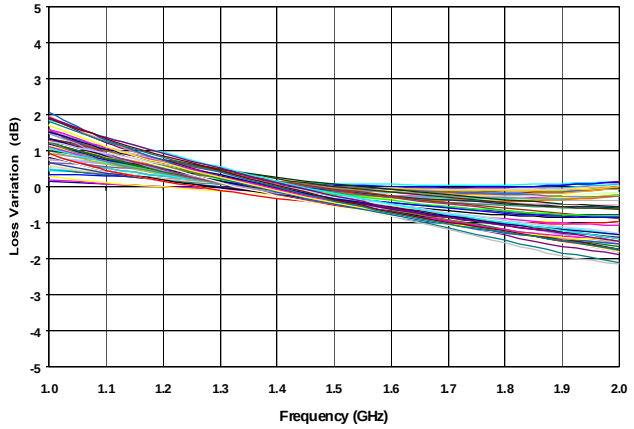

Figure 4. Loss Variation Over All Phase States

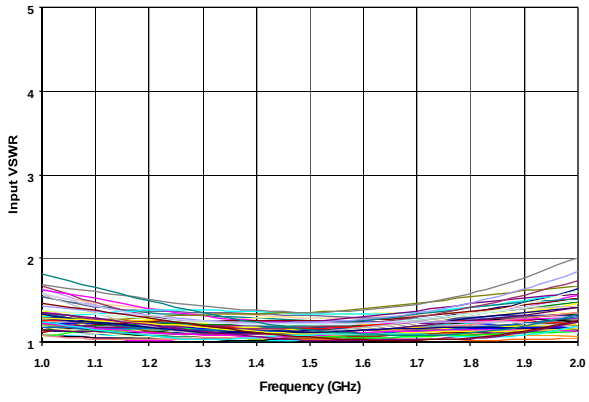

Figure 5. Input VSWR Over All Phase States

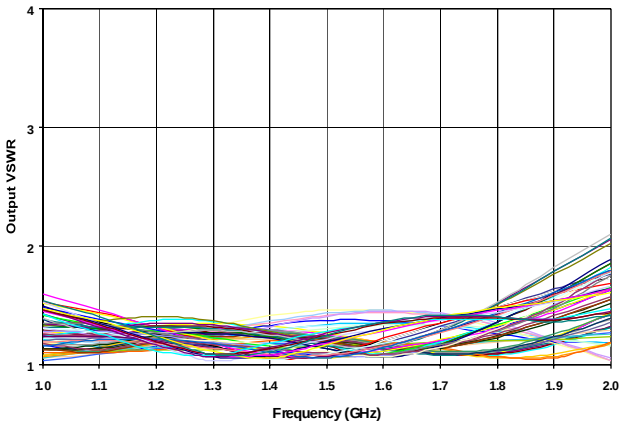

Figure 6. Output VSWR Over All Phase States

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Mechanical Information

Chip Size: 3.814 x 2.054 x 0.075 mm (150 x 81 x 3 mils)

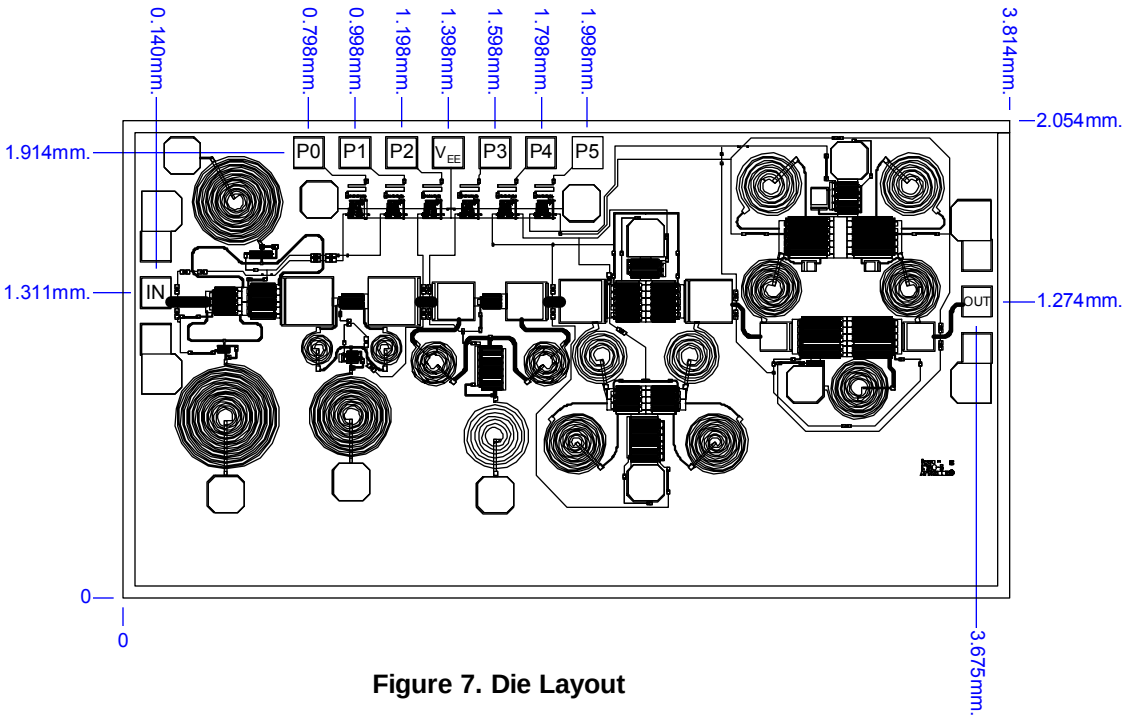

Figure 7. Die Layout

Bond Pad Information

Pad	Type	Nominal Voltage	Size	
			(µm)	(mils)
IN, OUT	RF	N/A	100 x 200	4 x 8
V_{EE}	DC	-5.0 V	125 x 125	5 x 5
P0 to P5	Control	0 / 5 V	125 x 125	5 x 5

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Assembly and Bonding Diagram

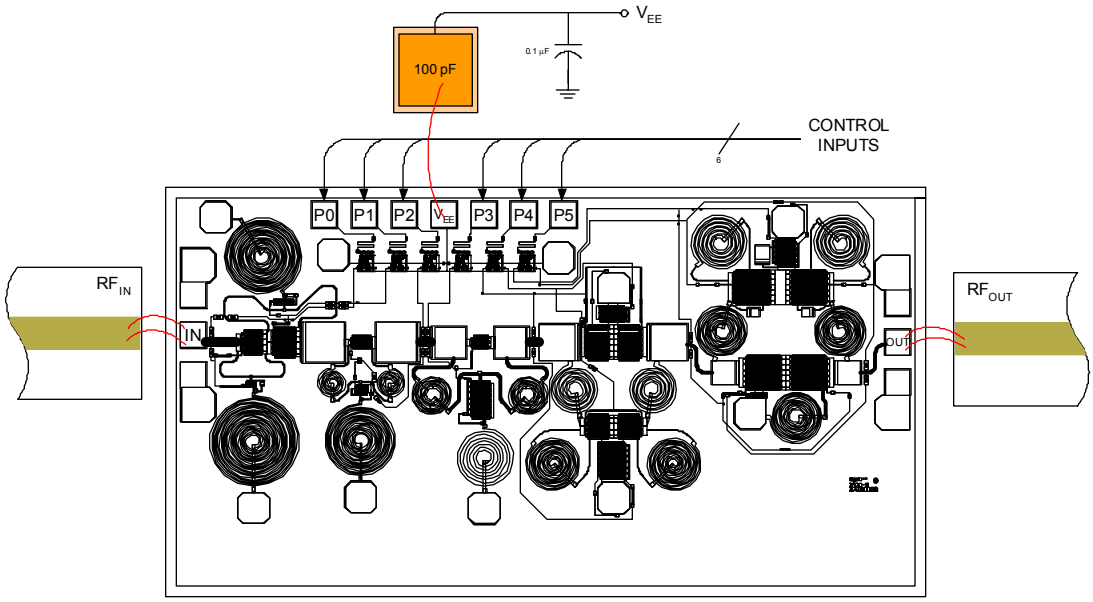

Figure 8. Recommended bonding diagram for pedestal mount.
Support circuitry typical of MMIC characterization.

Truth Table[3]

Designation	Description	Level	State
P5	180° Phase Bit : MSB	Logic High	Phase Shift ≈ -180°
P4	90° Phase Bit	Logic High	Phase Shift ≈ -90°
P3	45° Phase Bit	Logic High	Phase Shift ≈ -45°
V_{EE}	Digital Supply Voltage	-5V	ON
P2	22.5° Phase Bit	Logic High	Phase Shift ≈ -22.5°
P1	11.2° Phase Bit	Logic High	Phase Shift ≈ -11.2°
P0	5.6° Phase Bit : LSB	Logic High	Phase Shift ≈ -5.6°

3. All Phase Bits at Logic Low = Reference State.

Assembly Instructions:

Die attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{EE} before applying positive bias to Control Pads.

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