SPANSION™ MCP

Data Sheet

September 2003

This document specifies SPANSION™ memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a SPANSION™ product. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about SPANSION™ memory solutions.

3 Stacked MCP (Multi-Chip Package) FLASH & FLASH & FCRAM

CMOS

128M (×16) Burst FLASH MEMORY &
128M (×16) Burst FLASH MEMORY &
128M (×16) Page/Burst Mobile FCRAM™

MB84SF6H6H6L2-70

■ FEATURES

- **Power supply voltage**
  Flash _1 & 2: V_{ccf} = 1.65 V to 1.95 V
  FCARM: V_{ccr} = 2.5 V to 3.1 V, V_{ccqr} = 1.65 V to 1.95 V
- **High performance**
  11 ns maximum Burst read access time, 56 ns maximum random access time (Flash_1 & Flash_2)
  11 ns maximum Burst read access time, 70 ns maximum random access time (FCRAM™)

(Continued)

■ PRODUCT LINEUP

		Flash_1 & Flash_2	FCRAM
Supply Voltage (V)		V_{ccf}_1 & 2* = 1.8 V $^{+0.15V}_{-0.15V}$	V_{ccr}* = 3.0 V $^{+0.10V}_{-0.50V}$
I/O Supply Voltage (V)		V_{ccqr} = 1.65 V to 1.95 V	V_{ccqr} = 1.65 V to 1.95 V
Synchronous/ Burst	Max Latency Time (ns)	71	—
	Max Burst Access Time (ns)	11	11
	Max $\overline{OE}$ Access Time (ns)	11	—
Asynchronous	Max Address Access Time (ns)	56	70
	Max $\overline{CE}$ Access Time (ns)	56	70
	Max $\overline{OE}$ Access Time (ns)	11	40
	Max Page Access Time (ns)	—	20

*: All of V_{ccf}_1, V_{ccf}_2 and V_{ccr} must be the same level when either part is being accessed.

■ PACKAGE

115-ball plastic FBGA

BGA-115P-M03

FUJITSU
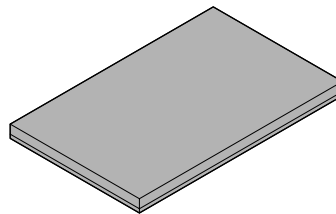
- **Operating Temperature**
  −30 °C to +85 °C
- **Package 115-ball BGA**

— **FLASH MEMORY_1 & FLASH MEMORY_2**

- **0.13 μm process technology**
- **Single 1.8 volt read, program and erase (1.65 V to 1.95 V)**
- **Simultaneous Read/Write operation (Dual Bank)**
- **FlexBank™ *1**
  Bank A: 16Mbit (4 Kwords × 8 and 32 Kwords × 31)
  Bank B: 48Mbit (32 Kwords × 96)
  Bank C: 48Mbit (32 Kwords × 96)
  Bank D: 16Mbit (4 Kwords × 8 and 32 Kwords × 31)
- **High Performance Burst frequency reach at 66MHz**
  Burst access times of 11 ns @ 30 pF at industrial temperature range
  Asynchronous random access times of 56 ns (at 30 pF)
- **Programmable Burst Interface**
  Linear Burst: 8, 16, and 32 words with wrap-around
- **Minimum 100,000 program/erase cycles**
- **Sector Erase Architecture**
  Eight 4 Kwords, two hundred fifty-four 32 Kwords sectors, eight 4 Kwords sectors.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **$\overline{WP}$ Input Pin ($\overline{WP}$_1, $\overline{WP}$_2)**
  At V_{IL}, allows protection of "outermost" 4×4 K words on low, high end or both ends of boot sectors, regardless
  of sector protection/unprotection status.
- **Accelerate Pin (ACC)**
  At V_{ACC}, increases program performance. ; all sectors locked when ACC = V_{IL}
- **Embedded Erase™ *2 Algorithms**
  Automatically preprograms and erases the chip or any sector
- **Embedded Program™ *2 Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{Data}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready Output (RY/$\overline{BY}$)**
  In Synchronous Mode, indicates the status of the Burst read.
  In Asynchronous Mode, indicates the status of the internal program and erase function.
- **Automatic sleep mode**
  When address remain stable, the device automatically switches itself to low power mode
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Hardware reset pin ($\overline{RESET}$)**
  Hardware method to reset the device for reading array data
- **Please refer to "MBM29BS12DH" Datasheet in deteiled function**

(Continued)

(Continued)

— **FCRAM™ *3**

  • **Power dissipation**
    Operating   : 35 mA Max
    Standby   : 300 μA Max (no CLK)
  • **Various Partial Power Down mode**
    Sleep   : 10 μA Max
    16M Partial : 120 μA Max
    32M Partial : 150 μA Max
  • **Power down control by CE2r**
  • **8 words Page Read Access Capability**
  • **Burst Read/Write Access Capability**
  • **Byte write control: $\overline{\text{LB}}$(DQ$_7$ to DQ$_0$), $\overline{\text{UB}}$(DQ$_{15}$ to DQ$_8$)**
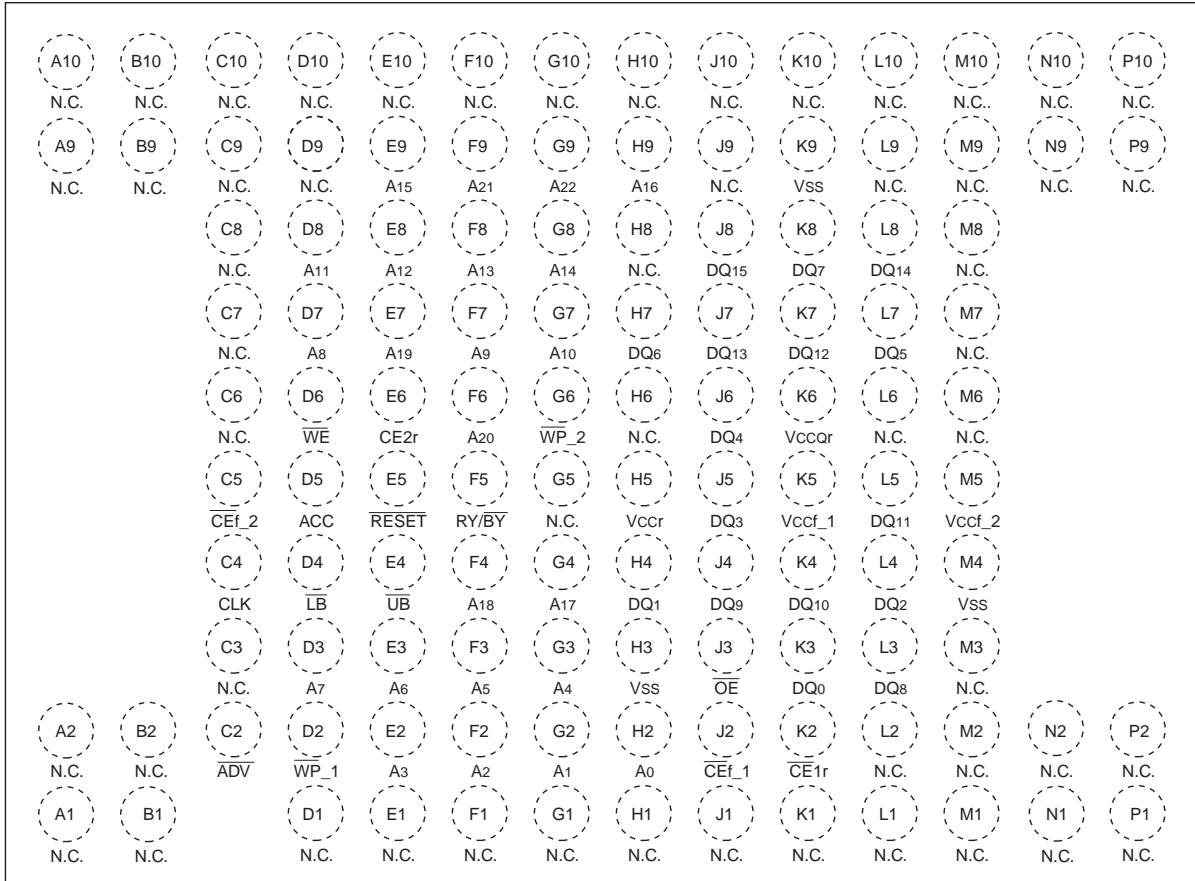
*1: FlexBank™ is a trademark of Fujitsu Limited, Japan.

*2: Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

*3: FCRAM™ is a trademark of Fujitsu Limited, Japan.

■ PIN ASSIGNMENT

(Top View)
Marking side

|													
A10	B10	C10	D10	E10	F10	G10	H10	J10	K10	L10	M10	N10	P10
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C..	N.C.	N.C.
A9	B9	C9	D9	E9	F9	G9	H9	J9	K9	L9	M9	N9	P9
N.C.	N.C.	N.C.	N.C.	A15	A21	A22	A16	N.C.	VSS	N.C.	N.C.	N.C.	N.C.
		C8	D8	E8	F8	G8	H8	J8	K8	L8	M8		
		N.C.	A11	A12	A13	A14	N.C.	DQ15	DQ7	DQ14	N.C.		
		C7	D7	E7	F7	G7	H7	J7	K7	L7	M7		
		N.C.	A8	A19	A9	A10	DQ6	DQ13	DQ12	DQ5	N.C.		
		C6	D6	E6	F6	G6	H6	J6	K6	L6	M6		
		N.C.	$\overline{WE}$	CE2r	A20	$\overline{WP\_2}$	N.C.	DQ4	VCCQr	N.C.	N.C.		
		C5	D5	E5	F5	G5	H5	J5	K5	L5	M5		
		$\overline{CEf\_2}$	ACC	$\overline{RESET}$	RY/$\overline{BY}$	N.C.	VCCr	DQ3	VCCf_1	DQ11	VCCf_2		
		C4	D4	E4	F4	G4	H4	J4	K4	L4	M4		
		CLK	$\overline{LB}$	$\overline{UB}$	A18	A17	DQ1	DQ9	DQ10	DQ2	VSS		
		C3	D3	E3	F3	G3	H3	J3	K3	L3	M3		
		N.C.	A7	A6	A5	A4	VSS	$\overline{OE}$	DQ0	DQ8	N.C.		
A2	B2	C2	D2	E2	F2	G2	H2	J2	K2	L2	M2	N2	P2
N.C.	N.C.	$\overline{ADV}$	$\overline{WP\_1}$	A3	A2	A1	A0	$\overline{CEf\_1}$	$\overline{CE1r}$	N.C.	N.C.	N.C.	N.C.
A1	B1		D1	E1	F1	G1	H1	J1	K1	L1	M1	N1	P1
N.C.	N.C.		N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.

(BGA-115P-M03)

■ PIN DESCRIPTION

Pin name	Input/ Output	Description
A_{22} to A_0	I	Address Inputs (Common)
DQ_{15} to DQ_0	I/O	Data Inputs/Outputs (Common)
$\overline{CE}f\_1$	I	Chip Enable (Flash_1)
$\overline{CE}f\_2$	I	Chip Enable (Flash_2)
$\overline{CE}1r$	I	Chip Enable (FCRAM)
CE2r	I	Chip Enable (FCRAM)
$\overline{OE}$	I	Output Enable (Common)
$\overline{WE}$	I	Write Enable (Common)
RY/$\overline{BY}$	O	Ready Output. (In asynchronous mode, RY/$\overline{BY}$ Output) / (Low Active) (Flash_1 & Flash_2) & Wait Signal Output (FCRAM)
$\overline{UB}$	I	Upper Byte Control (FCRAM)
$\overline{LB}$	I	Lower Byte Control (FCRAM)
$\overline{ADV}$	I	Address Data Valid (Common)
CLK	I	CLK Input (Common)
$\overline{RESET}$	I	Hardware Reset Pin/Sector Protection Unlock (Flash_1& Flash_2)
$\overline{WP}\_1$	I	Write Protect (Flash_1)
$\overline{WP}\_2$	I	Write Protect (Flash_2)
ACC	I	Program Acceleration (Flash_1&2)
N.C.	—	No Internal Connection
V_{SS}	Power	Device Ground (Common)
$V_{CC}f\_1$	Power	Device Power Supply (Flash_1)
$V_{CC}f\_2$	Power	Device Power Supply (Flash_2)
$V_{CC}r$	Power	Device Power Supply (FCRAM)
$V_{CCQ}r$	Power	I/O Power Supply (FCRAM)

MB84SF6H6H6L2-70

■ BLOCK DIAGRAM
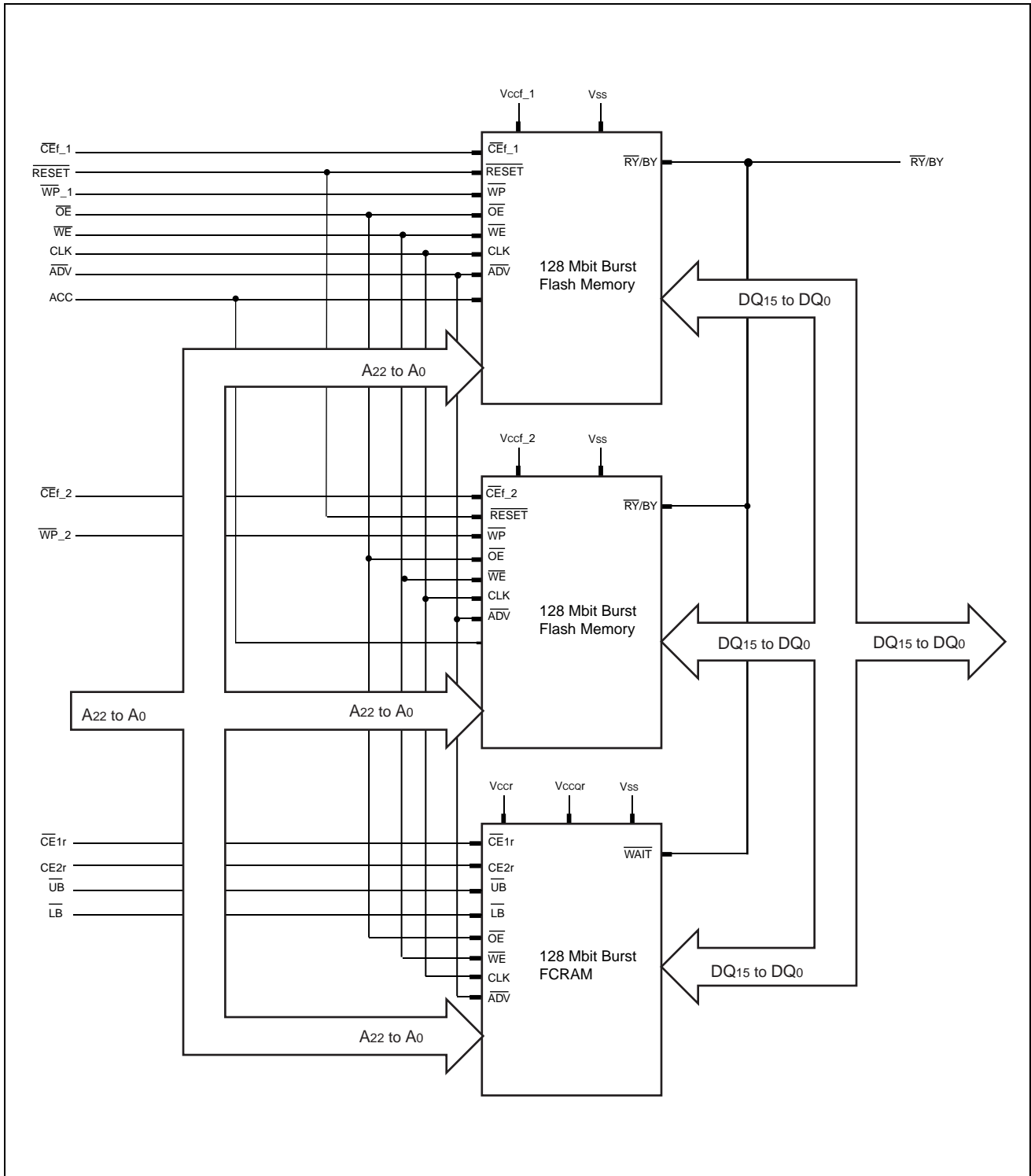
■ DEVICE BUS OPERATIONS

• **Asynchronous Operation**

Operation	$\overline{CEf\_1}$	$\overline{CEf\_2}$	$\overline{CE1r}$	CE2r	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	A_{22} to A_0	DQ_7 to DQ_0	DQ_{15} to DQ_8	$\overline{ADV}$	$\overline{RESET}$	$\overline{WP\_1}$	$\overline{WP\_2}$	ACC	$\overline{RY}/BY(\overline{WAIT})$
Full Standby	H	H	H	H	X	X	X	X	X	High-Z	High-Z	X	H	X	X	X	High-Z
Output Disable*1	H	H	L	H	H	H	X	X	X*3	High-Z	High-Z	X	H	X	X	X	High-Z
	H	L	H	H	H	H	X	X	X			X					
	L	H	H	H	H	H	X	X	X			X					
Flash_1 or 2 Asynchronous Read - Addresses Latched*2	L	H	H	H	L	H	X	X	Addr In	D_OUT	D_OUT	L	H	X	X	X	High-Z
	H	L															
Flash_1or 2 Write - WE address latched*4	L	H	H	H	H	L	X	X	Addr In	D_IN	D_IN	L	H	X*5	X*5	H*5	High-Z
	H	L															
Flash_1or 2 Write - ADV address latched*4	L	H	H	H	H	⎍	X	X	Addr In	D_IN	D_IN	⎍	H	X*5	X*5	H*5	High-Z
	H	L															
FCRAM NO Read	H	H	L	H	L	H	H	H	Valid	High-Z	High-Z	*6	X	X	X	X	High-Z
FCRAM Read (Upper Byte)	H	H	L	H	L	H	H	L	Valid	High-Z	Output Valid	*6	X	X	X	X	High-Z
FCRAM Read (Lower Byte)	H	H	L	H	L	H	L	H	Valid	Output Valid	High-Z	*6	X	X	X	X	High-Z
FCRAM Read (Word)	H	H	L	H	L	H	L	L	Valid	Output Valid	Output Valid	*6	X	X	X	X	High-Z
FCRAM Page Read	H	H	L	H	L	H	L/H	L/H	Valid	*7	*7	*6	X	X	X	X	High-Z
FCRAM No Write	H	H	L	H*9	H*9	L	H	H	Valid	Invalid	Invalid	*6	X	X	X	X	High-Z
FCRAM Write (Upper Byte)	H	H	L	H*9	H*9	L	H	L	Valid	Invalid	Input Valid	*6	X	X	X	X	High-Z
FCRAM Write (Lower Byte)	H	H	L	H*9	H*9	L	L	H	Valid	Input Valid	Invalid	*6	X	X	X	X	High-Z
FCRAM Write (Word)	H	H	L	H*9	H*9	L	L	L	Valid	Input Valid	Input Valid	*6	X	X	X	X	High-Z
Flash_1 Boot Sector Write Protection*5	X	X	X	X	X	X	X	X	X	X	X	X	H	L*5	X	X	High-Z
Flash_2 Boot Sector Write Protection*5	X	X	X	X	X	X	X	X	X	X	X	X	H	X	L*5	X	High-Z
Flash_1 &2 All Sector Write Protection*5	X	X	H	H	X	X	X	X	X	X	X	X	H	X	X	L*5	High-Z
Flash_1 & Flash_2 RESET	X	X	H	H	X	X	X	X	X	High-Z	High-Z	X	L	X	X	X	High-Z
FCRAM Power Down*8	X	X	X	L	X	X	X	X	X	High-Z	High-Z	X	X	X	X	X	High-Z

(Continued)

7

(Continued)
Legend : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance.
　　　　See "• DC Characteristics" in "■ ELECTRICAL CHARACTERISTICS" for voltage levels.

*1 :　FCRAM Output Disable Mode($\overline{CE}$1r = "L")Should not be kept this logic condition longer than 4 ms.
　　　Please contact local FUJITSU representative for the relaxation of 4 ms limitation.

*2 :　$\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*3 :　Can be either V_{IL} or V_{IH} but must be valid before Read or Write.

*4 :　Write Operation: at asynchronous mode, addresses are latched on the last falling edge of
　　　$\overline{WE}$ pulse while $\overline{ADV}$ is held low or rising edge of $\overline{ADV}$ pulse whichever comes first.
　　　Data is latched on the 1st rising edge of $\overline{WE}$.

*5 :　At $\overline{WP}$=V_{IL}, SA0 to SA3 and SA266 to SA269 are protected. At ACC=V_{IL}, all sectors are protected.

*6 :　"L" for address pass through and "H" for address latch on the rising edge of $\overline{ADV}$.

*7 :　Output is either Valid or High-Z depending on the level of $\overline{UB}$ and $\overline{LB}$ input.

*8 :　Power Down mode can be entered from Standby state and all DQ pins are in High-Z state.
　　　Data retention depends on the selection of Partial Size.
　　　Refer to "2. Functional Description • Power Down" in "■ 128M FCRAM CHARACTERISTICS for MCP" for the
　　　details.

*9 :　$\overline{OE}$ can be V_{IL} during Write operation if the following conditions are satisfied;
　　　(1)　Write pulse is initiated by $\overline{CE}$1r (refer to $\overline{CE}$1r Controlled Write timing), or
　　　　　cycle time of the previous operation cycle is satisfied.
　　　(2)　$\overline{OE}$ stays V_{IL} during Write cycle.

• **Synchronous Operation**

Operation	$\overline{CEf\_1}$	$\overline{CEf\_2}$	$\overline{CE1r}$	CE2r	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	A_{22} to A_0	DQ_7 to DQ_0	DQ_{15} to DQ_8	CLK*1	$\overline{ADV}$	$\overline{RESET}$	$\overline{WP\_1}$	$\overline{WP\_2}$	ACC	$\overline{RY/BY(WAIT)}$
Flash_1 or 2 Load Starting Burst Address (CLK latch)*3	L	H	H	H	X	H	X	X	Addr In	X	X	↑*9	⊔	H	X	X	X	High-Z
	H	L																
Flash_1 or 2 Advance Burst to next address with appropriate Data presented on the Data Bus*3	L	H	H	H	L	H	X	X	X	D$_{OUT}$	D$_{OUT}$	↑*9	H	H	X	X	X	High-Z
	H	L																
Flash_1 or 2 Terminate current Burst read cycle	H	H	H	H	X	H	X	X	X	X	HIGH-Z	↑*9	X	H	X	X	X	High-Z
Flash_1 or 2 Terminate current Burst read cycle and start new Burst read cycle	L	H	H	H	X	H	X	X	Addr In	D$_{OUT}$	D$_{OUT}$	↑*9	⊔	H	X	X	X	High-Z
	H	L																
Flash_1 or 2 Burst Suspend	L	H	H	H	H	H	X	X	X	High-Z	High-Z	X	H	H	X	X	X	High-Z
	H	L																
Flash_1 or 2 Synchronous Write - WE address latched*12	L	H	H	H	H	L	X	X	Addr In	D$_{IN}$	D$_{IN}$	H/L	L	H	X*4	X*4	H*4	High-Z
	H	L																
Flash_1 or 2 Synchronous Write - CLK address latched*12	L	H	H	H	H	⊔	X	X	Addr In	DIN	DIN	↑*9	L	H	X*4	X*4	H*4	High-Z
	H	L																
Flash_1 or 2 Synchronous Write -ADV address latched *12	L	H	H	H	H	⊔	X	X	Addr In	D$_{IN}$	D$_{IN}$	H/L	⊔	H	X*4	X*4	H*4	High-Z
	L	L																
Flash_1& 2 Terminate current Burst read via RESET	X	X	H	H	X	H	X	X	X	HIGH-Z	HIGH-Z	X	X	L	X	X	X	High-Z
FCRAM Start Address*2 Latch	H	H	L	H	X*5	X*5	X*6	X*6	Valid*7	High-Z*8	High-Z*8	↑*9	⊔	X	X	X	X	High-Z*14
FCRAM Advance Burst Read to Next Address*2	H	H	L	H	L	H	X*6	X*6	X	Output Valid*10	Output Valid*10	↑*9	H	X	X	X	X	Output Valid
FCRAM Burst Read Suspend*2	H	H	L	H	H	H	X*6	X*6	X	High-Z	High-Z	↑*9	H	X	X	X	X	High-Z*15

(Continued)

(Continued)

Operation	$\overline{CEf}\_1$	$\overline{CEf}\_2$	$\overline{CE1r}$	CE2r	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	A_{22} to A_0	DQ_7 to DQ_0	DQ_{15} to DQ_8	CLK*1	$\overline{ADV}$	$\overline{RESET}$	$\overline{WP}\_1$	$\overline{WP}\_2$	ACC	$RY/BY(\overline{WAIT})$
FCRAM Advance Burst Write to Next Address*2	H	H	L	H	H	L*13	X*6	X*6	X	Input Valid *11	Input Valid *11	⤒ *9	H	X	X	X	X	High-Z*16
FCRAM Burst Write Suspend*2	H	H	L	H	H	H*13	X*6	X*6	X	Input Invalid	Input Invalid	⤒ *9	H	X	X	X	X	High-Z*15
FCRAM Terminate Burst Read	H	H	⌐	H	L	H	X*6	X*6	X	High-Z	High-Z	X	H	X	X	X	X	High-Z
FCRAM Terminate Burst Write	H	H	⌐	H	H	L	X*6	X*6	X	High-Z	High-Z	X	H	X	X	X	X	High-Z

Legend : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, ⤒ = positive edge, ⌐ = positive edge of Low pulse, High-Z = High Impedance. See "• DC Characteristics" in "■ ELECTRICAL CHARACTERISTICS" for voltage levels.

*1 : Default state is "X" after power-up.

*2 : FCRAM Output Disable Mode($\overline{CE}$1r = "L")Should not be kept this logic condition longer than 4 ms. Please contact local FUJITSU representative for the relaxation of 4 ms limitation.

*3 : $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*4 : At $\overline{WP}=V_{IL}$, SA0 to SA3 and SA266 to SA269 are protected. At ACC=V_{IL}, all sectors are protected.

*5 : Can be either V_{IL} or V_{IH} except for the case the both of $\overline{OE}$ and $\overline{WE}$ are V_{IL}. It is prohibited to bring the both of $\overline{OE}$ and $\overline{WE}$ to V_{IL}.

*6 : Can be either V_{IL} or V_{IH} but must be valid before Read or Write is determined. And once $\overline{UB}$ and $\overline{LB}$ inputs are determined, it must not be changed until the end of burst.

*7 : Once valid address is determined, input address must not be changed during $\overline{ADV}$=L. In case A_{22}, "H" must not be changed until end of burst.

*8 : If $\overline{OE}$=L, output is either Invalid or High-Z depending on the level of $\overline{UB}$ and $\overline{LB}$ input. If $\overline{WE}$=L, Input is Invalid. If $\overline{OE}=\overline{WE}$=H, output is High-Z.

*9 : Valid clock edge shall be set on either positive or negative edge through CR (Configration Register) Set.

*10 : Output is either Valid or High-Z depending on the level of $\overline{UB}$ and $\overline{LB}$ input.

*11 : Input is either Valid or Invalid depending on the level of $\overline{UB}$ and $\overline{LB}$ input.

*12 : Write Operation: at synchronous mode, addresses are latched on the falling edge of $\overline{WE}$ while $\overline{ADV}$ is held low, active edge of CLK while $\overline{ADV}$ is held low or rising edge of $\overline{ADV}$ whichever happens first. Data is latched on the 1st rising edge of $\overline{WE}$.

*13 : When device is operationg in "$\overline{WE}$ Single Clock Pulse Control" mode, $\overline{WE}$ is don't care once write operation is determined by $\overline{WE}$ Low Pulse at the begginig of write access together with address latcing. Write suspend feature is not supported in "$\overline{WE}$ Single Clock Pulse Control" mode.

*14 : Output is either High-Z or Invalid depending on the level of $\overline{OE}$ and $\overline{WE}$ input.

*15 : Keep the level from previous cycle except for suspending on last data. Refere to "2. Functional Description • $\overline{WAIT}$ Output Function" in "■ 128M FCRAM CHARACTERISTICS for MCP" for the details.

*16 : $\overline{WAIT}$ output is driven in High level during write operation.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	−55	+125	°C
Ambient Temperature with Power Applied	T_A	−30	+85	°C
Voltage with Respect to Ground All pins except $\overline{RESET}$, ACC *1 *2	V_{IN}, V_{OUT}	−0.3	Vccf_1 +0.3	V
			Vccf_2 +0.3	V
			Vccɑr +0.3	V
Vccr Supply *1	Vccr	−0.3	+3.6	V
Vccf_1/ Vccf_2 / Vccɑr Supply *1	Vccf_1, Vccf_2, Vccɑr	−0.3	+2.5	V
ACC *1,*3	VACC	−0.5	+10.5	V

*1 : Voltage is defined on the basis of V_{SS} = GND = 0 V.

*2 : Minimum DC voltage on input or I/O pins is −0.3 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to −1.0 V for periods of up to 10 ns. Maximum DC voltage on input or I/O pins is Vccf_1 + 0.3 V or Vccf_2 +0.3V or Vccɑr + 0.2 V . During voltage transitions, input or I/O pins may overshoot to Vccf + 1.0 V or Vccf_2 + 1.0 V or Vccɑr + 1.0 V for periods of up to 5 ns.

*3 : Minimum DC input voltage on ACC pin is −0.5 V. During voltage transitions, ACC pin may undershoot V_{SS} to −2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN} - V_{CC}) does not exceed +9.0 V. Maximum DC input voltage on ACC pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Ambient Temperature	T_A	−30	+85	°C
Vccr Supply Voltages	Vccr	+2.5	+3.1	V
Vccf/Vccɑr Supply Voltages	Vccf_1, Vccf_2, Vccɑr	+1.65	+1.95	V

Note : Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating conditionranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CCf}, V_{CCQr}		−1.0	—	+1.0	μA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{CCf}, V_{CCQr}		−1.0	—	+1.0	μA
Flash V_{CCf} Current (Standby) (Flash_1 & Flash_2)	I_{SB1f}	$\overline{CE}f = \overline{RESET} = V_{CCf} \pm 0.2$ V *9		—	1*7	50*7	μA
Flash_1 & 2 V_{CCf} Current (Standby, Reset) (Flash_1 & Flash_2)	I_{SB2f}	$\overline{RESET} = V_{SS} \pm 0.2$ V, CLK = V_{IL} *9		—	1*7	50*7	μA
Flash_1 & 2 V_{CCf} Current (Automatic Sleep Mode)*3 (Flash_1 & Flash_2)	I_{SB3f}	$V_{CCf} = V_{CCf}$ Max, $\overline{CE}f = V_{SS} \pm 0.2$ V, $\overline{RESET} = V_{CCf} \pm 0.2$ V, $V_{IN} = V_{CCf} \pm 0.2$ V or $V_{SS} \pm 0.2$ V *9		—	1*7	50*7	μA
Flash V_{CCf} Active Burst Read Current (Flash_1 or Flash_2)	I_{CC1f}	$\overline{CE}f = V_{IL}$, $\overline{OE} = V_{IH}$, $\overline{WE} = V_{IH}$, 66 MHz *9		—	15	30	mA
Flash V_{CCf} Active Asynchronous Read Current*1 (Flash_1 or Flash_2)	I_{CC2f}	$\overline{CE}f = V_{IL}$, $\overline{OE} = V_{IH}$, $\overline{WE} = V_{IH}$ *9	10 MHz	—	20	30	mA
			5 MHz		10	15	
Flash V_{CCf} Active Current *2 (Flash_1 or Flash_2)	I_{CC3f}	$\overline{CE}f = V_{IL}$, $\overline{OE} = V_{IH}$, $V_{PP} = V_{IH}$ *9		—	15	40	mA
Flash V_{CCf} Active Current (Read-While-Program) *4 (Flash_1 or Flash_2)	I_{CC4f}	$\overline{CE}f = V_{IL}$, $\overline{OE} = V_{IH}$ *9		—	25	60	mA
Flash V_{CCf} Active Current (Read-While-Erase) *4 (Flash_1 or Flash_2)	I_{CC5f}	$\overline{CE}f = V_{IL}$, $\overline{OE} = V_{IH}$ *9		—	25	60	mA
FCRAM V_{CCr} Power Down Current*5	I_{DDPSr}	$V_{CCr} = V_{CCr}$ Max, $V_{CCQr} = V_{CCQr}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $CE2r \leq 0.2$ V	Sleep	—	—	10	μA
	I_{DDP8r}		16M Partial	—	—	120	μA
	I_{DDP16r}		32M Partial	—	—	150	μA
FCRAM V_{CCr} Standby Current*5, *8	I_{SBSr}	$V_{CCr} = V_{CCr}$ Max, $V_{CCQr} = V_{CCQr}$ Max, V_{IN} (including CLK) = V_{IH} or V_{IL} , $\overline{CE}1r = CE2r = V_{IH}$		—	—	1.5	mA
	I_{SB1r}	$V_{CCr} = V_{CCr}$ Max, $V_{CCQr} = V_{CCQr}$ Max, V_{IN} (including CLK) ≤ 0.2 V or V_{IN} (including CLK) $\geq V_{CCQr} - 0.2$ V, $\overline{CE}1r = CE2r \geq V_{CCQr} - 0.2$ V		—	—	300	μA
	I_{SB2r}	$V_{CCQr} = V_{CCQr}$ Max, $t_{CK} = $ Min, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CCQr} - 0.2$ V, $\overline{CE}1r = CE2r \geq V_{CCQr} - 0.2$ V		—	—	350	μA

(Continued)

(Continued)

Parameter	Symbol	Conditions		Value Min	Value Typ	Value Max	Unit
FCRAM $V_{CC}r$ Active Current *5, *8	$I_{CC1}r$	$V_{CC}r = V_{CC}r$ Max, $V_{CCQ}r = V_{CCQ}r$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1r = V_{IL}$ and $CE2r = V_{IH}$, $I_{OUT} = 0$ mA	t_{RC} / t_{WC} = Min	—	—	35	mA
	$I_{CC2}r$		t_{RC} / t_{WC} = 1 μs	—	—	5	mA
FCRAM $V_{CC}r$ Page Read Current *5, *8	$I_{CC3}r$	$V_{CC}r = V_{CC}r$ Max, $V_{CCQ}r = V_{CCQ}r$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1r = V_{IL}$ and $CE2r = V_{IH}$, $I_{OUT}= 0$ mA, t_{PRC} = Min		—	—	15	mA
FCRAM $V_{CC}r$ Burst Access Current *5, *8	$I_{CC4}r$	$V_{CC}r = V_{CC}r$ Max, $V_{CCQ}r = V_{CCQ}r$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1r = V_{IL}$ and $CE2r = V_{IH}$, $t_{CK} = t_{CK}$ Min, BL = Continuous, $I_{OUT} = 0$ mA		—	—	30	mA
Input Low Level	V_{IL}	—		−0.3	—	$V_{CC} \times 0.2$ *6	V
Input High Level	V_{IH}	—		$V_{CC} - 0.4$ *6	—	$V_{CC} + 0.2$ *6	V
Output Low Voltage Level	$V_{OL}f$	$I_{OL} = 0.1$ mA	Flash_1 or Flash_2	—	—	0.1	V
	$V_{OL}r$	$I_{OL} = 1.0$ mA	FCRAM	—	—	0.4	V
Output High Voltage Level	$V_{OH}f$	$I_{OH} = - 0.1$ mA	Flash_1 or Flash_2	$V_{CC}f - 0.1$	—	—	V
	$V_{OH}r$	$V_{CCQ}r = V_{CCQ}r$ Min, $I_{OH} = - 0.5$ mA	FCRAM	1.4	—	—	V
Voltage for ACC Program Acceleration*10	V_{ACC}	—		8.5	—	9.5	V

*1 : The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2 : I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3 : Automatic sleep mode enables the low power mode when address remains stable for t_{ACC} + 60 ns.

*4 : Embedded Alogorithm (program or erase) is in progress. (@5 MHz)

*5 : FCRAM DC Current is measured after following POWER-UP timing.

*6 : V_{CC} means $V_{CC}f\_1$ or $V_{CC}f\_2$ or $V_{CCQ}r$.

*7 : Actual Standby Current is twice of what is indicated in the table, due to two Flash chips embedment withn one device.

*8 : I_{OUT} depemds on the output load comditions.

*9 : $\overline{CE}f$ means $\overline{CE}f\_1$ or $\overline{CE}f\_2$.

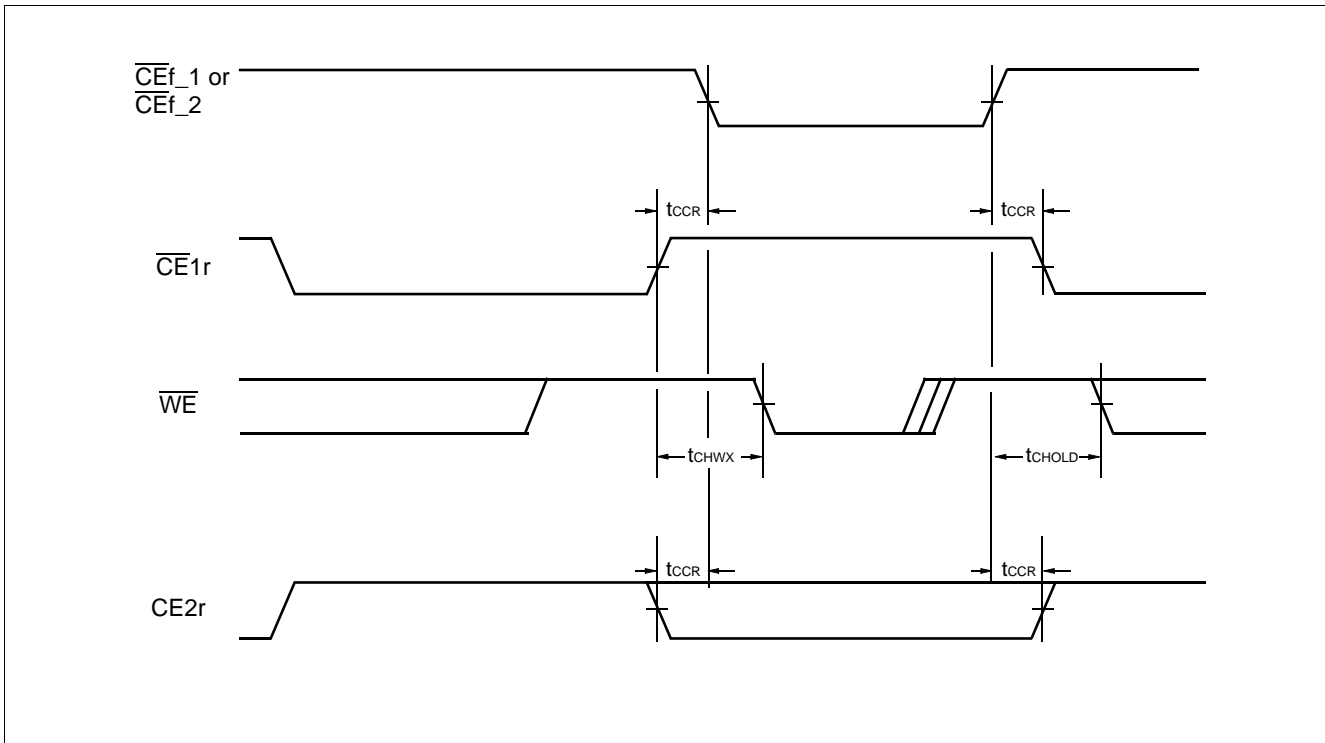*10 : Applicable for only $V_{CC}f\_1$ or $V_{CC}f\_2$.

- **AC Characteristics**

- $\overline{\text{CE}}$ **Timing**

Parameter	Symbol		Condition	Value		Unit
	JEDEC	Standard		Min	Max	
$\overline{\text{CE}}$ Recover Time	—	t_{CCR}	—	0	—	ns
$\overline{\text{CE}}$f Hold Time	—	t_{CHOLD}	—	3	—	ns
$\overline{\text{CE}}$1r High to $\overline{\text{WE}}$ Invalid time for Standby Entry	—	t_{CHWX}	—	10	—	ns

- **Timing Diagram for alternating RAM to Flash**

- **NOR Flash_1&2 Characteristics**
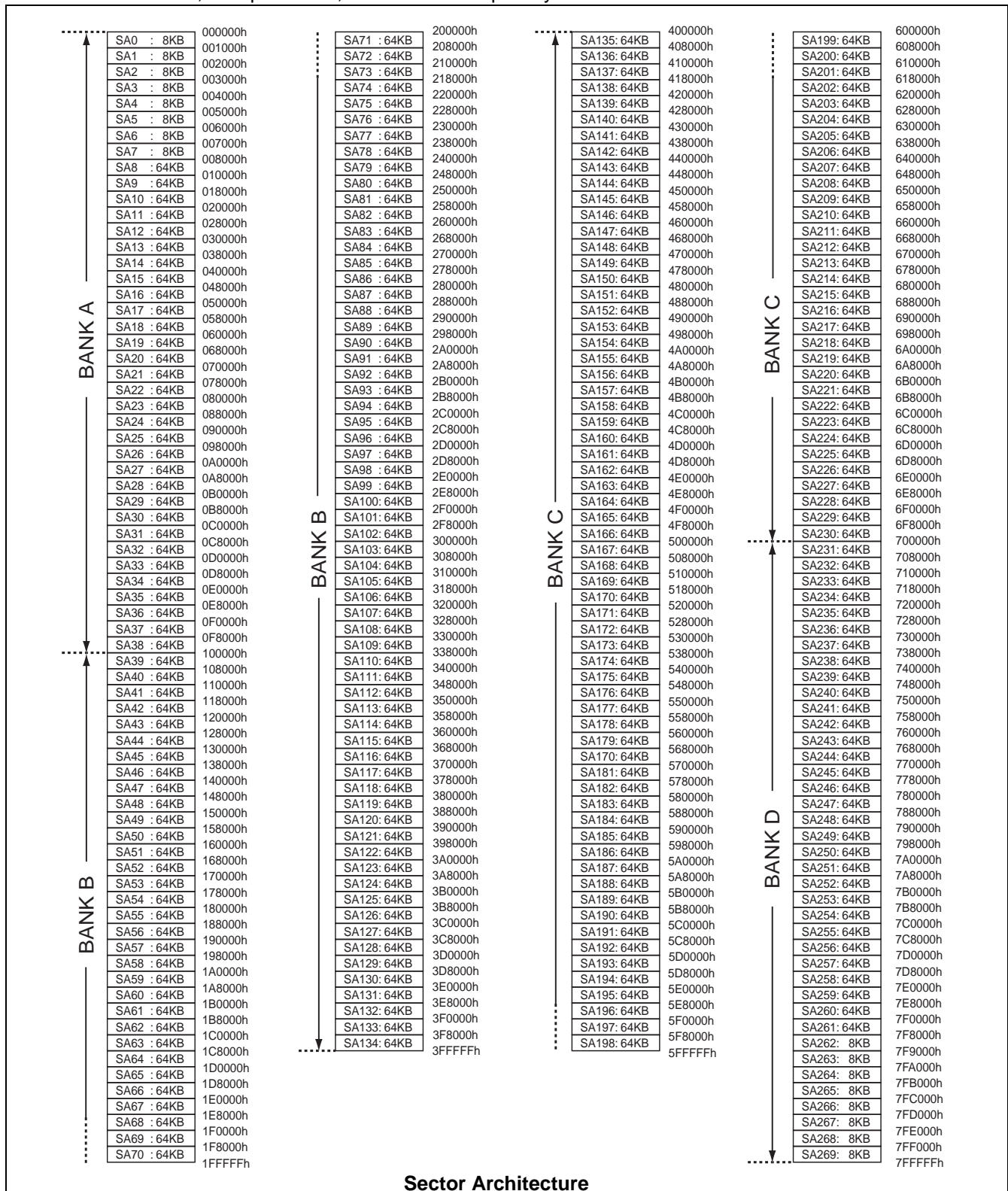 Please refer to "■ 128M BURST FLASH MEMORY CARACTERISTICS for MCP".

- **FCRAM Characteristics**
  Please refer to "■ 128M FCRAM CHARACTERISTICS for MCP".

■ 128M BURST FLASH MEMORY CHARACTERISTICS for MCP

1. Flexible Sector-erase Architecture on Flash Memory
- Sixteen 4K words, and one hundred twenty-six 32K words.
- Individual-sector, multiple-sector, or bulk-erase capability.

BANK A / BANK B

Sector	Size	Address
SA0	8KB	000000h
SA1	8KB	001000h
SA2	8KB	002000h
SA3	8KB	003000h
SA4	8KB	004000h
SA5	8KB	005000h
SA6	8KB	006000h
SA7	8KB	007000h
SA8	64KB	008000h
SA9	64KB	010000h
SA10	64KB	018000h
SA11	64KB	020000h
SA12	64KB	028000h
SA13	64KB	030000h
SA14	64KB	038000h
SA15	64KB	040000h
SA16	64KB	048000h
SA17	64KB	050000h
SA18	64KB	058000h
SA19	64KB	060000h
SA20	64KB	068000h
SA21	64KB	070000h
SA22	64KB	078000h
SA23	64KB	080000h
SA24	64KB	088000h
SA25	64KB	090000h
SA26	64KB	098000h
SA27	64KB	0A0000h
SA28	64KB	0A8000h
SA29	64KB	0B0000h
SA30	64KB	0B8000h
SA31	64KB	0C0000h
SA32	64KB	0C8000h
SA33	64KB	0D0000h
SA34	64KB	0D8000h
SA35	64KB	0E0000h
SA36	64KB	0E8000h
SA37	64KB	0F0000h
SA38	64KB	0F8000h
SA39	64KB	100000h
SA40	64KB	108000h
SA41	64KB	110000h
SA42	64KB	118000h
SA43	64KB	120000h
SA44	64KB	128000h
SA45	64KB	130000h
SA46	64KB	138000h
SA47	64KB	140000h
SA48	64KB	148000h
SA49	64KB	150000h
SA50	64KB	158000h
SA51	64KB	160000h
SA52	64KB	168000h
SA53	64KB	170000h
SA54	64KB	178000h
SA55	64KB	180000h
SA56	64KB	188000h
SA57	64KB	190000h
SA58	64KB	198000h
SA59	64KB	1A0000h
SA60	64KB	1A8000h
SA61	64KB	1B0000h
SA62	64KB	1B8000h
SA63	64KB	1C0000h
SA64	64KB	1C8000h
SA65	64KB	1D0000h
SA66	64KB	1D8000h
SA67	64KB	1E0000h
SA68	64KB	1E8000h
SA69	64KB	1F0000h
SA70	64KB	1F8000h
		1FFFFFh

BANK B

Sector	Size	Address
SA71	64KB	200000h
SA72	64KB	208000h
SA73	64KB	210000h
SA74	64KB	218000h
SA75	64KB	220000h
SA76	64KB	228000h
SA77	64KB	230000h
SA78	64KB	238000h
SA79	64KB	240000h
SA80	64KB	248000h
SA81	64KB	250000h
SA82	64KB	258000h
SA83	64KB	260000h
SA84	64KB	268000h
SA85	64KB	270000h
SA86	64KB	278000h
SA87	64KB	280000h
SA88	64KB	288000h
SA89	64KB	290000h
SA90	64KB	298000h
SA91	64KB	2A0000h
SA92	64KB	2A8000h
SA93	64KB	2B0000h
SA94	64KB	2B8000h
SA95	64KB	2C0000h
SA96	64KB	2C8000h
SA97	64KB	2D0000h
SA98	64KB	2D8000h
SA99	64KB	2E0000h
SA100	64KB	2E8000h
SA101	64KB	2F0000h
SA102	64KB	2F8000h
SA103	64KB	300000h
SA104	64KB	308000h
SA105	64KB	310000h
SA106	64KB	318000h
SA107	64KB	320000h
SA108	64KB	328000h
SA109	64KB	330000h
SA110	64KB	338000h
SA111	64KB	340000h
SA112	64KB	348000h
SA113	64KB	350000h
SA114	64KB	358000h
SA115	64KB	360000h
SA116	64KB	368000h
SA117	64KB	370000h
SA118	64KB	378000h
SA119	64KB	380000h
SA120	64KB	388000h
SA121	64KB	390000h
SA122	64KB	398000h
SA123	64KB	3A0000h
SA124	64KB	3A8000h
SA125	64KB	3B0000h
SA126	64KB	3B8000h
SA127	64KB	3C0000h
SA128	64KB	3C8000h
SA129	64KB	3D0000h
SA130	64KB	3D8000h
SA131	64KB	3E0000h
SA132	64KB	3E8000h
SA133	64KB	3F0000h
SA134	64KB	3F8000h
		3FFFFFh

BANK C

Sector	Size	Address
SA135	64KB	400000h
SA136	64KB	408000h
SA137	64KB	410000h
SA138	64KB	418000h
SA139	64KB	420000h
SA140	64KB	428000h
SA141	64KB	430000h
SA142	64KB	438000h
SA143	64KB	440000h
SA144	64KB	448000h
SA145	64KB	450000h
SA146	64KB	458000h
SA147	64KB	460000h
SA148	64KB	468000h
SA149	64KB	470000h
SA150	64KB	478000h
SA151	64KB	480000h
SA152	64KB	488000h
SA153	64KB	490000h
SA154	64KB	498000h
SA155	64KB	4A0000h
SA156	64KB	4A8000h
SA157	64KB	4B0000h
SA158	64KB	4B8000h
SA159	64KB	4C0000h
SA160	64KB	4C8000h
SA161	64KB	4D0000h
SA162	64KB	4D8000h
SA163	64KB	4E0000h
SA164	64KB	4E8000h
SA165	64KB	4F0000h
SA166	64KB	4F8000h
SA167	64KB	500000h
SA168	64KB	508000h
SA169	64KB	510000h
SA170	64KB	518000h
SA171	64KB	520000h
SA172	64KB	528000h
SA173	64KB	530000h
SA174	64KB	538000h
SA175	64KB	540000h
SA176	64KB	548000h
SA177	64KB	550000h
SA178	64KB	558000h
SA179	64KB	560000h
SA170	64KB	568000h
SA181	64KB	570000h
SA182	64KB	578000h
SA183	64KB	580000h
SA184	64KB	588000h
SA185	64KB	590000h
SA186	64KB	598000h
SA187	64KB	5A0000h
SA188	64KB	5A8000h
SA189	64KB	5B0000h
SA190	64KB	5B8000h
SA191	64KB	5C0000h
SA192	64KB	5C8000h
SA193	64KB	5D0000h
SA194	64KB	5D8000h
SA195	64KB	5E0000h
SA196	64KB	5E8000h
SA197	64KB	5F0000h
SA198	64KB	5F8000h
		5FFFFFh

BANK C / BANK D

Sector	Size	Address
SA199	64KB	600000h
SA200	64KB	608000h
SA201	64KB	610000h
SA202	64KB	618000h
SA203	64KB	620000h
SA204	64KB	628000h
SA205	64KB	630000h
SA206	64KB	638000h
SA207	64KB	640000h
SA208	64KB	648000h
SA209	64KB	650000h
SA210	64KB	658000h
SA211	64KB	660000h
SA212	64KB	668000h
SA213	64KB	670000h
SA214	64KB	678000h
SA215	64KB	680000h
SA216	64KB	688000h
SA217	64KB	690000h
SA218	64KB	698000h
SA219	64KB	6A0000h
SA220	64KB	6A8000h
SA221	64KB	6B0000h
SA222	64KB	6B8000h
SA223	64KB	6C0000h
SA224	64KB	6C8000h
SA225	64KB	6D0000h
SA226	64KB	6D8000h
SA227	64KB	6E0000h
SA228	64KB	6E8000h
SA229	64KB	6F0000h
SA230	64KB	6F8000h
SA231	64KB	700000h
SA232	64KB	708000h
SA233	64KB	710000h
SA234	64KB	718000h
SA235	64KB	720000h
SA236	64KB	728000h
SA237	64KB	730000h
SA238	64KB	738000h
SA239	64KB	740000h
SA240	64KB	748000h
SA241	64KB	750000h
SA242	64KB	758000h
SA243	64KB	760000h
SA244	64KB	768000h
SA245	64KB	770000h
SA246	64KB	778000h
SA247	64KB	780000h
SA248	64KB	788000h
SA249	64KB	790000h
SA250	64KB	798000h
SA251	64KB	7A0000h
SA252	64KB	7A8000h
SA253	64KB	7B0000h
SA254	64KB	7B8000h
SA255	64KB	7C0000h
SA256	64KB	7C8000h
SA257	64KB	7D0000h
SA258	64KB	7D8000h
SA259	64KB	7E0000h
SA260	64KB	7E8000h
SA261	64KB	7F0000h
SA262	8KB	7F8000h
SA263	8KB	7F9000h
SA264	8KB	7FA000h
SA265	8KB	7FB000h
SA266	8KB	7FC000h
SA267	8KB	7FD000h
SA268	8KB	7FE000h
SA269	8KB	7FF000h
		7FFFFFh

Sector Architecture

• **FlexBank™ Architecture**

Bank Splits	Bank 1		Bank 2	
	Volume	Combination	Volume	Combination
1	16 Mbit	Bank A	112Mbit	Remember (Bank B, C, D)
2	48 Mbit	Bank B	96 Mbit	Remember (Bank A, C, D)
3	48 Mbit	Bank C	96 Mbit	Remember (Bank A, B, D)
4	16 Mbit	Bank D	112Mbit	Remember (Bank A, B, C)

• **Simultaneous Operation**

Case	Bank 1 Status	Bank 2 Status
1	Read mode	Read mode
2	Read mode	Autoselect mode
3	Read mode	Program mode
4	Read mode	Erase mode
5	Autoselect mode	Read mode
6	Program mode	Read mode
7	Erase mode	Read mode

Note : Bank 1 and Bank 2 are divided for the sake of convenience at Simultaneous Operation. Actually, the Bank consists of 4 banks, Bank A, Bank B, BankC and Bank D. Bank Address (BA) meant to specify each of the Banks.

• **Sector Address Tables (Bank A)**

Bank	Sector	Sector Address											Sector Size (Kwords)	(× 16) Address Range
		Bank Address												
		A_{22}	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank A	SA0	0	0	0	0	0	0	0	0	0	0	0	4	000000h to 000FFFh
	SA1	0	0	0	0	0	0	0	0	0	0	1	4	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	0	0	1	0	4	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	0	0	1	1	4	003000h to 003FFFh
	SA4	0	0	0	0	0	0	0	0	1	0	0	4	004000h to 004FFFh
	SA5	0	0	0	0	0	0	0	0	1	0	1	4	005000h to 005FFFh
	SA6	0	0	0	0	0	0	0	0	1	1	0	4	006000h to 006FFFh
	SA7	0	0	0	0	0	0	0	0	1	1	1	4	007000h to 007FFFh
	SA8	0	0	0	0	0	0	0	1	X	X	X	32	008000h to 00FFFFh
	SA9	0	0	0	0	0	0	1	0	X	X	X	32	010000h to 017FFFh
	SA10	0	0	0	0	0	0	1	1	X	X	X	32	018000h to 01FFFFh
	SA11	0	0	0	0	0	1	0	0	X	X	X	32	020000h to 027FFFh
	SA12	0	0	0	0	0	1	0	1	X	X	X	32	028000h to 02FFFFh
	SA13	0	0	0	0	0	1	1	0	X	X	X	32	030000h to 037FFFh
	SA14	0	0	0	0	0	1	1	1	X	X	X	32	038000h to 03FFFFh
	SA15	0	0	0	0	1	0	0	0	X	X	X	32	040000h to 047FFFh
	SA16	0	0	0	0	1	0	0	1	X	X	X	32	048000h to 04FFFFh
	SA17	0	0	0	0	1	0	1	0	X	X	X	32	050000h to 057FFFh
	SA18	0	0	0	0	1	0	1	1	X	X	X	32	058000h to 05FFFFh
	SA19	0	0	0	0	1	1	0	0	X	X	X	32	060000h to 06FFFFh
	SA20	0	0	0	0	1	1	0	1	X	X	X	32	068000h to 06FFFFh
	SA21	0	0	0	0	1	1	1	0	X	X	X	32	070000h to 077FFFh
	SA22	0	0	0	0	1	1	1	1	X	X	X	32	078000h to 07FFFFh
	SA23	0	0	0	1	0	0	0	0	X	X	X	32	080000h to 087FFFh
	SA24	0	0	0	1	0	0	0	1	X	X	X	32	088000h to 08FFFFh
	SA25	0	0	0	1	0	0	1	0	X	X	X	32	090000h to 097FFFh
	SA26	0	0	0	1	0	0	1	1	X	X	X	32	098000h to 09FFFFh
	SA27	0	0	0	1	0	1	0	0	X	X	X	32	0A0000h to 0A7FFFh
	SA28	0	0	0	1	0	1	0	1	X	X	X	32	0A8000h to 0AFFFFh
	SA29	0	0	0	1	0	1	1	0	X	X	X	32	0B0000h to 0B7FFFh
	SA30	0	0	0	1	0	1	1	1	X	X	X	32	0B8000h to 0BFFFFh
	SA31	0	0	0	1	1	0	0	0	X	X	X	32	0C0000h to 0C7FFFh
	SA32	0	0	0	1	1	0	0	1	X	X	X	32	0C8000h to 0CFFFFh
	SA33	0	0	0	1	1	0	1	0	X	X	X	32	0D0000h to 0D7FFFh
	SA34	0	0	0	1	1	0	1	1	X	X	X	32	0D8000h to 0DFFFFh
	SA35	0	0	0	1	1	1	0	0	X	X	X	32	0E0000h to 0E7FFFh
	SA36	0	0	0	1	1	1	0	1	X	X	X	32	0E8000h to 0EFFFFh
	SA37	0	0	0	1	1	1	1	0	X	X	X	32	0F0000h to 0F7FFFh
	SA38	0	0	0	1	1	1	1	1	X	X	X	32	0F8000h to 0FFFFFh

• **Sector Address Tables (Bank B)**

Bank	Sector	Sector Address											Sector Size (Kwords)	(× 16) Address Range
		Bank Address												
		A_{22}	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
	SA39	0	0	1	0	0	0	0	0	X	X	X	32	100000h to 107FFFh
	SA40	0	0	1	0	0	0	0	1	X	X	X	32	108000h to 10FFFFh
	SA41	0	0	1	0	0	0	1	0	X	X	X	32	110000h to 117FFFh
	SA42	0	0	1	0	0	0	1	1	X	X	X	32	118000h to 11FFFFh
	SA43	0	0	1	0	0	1	0	0	X	X	X	32	120000h to 127FFFh
	SA44	0	0	1	0	0	1	0	1	X	X	X	32	128000h to 12FFFFh
	SA45	0	0	1	0	0	1	1	0	X	X	X	32	130000h to 137FFFh
	SA46	0	0	1	0	0	1	1	1	X	X	X	32	138000h to 13FFFFh
	SA47	0	0	1	0	1	0	0	0	X	X	X	32	140000h to 147FFFh
	SA48	0	0	1	0	1	0	0	1	X	X	X	32	148000h to 14FFFFh
	SA49	0	0	1	0	1	0	1	0	X	X	X	32	150000h to 157FFFh
	SA50	0	0	1	0	1	0	1	1	X	X	X	32	158000h to 15FFFFh
	SA51	0	0	1	0	1	1	0	0	X	X	X	32	160000h to 167FFFh
	SA52	0	0	1	0	1	1	0	1	X	X	X	32	168000h to 16FFFFh
	SA53	0	0	1	0	1	1	1	0	X	X	X	32	170000h to 177FFFh
	SA54	0	0	1	0	1	1	1	1	X	X	X	32	178000h to 17FFFFh
	SA55	0	0	1	1	0	0	0	0	X	X	X	32	180000h to 187FFFh
	SA56	0	0	1	1	0	0	0	1	X	X	X	32	188000h to 18FFFFh
	SA57	0	0	1	1	0	0	1	0	X	X	X	32	190000h to 197FFFh
Bank B	SA58	0	0	1	1	0	0	1	1	X	X	X	32	198000h to 19FFFFh
	SA59	0	0	1	1	0	1	0	0	X	X	X	32	1A0000h to 1A7FFFh
	SA60	0	0	1	1	0	1	0	1	X	X	X	32	1A8000h to 1AFFFFh
	SA61	0	0	1	1	0	1	1	0	X	X	X	32	1B0000h to 1B7FFFh
	SA62	0	0	1	1	0	1	1	1	X	X	X	32	1B8000h to 1BFFFFh
	SA63	0	0	1	1	1	0	0	0	X	X	X	32	1C0000h to 1C7FFFh
	SA64	0	0	1	1	1	0	0	1	X	X	X	32	1C8000h to 1CFFFFh
	SA65	0	0	1	1	1	0	1	0	X	X	X	32	1D0000h to 1D7FFFh
	SA66	0	0	1	1	1	0	1	1	X	X	X	32	1D8000h to 1DFFFFh
	SA67	0	0	1	1	1	1	0	0	X	X	X	32	1E0000h to 1E7FFFh
	SA68	0	0	1	1	1	1	0	1	X	X	X	32	1E8000h to 1EFFFFh
	SA69	0	0	1	1	1	1	1	0	X	X	X	32	1F0000h to 1F7FFFh
	SA70	0	0	1	1	1	1	1	1	X	X	X	32	1F8000h to 1FFFFFh
	SA71	0	1	0	0	0	0	0	0	X	X	X	32	200000h to 207FFFh
	SA72	0	1	0	0	0	0	0	1	X	X	X	32	208000h to 20FFFFh
	SA73	0	1	0	0	0	0	1	0	X	X	X	32	210000h to 217FFFh
	SA74	0	1	0	0	0	0	1	1	X	X	X	32	218000h to 21FFFFh
	SA75	0	1	0	0	0	1	0	0	X	X	X	32	220000h to 227FFFh
	SA76	0	1	0	0	0	1	0	1	X	X	X	32	228000h to 22FFFFh
	SA77	0	1	0	0	0	1	1	0	X	X	X	32	230000h to 237FFFh

(Continued)

Bank	Sector	Sector Address											Sector Size (Kwords)	(× 16) Address Range
		Bank Address												
		A_{22}	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
	SA78	0	1	0	0	0	1	1	1	X	X	X	32	238000h to 23FFFFh
	SA79	0	1	0	0	1	0	0	0	X	X	X	32	240000h to 247FFFh
	SA80	0	1	0	0	1	0	0	1	X	X	X	32	248000h to 24FFFFh
	SA81	0	1	0	0	1	0	1	0	X	X	X	32	250000h to 257FFFh
	SA82	0	1	0	0	1	0	1	1	X	X	X	32	258000h to 25FFFFh
	SA83	0	1	0	0	1	1	0	0	X	X	X	32	260000h to 267FFFh
	SA84	0	1	0	0	1	1	0	1	X	X	X	32	268000h to 26FFFFh
	SA85	0	1	0	0	1	1	1	0	X	X	X	32	270000h to 277FFFh
	SA86	0	1	0	0	1	1	1	1	X	X	X	32	278000h to 27FFFFh
	SA87	0	1	0	1	0	0	0	0	X	X	X	32	280000h to 287FFFh
	SA88	0	1	0	1	0	0	0	1	X	X	X	32	288000h to 28FFFFh
	SA89	0	1	0	1	0	0	1	0	X	X	X	32	290000h to 297FFFh
	SA90	0	1	0	1	0	0	1	1	X	X	X	32	298000h to 29FFFFh
	SA91	0	1	0	1	0	1	0	0	X	X	X	32	2A0000h to 2A7FFFh
	SA92	0	1	0	1	0	1	0	1	X	X	X	32	2A8000h to 2AFFFFh
	SA93	0	1	0	1	0	1	1	0	X	X	X	32	2B0000h to 2B7FFFh
	SA94	0	1	0	1	0	1	1	1	X	X	X	32	2B8000h to 2BFFFFh
	SA95	0	1	0	1	1	0	0	0	X	X	X	32	2C0000h to 2C7FFFh
	SA96	0	1	0	1	1	0	0	1	X	X	X	32	2C8000h to 2CFFFFh
Bank B	SA97	0	1	0	1	1	0	1	0	X	X	X	32	2D0000h to 2D7FFFh
	SA98	0	1	0	1	1	0	1	1	X	X	X	32	2D8000h to 2DFFFFh
	SA99	0	1	0	1	1	1	0	0	X	X	X	32	2E0000h to 2E7FFFh
	SA100	0	1	0	1	1	1	0	1	X	X	X	32	2E8000h to 2EFFFFh
	SA101	0	1	0	1	1	1	1	0	X	X	X	32	2F0000h to 2F7FFFh
	SA102	0	1	0	1	1	1	1	1	X	X	X	32	2F8000h to 2FFFFFh
	SA103	0	1	1	0	0	0	0	0	X	X	X	32	300000h to 307FFFh
	SA104	0	1	1	0	0	0	0	1	X	X	X	32	308000h to 30FFFFh
	SA105	0	1	1	0	0	0	1	0	X	X	X	32	310000h to 317FFFh
	SA106	0	1	1	0	0	0	1	1	X	X	X	32	318000h to 31FFFFh
	SA107	0	1	1	0	0	1	0	0	X	X	X	32	320000h to 327FFFh
	SA108	0	1	1	0	0	1	0	1	X	X	X	32	328000h to 32FFFFh
	SA109	0	1	1	0	0	1	1	0	X	X	X	32	330000h to 337FFFh
	SA110	0	1	1	0	0	1	1	1	X	X	X	32	338000h to 33FFFFh
	SA111	0	1	1	0	1	0	0	0	X	X	X	32	340000h to 347FFFh
	SA112	0	1	1	0	1	0	0	1	X	X	X	32	348000h to 34FFFFh
	SA113	0	1	1	0	1	0	1	0	X	X	X	32	350000h to 357FFFh
	SA114	0	1	1	0	1	0	1	1	X	X	X	32	358000h to 35FFFFh
	SA115	0	1	1	0	1	1	0	0	X	X	X	32	360000h to 367FFFh
	SA116	0	1	1	0	1	1	0	1	X	X	X	32	368000h to 36FFFFh

(Continued)

19

(Continued)

Bank	Sector	Sector Address												Sector Size (Kwords)	(× 16) Address Range
		Bank Address													
		A_{22}	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank B	SA117	0	1	1	0	1	1	1	0	X	X	X	32	370000h to 377FFFh
	SA118	0	1	1	0	1	1	1	1	X	X	X	32	378000h to 37FFFFh
	SA119	0	1	1	1	0	0	0	0	X	X	X	32	380000h to 387FFFh
	SA120	0	1	1	1	0	0	0	1	X	X	X	32	388000h to 38FFFFh
	SA121	0	1	1	1	0	0	1	0	X	X	X	32	390000h to 397FFFh
	SA122	0	1	1	1	0	0	1	1	X	X	X	32	398000h to 39FFFFh
	SA123	0	1	1	1	0	1	0	0	X	X	X	32	3A0000h to 3A7FFFh
	SA124	0	1	1	1	0	1	0	1	X	X	X	32	3A8000h to 3AFFFFh
	SA125	0	1	1	1	0	1	1	0	X	X	X	32	3B0000h to 3B7FFFh
	SA126	0	1	1	1	0	1	1	1	X	X	X	32	3B8000h to 3BFFFFh
	SA127	0	1	1	1	1	0	0	0	X	X	X	32	3C0000h to 3C7FFFh
	SA128	0	1	1	1	1	0	0	1	X	X	X	32	3C8000h to 3CFFFFh
	SA129	0	1	1	1	1	0	1	0	X	X	X	32	3D0000h to 3D7FFFh
	SA130	0	1	1	1	1	0	1	1	X	X	X	32	3D8000h to 3DFFFFh
	SA131	0	1	1	1	1	1	0	0	X	X	X	32	3E0000h to 3E7FFFh
	SA132	0	1	1	1	1	1	0	1	X	X	X	32	3E8000h to 3EFFFFh
	SA133	0	1	1	1	1	1	1	0	X	X	X	32	3F0000h to 3F7FFFh
	SA134	0	1	1	1	1	1	1	1	X	X	X	32	3F8000h to 3FFFFFh

• **Sector Address Tables (Bank C)**

Bank	Sector	Sector Address											Sector Size (Kwords)	(× 16) Address Range
		Bank Address			A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
		A_{22}	A_{21}	A_{20}										
Bank C	SA135	1	0	0	0	0	0	0	0	X	X	X	32	400000h to 407FFFh
	SA136	1	0	0	0	0	0	0	1	X	X	X	32	408000h to 40FFFFh
	SA137	1	0	0	0	0	0	1	0	X	X	X	32	410000h to 417FFFh
	SA138	1	0	0	0	0	0	1	1	X	X	X	32	418000h to 41FFFFh
	SA139	1	0	0	0	0	1	0	0	X	X	X	32	420000h to 427FFFh
	SA140	1	0	0	0	0	1	0	1	X	X	X	32	428000h to 42FFFFh
	SA141	1	0	0	0	0	1	1	0	X	X	X	32	430000h to 437FFFh
	SA142	1	0	0	0	0	1	1	1	X	X	X	32	438000h to 43FFFFh
	SA143	1	0	0	0	1	0	0	0	X	X	X	32	440000h to 447FFFh
	SA144	1	0	0	0	1	0	0	1	X	X	X	32	448000h to 44FFFFh
	SA145	1	0	0	0	1	0	1	0	X	X	X	32	450000h to 457FFFh
	SA146	1	0	0	0	1	0	1	1	X	X	X	32	458000h to 45FFFFh
	SA147	1	0	0	0	1	1	0	0	X	X	X	32	460000h to 467FFFh
	SA148	1	0	0	0	1	1	0	1	X	X	X	32	468000h to 46FFFFh
	SA149	1	0	0	0	1	1	1	0	X	X	X	32	470000h to 477FFFh
	SA150	1	0	0	0	1	1	1	1	X	X	X	32	478000h to 47FFFFh
	SA151	1	0	0	1	0	0	0	0	X	X	X	32	480000h to 487FFFh
	SA152	1	0	0	1	0	0	0	1	X	X	X	32	488000h to 48FFFFh
	SA153	1	0	0	1	0	0	1	0	X	X	X	32	490000h to 497FFFh
	SA154	1	0	0	1	0	0	1	1	X	X	X	32	498000h to 49FFFFh
	SA155	1	0	0	1	0	1	0	0	X	X	X	32	4A0000h to 4A7FFFh
	SA156	1	0	0	1	0	1	0	1	X	X	X	32	4A8000h to 4AFFFFh
	SA157	1	0	0	1	0	1	1	0	X	X	X	32	4B0000h to 4B7FFFh
	SA158	1	0	0	1	0	1	1	1	X	X	X	32	4B8000h to 4BFFFFh
	SA159	1	0	0	1	1	0	0	0	X	X	X	32	4C0000h to 4C7FFFh
	SA160	1	0	0	1	1	0	0	1	X	X	X	32	4C8000h to 4CFFFFh
	SA161	1	0	0	1	1	0	1	0	X	X	X	32	4D0000h to 4D7FFFh
	SA162	1	0	0	1	1	0	1	1	X	X	X	32	4D8000h to 4DFFFFh
	SA163	1	0	0	1	1	1	0	0	X	X	X	32	4E0000h to 4E7FFFh
	SA164	1	0	0	1	1	1	0	1	X	X	X	32	4E8000h to 4EFFFFh
	SA165	1	0	0	1	1	1	1	0	X	X	X	32	4F0000h to 4F7FFFh
	SA166	1	0	0	1	1	1	1	1	X	X	X	32	4F8000h to 4FFFFFh
	SA167	1	0	1	0	0	0	0	0	X	X	X	32	500000h to 507FFFh
	SA168	1	0	1	0	0	0	0	1	X	X	X	32	508000h to 50FFFFh
	SA169	1	0	1	0	0	0	1	0	X	X	X	32	510000h to 517FFFh
	SA170	1	0	1	0	0	0	1	1	X	X	X	32	518000h to 51FFFFh
	SA171	1	0	1	0	0	1	0	0	X	X	X	32	520000h to 527FFFh
	SA172	1	0	1	0	0	1	0	1	X	X	X	32	528000h to 52FFFFh
	SA173	1	0	1	0	0	1	1	0	X	X	X	32	530000h to 537FFFh

(Continued)

21

Bank	Sector	Sector Address											Sector Size (Kwords)	(× 16) Address Range
		Bank Address												
		A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12		
Bank C	SA174	1	0	1	0	0	1	1	1	X	X	X	32	538000h to 53FFFFh
	SA175	1	0	1	0	1	0	0	0	X	X	X	32	540000h to 547FFFh
	SA176	1	0	1	0	1	0	0	1	X	X	X	32	548000h to 54FFFFh
	SA177	1	0	1	0	1	0	1	0	X	X	X	32	550000h to 557FFFh
	SA178	1	0	1	0	1	0	1	1	X	X	X	32	558000h to 55FFFFh
	SA179	1	0	1	0	1	1	0	0	X	X	X	32	560000h to 567FFFh
	SA180	1	0	1	0	1	1	0	1	X	X	X	32	568000h to 56FFFFh
	SA181	1	0	1	0	1	1	1	0	X	X	X	32	570000h to 577FFFh
	SA182	1	0	1	0	1	1	1	1	X	X	X	32	578000h to 57FFFFh
	SA183	1	0	1	1	0	0	0	0	X	X	X	32	580000h to 587FFFh
	SA184	1	0	1	1	0	0	0	1	X	X	X	32	588000h to 58FFFFh
	SA185	1	0	1	1	0	0	1	0	X	X	X	32	590000h to 597FFFh
	SA186	1	0	1	1	0	0	1	1	X	X	X	32	598000h to 59FFFFh
	SA187	1	0	1	1	0	1	0	0	X	X	X	32	5A0000h to 5A7FFFh
	SA188	1	0	1	1	0	1	0	1	X	X	X	32	5A8000h to 5AFFFFh
	SA189	1	0	1	1	0	1	1	0	X	X	X	32	5B0000h to 5B7FFFh
	SA190	1	0	1	1	0	1	1	1	X	X	X	32	5B8000h to 5BFFFFh
	SA191	1	0	1	1	1	0	0	0	X	X	X	32	5C0000h to 5C7FFFh
	SA192	1	0	1	1	1	0	0	1	X	X	X	32	5C8000h to 5CFFFFh
	SA193	1	0	1	1	1	0	1	0	X	X	X	32	6D0000h to 5D7FFFh
	SA194	1	0	1	1	1	0	1	1	X	X	X	32	6D8000h to 5DFFFFh
	SA195	1	0	1	1	1	1	0	0	X	X	X	32	5E0000h to 5E7FFFh
	SA196	1	0	1	1	1	1	0	1	X	X	X	32	5E8000h to 5EFFFFh
	SA197	1	0	1	1	1	1	1	0	X	X	X	32	5F0000h to 5F7FFFh
	SA198	1	0	1	1	1	1	1	1	X	X	X	32	5F8000h to 5FFFFFh
	SA199	1	1	0	0	0	0	0	0	X	X	X	32	600000h to 607FFFh
	SA200	1	1	0	0	0	0	0	1	X	X	X	32	608000h to 60FFFFh
	SA201	1	1	0	0	0	0	1	0	X	X	X	32	610000h to 617FFFh
	SA202	1	1	0	0	0	0	1	1	X	X	X	32	618000h to 61FFFFh
	SA203	1	1	0	0	0	1	0	0	X	X	X	32	620000h to 627FFFh
	SA204	1	1	0	0	0	1	0	1	X	X	X	32	628000h to 62FFFFh
	SA205	1	1	0	0	0	1	1	0	X	X	X	32	630000h to 637FFFh
	SA206	1	1	0	0	0	1	1	1	X	X	X	32	638000h to 63FFFFh
	SA207	1	1	0	0	1	0	0	0	X	X	X	32	640000h to 647FFFh
	SA208	1	1	0	0	1	0	0	1	X	X	X	32	648000h to 64FFFFh
	SA209	1	1	0	0	1	0	1	0	X	X	X	32	650000h to 657FFFh
	SA210	1	1	0	0	1	0	1	1	X	X	X	32	658000h to 65FFFFh
	SA211	1	1	0	0	1	1	0	0	X	X	X	32	660000h to 667FFFh
	SA212	1	1	0	0	1	1	0	1	X	X	X	32	668000h to 66FFFFh

(Continued)

(Continued)

Bank	Sector	Sector Address											Sector Size (Kwords)	(× 16) Address Range
		Bank Address												
		A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12		
Bank C	SA213	1	1	0	0	1	1	1	0	X	X	X	32	670000h to 677FFFh
	SA214	1	1	0	0	1	1	1	1	X	X	X	32	678000h to 67FFFFh
	SA215	1	1	0	1	0	0	0	0	X	X	X	32	680000h to 687FFFh
	SA216	1	1	0	1	0	0	0	1	X	X	X	32	688000h to 68FFFFh
	SA217	1	1	0	1	0	0	1	0	X	X	X	32	690000h to 697FFFh
	SA218	1	1	0	1	0	0	1	1	X	X	X	32	698000h to 69FFFFh
	SA219	1	1	0	1	0	1	0	0	X	X	X	32	6A0000h to 6A7FFFh
	SA220	1	1	0	1	0	1	0	1	X	X	X	32	6A8000h to 6AFFFFh
	SA221	1	1	0	1	0	1	1	0	X	X	X	32	6B0000h to 6B7FFFh
	SA222	1	1	0	1	0	1	1	1	X	X	X	32	8B8000h to 6BFFFFh
	SA223	1	1	0	1	1	0	0	0	X	X	X	32	6C0000h to 6C7FFFh
	SA224	1	1	0	1	1	0	0	1	X	X	X	32	6C8000h to 6CFFFFh
	SA225	1	1	0	1	1	0	1	0	X	X	X	32	6D0000h to 6D7FFFh
	SA226	1	1	0	1	1	0	1	1	X	X	X	32	6D8000h to 6DFFFFh
	SA227	1	1	0	1	1	1	0	0	X	X	X	32	6E0000h to 6E7FFFh
	SA228	1	1	0	1	1	1	0	1	X	X	X	32	6E8000h to 6EFFFFh
	SA229	1	1	0	1	1	1	1	0	X	X	X	32	6F0000h to 6F7FFFh
	SA230	1	1	0	1	1	1	1	1	X	X	X	32	6F8000h to 6FFFFFh

23

• **Sector Address Tables (Bank D)**

Bank	Sector	Sector Address											Sector Size (Kwords)	(× 16) Address Range
		Bank Address												
		A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12		
Bank D	SA231	1	1	1	0	0	0	0	0	X	X	X	32	700000h to 707FFFh
	SA232	1	1	1	0	0	0	0	1	X	X	X	32	708000h to 70FFFFh
	SA233	1	1	1	0	0	0	1	0	X	X	X	32	710000h to 717FFFh
	SA234	1	1	1	0	0	0	1	1	X	X	X	32	718000h to 71FFFFh
	SA235	1	1	1	0	0	1	0	0	X	X	X	32	720000h to 727FFFh
	SA236	1	1	1	0	0	1	0	1	X	X	X	32	728000h to 72FFFFh
	SA237	1	1	1	0	0	1	1	0	X	X	X	32	730000h to 737FFFh
	SA238	1	1	1	0	0	1	1	1	X	X	X	32	738000h to 73FFFFh
	SA239	1	1	1	0	1	0	0	0	X	X	X	32	740000h to 747FFFh
	SA240	1	1	1	0	1	0	0	1	X	X	X	32	748000h to 74FFFFh
	SA241	1	1	1	0	1	0	1	0	X	X	X	32	750000h to 757FFFh
	SA242	1	1	1	0	1	0	1	1	X	X	X	32	758000h to 75FFFFh
	SA243	1	1	1	0	1	1	0	0	X	X	X	32	760000h to 767FFFh
	SA244	1	1	1	0	1	1	0	1	X	X	X	32	768000h to 76FFFFh
	SA245	1	1	1	0	1	1	1	0	X	X	X	32	770000h to 777FFFh
	SA246	1	1	1	0	1	1	1	1	X	X	X	32	778000h to 77FFFFh
	SA247	1	1	1	1	0	0	0	0	X	X	X	32	780000h to 787FFFh
	SA248	1	1	1	1	0	0	0	1	X	X	X	32	788000h to 78FFFFh
	SA249	1	1	1	1	0	0	1	0	X	X	X	32	790000h to 797FFFh
	SA250	1	1	1	1	0	0	1	1	X	X	X	32	798000h to 79FFFFh
	SA251	1	1	1	1	0	1	0	0	X	X	X	32	7A0000h to 7A7FFFh
	SA252	1	1	1	1	0	1	0	1	X	X	X	32	7A8000h to 7AFFFFh
	SA253	1	1	1	1	0	1	1	0	X	X	X	32	7B0000h to 7B7FFFh
	SA254	1	1	1	1	0	1	1	1	X	X	X	32	7B8000h to 7BFFFFh
	SA255	1	1	1	1	1	0	0	0	X	X	X	32	7C0000h to 7C7FFFh
	SA256	1	1	1	1	1	0	0	1	X	X	X	32	7C8000h to 7CFFFFh
	SA257	1	1	1	1	1	0	1	0	X	X	X	32	7D0000h to 7D7FFFh
	SA258	1	1	1	1	1	0	1	1	X	X	X	32	7D8000h to 7DFFFFh
	SA259	1	1	1	1	1	1	0	0	X	X	X	32	7E0000h to 7E7FFFh
	SA260	1	1	1	1	1	1	0	1	X	X	X	32	7E8000h to 7EFFFFh
	SA261	1	1	1	1	1	1	1	0	X	X	X	32	7F0000h to 7F7FFFh
	SA262	1	1	1	1	1	1	1	1	0	0	0	4	7F8000h to 7F8FFFh
	SA263	1	1	1	1	1	1	1	1	0	0	1	4	7F9000h to 7F9FFFh
	SA264	1	1	1	1	1	1	1	1	0	1	0	4	7FA000h to 7FAFFFh
	SA265	1	1	1	1	1	1	1	1	0	1	1	4	7FB000h to 7FBFFFh
	SA266	1	1	1	1	1	1	1	1	1	0	0	4	7FC000h to 7FCFFFh
	SA267	1	1	1	1	1	1	1	1	1	0	1	4	7FD000h to 7FDFFFh
	SA268	1	1	1	1	1	1	1	1	1	1	0	4	7FE000h to 7FEFFFh
	SA269	1	1	1	1	1	1	1	1	1	1	1	4	7FF000h to 7FFFFFh

• **Sector Group Address Table**

Sector Group	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	Sectors
SGA0	0	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	0	0	1	X	X	X	SA8
SGA9	0	0	0	0	0	0	1	0	X	X	X	SA9
SGA10	0	0	0	0	0	0	1	1	X	X	X	SA10
SGA11	0	0	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA12	0	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA13	0	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA14	0	0	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA15	0	0	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA16	0	0	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA17	0	0	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA18	0	0	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA19	0	0	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA20	0	0	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA21	0	0	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA22	0	0	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA23	0	0	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA24	0	0	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA25	0	0	1	1	1	1	X	X	X	X	X	SA67 to SA70
SGA26	0	1	0	0	0	0	X	X	X	X	X	SA71 to SA74
SGA27	0	1	0	0	0	1	X	X	X	X	X	SA75 to SA78

(Continued)

Sector Group	A_{22}	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA28	0	1	0	0	1	0	X	X	X	X	X	SA79 to SA82
SGA29	0	1	0	0	1	1	X	X	X	X	X	SA83 to SA86
SGA30	0	1	0	1	0	0	X	X	X	X	X	SA87 to SA90
SGA31	0	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA32	0	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA33	0	1	0	1	1	1	X	X	X	X	X	SA99 to SA102
SGA34	0	1	1	0	0	0	X	X	X	X	X	SA103 to SA106
SGA35	0	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA36	0	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA37	0	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA38	0	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA39	0	1	1	1	0	1	X	X	X	X	X	SA123 to SA126
SGA40	0	1	1	1	1	0	X	X	X	X	X	SA127 to SA130
SGA41	0	1	1	1	1	1	X	X	X	X	X	SA131 to SA134
SGA42	1	0	0	0	0	0	X	X	X	X	X	SA135 to SA138
SGA43	1	0	0	0	0	1	X	X	X	X	X	SA139 to SA142
SGA44	1	0	0	0	1	0	X	X	X	X	X	SA143 to SA146
SGA45	1	0	0	0	1	1	X	X	X	X	X	SA147 to SA150
SGA46	1	0	0	1	0	0	X	X	X	X	X	SA151 to SA154
SGA47	1	0	0	1	0	1	X	X	X	X	X	SA155 to SA158
SGA48	1	0	0	1	1	0	X	X	X	X	X	SA159 to SA162
SGA49	1	0	0	1	1	1	X	X	X	X	X	SA163 to SA166
SGA50	1	0	1	0	0	0	X	X	X	X	X	SA167 to SA170
SGA51	1	0	1	0	0	1	X	X	X	X	X	SA171 to SA174

(Continued)

(Continued)

Sector Group	A_{22}	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA52	1	0	1	0	1	0	X	X	X	X	X	SA175 to SA178
SGA53	1	0	1	0	1	1	X	X	X	X	X	SA179 to SA182
SGA54	1	0	1	1	0	0	X	X	X	X	X	SA183 to SA186
SGA55	1	0	1	1	0	1	X	X	X	X	X	SA187 to SA190
SGA56	1	0	1	1	1	0	X	X	X	X	X	SA191 to SA194
SGA57	1	0	1	1	1	1	X	X	X	X	X	SA195 to SA198
SGA58	1	1	0	0	0	0	X	X	X	X	X	SA199 to SA202
SGA59	1	1	0	0	0	1	X	X	X	X	X	SA203 to SA206
SGA60	1	1	0	0	1	0	X	X	X	X	X	SA207 to SA210
SGA61	1	1	0	0	1	1	X	X	X	X	X	SA211 to SA214
SGA62	1	1	0	1	0	0	X	X	X	X	X	SA215 to SA218
SGA63	1	1	0	1	0	1	X	X	X	X	X	SA219 to SA222
SGA64	1	1	0	1	1	0	X	X	X	X	X	SA223 to SA226
SGA65	1	1	0	1	1	1	X	X	X	X	X	SA227 to SA230
SGA66	1	1	1	0	0	0	X	X	X	X	X	SA231 to SA234
SGA67	1	1	1	0	0	1	X	X	X	X	X	SA235 to SA238
SGA68	1	1	1	0	1	0	X	X	X	X	X	SA239 to SA242
SGA69	1	1	1	0	1	1	X	X	X	X	X	SA243 to SA246
SGA70	1	1	1	1	0	0	X	X	X	X	X	SA247 to SA250
SGA71	1	1	1	1	0	1	X	X	X	X	X	SA251 to SA254
SGA72	1	1	1	1	1	0	X	X	X	X	X	SA255 to SA258
SGA73	1	1	1	1	1	1	0	0	X	X	X	SA259
SGA74	1	1	1	1	1	1	0	1	X	X	X	SA260
SGA75	1	1	1	1	1	1	1	0	X	X	X	SA261
SGA76	1	1	1	1	1	1	1	1	0	0	0	SA262
SGA77	1	1	1	1	1	1	1	1	0	0	1	SA263
SGA78	1	1	1	1	1	1	1	1	0	1	0	SA264
SGA79	1	1	1	1	1	1	1	1	0	1	1	SA265
SGA80	1	1	1	1	1	1	1	1	1	0	0	SA266
SGA81	1	1	1	1	1	1	1	1	1	0	1	SA267
SGA82	1	1	1	1	1	1	1	1	1	1	0	SA268
SGA83	1	1	1	1	1	1	1	1	1	1	1	SA269

• **Sector Protection Verify Autoselect Codes Table**

Type	A$_{22}$ to A$_{12}$	A$_7$	A$_6$	A$_5$	A$_4$	A$_3$	A$_2$	A$_1$	A$_0$	Code (HEX)
Manufacture's Code	BA	L	L	L	L	L	L	L	L	04h
Device Code	BA	L	L	L	L	L	L	L	H	227Eh
Extended Device Code *2	BA	L	L	L	L	H	H	H	L	2218h
	BA	L	L	L	L	H	H	H	H	2200h
Sector Group Protection	Sector Group Addresses	L	L	L	L	L	L	H	L	01h*1
Indicator Bits	BA	L	L	L	L	L	L	H	H	DQ$_7$ - Factory Lock Bit 1 = Locked, 0 = Not Locked DQ$_6$ - Customer Lock Bit 1 = Locked, 0 = Not Locked

Legend : L = V$_{IL}$, H = V$_{IH}$. See DC Characteristics for voltage levels.

*1 : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*2 : A read cycle at address (BA) 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes, will be required. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh.

28

• **Flash Memory Command Definitions**

Command Sequence	Bus Write Cy-cles Req'd	First Bus Write Cycle		Second Write Cycle		Third Write Cycle		Fourth Write Cycle		Fifth Write Cycle		Sixth Write Cycle		Seventh Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read / Reset	1	XXXh	F0h	RA	RD	—	—	—	—	—	—	—	—	—	—
Read / Reset	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h	—	—
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h	—	—
Erase Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—	—	—
Erase Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—	—	—
Fast Program	2	XXXh	A0	PA	PD									—	—
Reset from Fast Mode *1	2	BA	90h	XXXh	F0h*2	—	—	—	—	—	—	—	—	—	—
Set Burst Mode Configuration Register	3	555h	AAh	2AAh	55h	(CR) 555h	C0h	—	—	—	—	—	—	—	—
Query	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—	—	—
HiddenROM Entry	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—	—	—
HiddenROM Program*3	4	555h	AAh	2AAh	55h	555h	A0h	(HRA) PA	PD	—	—	—	—	—	—
HiddenROM Exit*3	4	555h	AAh	2AAh	55h	555h	90h	XXXh	00h	—	—	—	—	—	—
HiddenROM Protect*3	6	555h	AAh	2AAh	55h	555h	60h	OPBP	68h	OPBP	48h	XXXh	RD(0)	—	—

Legend :

RA = Address of the memory location to be read.

PA = Address of the memory location to be programmed. Addresses latch on the rising edge of the $\overline{\text{ADV}}$ pulse or active edge of CLK while $\overline{\text{ADV}}$ = V_{IL} whichever comes first or falling edge of wirte pulse while $\overline{\text{ADV}}$ = $V_{IL.}$

SA = Address of the sector to be erased. The combination of A_{22}, A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.

BA = Bank Address. Address setted by A_{22}, A_{21}, A_{20} will select Bank A, Bank B, Bank C and Bank D.

RD = Data read from location RA during read operation.

PD = Data to be programmed at location PA. Data latches on the rising edge of write pulse.

SGA = Sector group address to be protected.

HRA = Address of the HiddenROM area 000000h to 00007Fh

HRBA = Bank Address of the HiddenROM area (A_{22} = A_{21} = A_{20} = A_{19} = A_{18} = V_{IL})

(Continued)

29

(Continued)
RD (0) = Read Data bit. If programmed, $DQ_0 = 1$, if erase, $DQ_0 = 0$
OPBP = (A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (0, 0, 0, 1, 1, 0, 1, 0)
CR = Configuration Register address bits A_{19} to A_{12}.

*1: This command is valid during Fast Mode.

*2: This command is valid during HiddenROM mode.

*3: The data "00h" is also acceptable.

Notes : • Address bits A_{22} to A_{11} = X = "H" or "L" for all address commands except for PA, SA, BA, SGA, OPBP.
        • Bus operations are defined in "■ DEVICE BUS OPERATIONS".
        • Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

2. AC Characteristics
• Synchronous/Burst Read

Parameter	Symbol		Value		Unit
	JEDEC	Standard	Min	Max	
Latency	—	t_{IACC}	—	71	ns
Burst Access Time Valid Clock to Output Delay	—	t_{BACC}	—	11	ns
Address Setup Time to CLK*1	—	t_{ACS}	4	—	ns
Address Hold Time from CLK*2	—	t_{ACH}	6	—	ns
Data Hold Time from Next Clock Cycle	—	t_{BDH}	3	—	ns
Chip Enable to RY/$\overline{BY}$ Valid	—	t_{CR}	—	11	ns
Output Enable to Output Valid	—	t_{OE}	—	11	ns
Chip Enable to High-Z	—	t_{CEZ}	—	8	ns
Output Enable to High-Z	—	t_{OEZ}	—	8	ns
$\overline{CE}$f Setup Time to CLK	—	t_{CES}	4	—	ns
Ready Access Time from CLK	—	t_{RACC}	—	11	ns
$\overline{CE}$f Setup Time to $\overline{ADV}$	—	t_{CAS}	0	—	ns
$\overline{ADV}$ Set Up Time to CLK	—	t_{AVSC}	4	—	ns
$\overline{ADV}$ Hold Time to CLK	—	t_{AVHC}	6	—	ns
CLK to access resume	—	t_{CKA}	—	11	ns
CLK to High-Z	—	t_{CKZ}	—	8	ns
Output Enable Setup Time	—	t_{OES}	4	—	ns
Read Cycle for Continuous suspend	—	t_{RCC}	—	1	ms
Read Cycle Time	—	t_{RC}	56	—	ns

*1 : Access Time is from the last of either stable addresses .

*2 : Addresses are latched on the active edge of CLK.

Note : Test Conditions
Output Load : V_{CCQ}r =1.65 V to 1.95 V : 30 pF
Input rise and fall times : 5 ns
Input pulse levels : 0.0 V to V_{CC}f
Timing measurement reference level : Input : $0.5 \times V_{CC}$f, Output : $0.5 \times V_{CC}$f

• **Asynchronous Read**

Parameter	Symbol		Value		Unit
	JEDEC	Standard	Min	Max	
Read Cycle Time	—	t_{RC}	56	—	ns
Access Time from $\overline{CE}$f Low	—	t_{CE}	—	56	ns
Asynchronous Access Time*	—	t_{ACC}	—	56	ns
Output Enable to Output Valid	—	t_{OE}	—	11	ns
Output Enable Hold Time — Read	—	t_{OEH}	0	—	ns
Output Enable Hold Time — Toggle and $\overline{Data}$ Polling			8	—	ns
Chip Enable to High-Z	—	t_{CEZ}	—	8	ns
$\overline{CE}$f High During Toggle Bit Polling	—	t_{CEPH}	20	—	ns
Output Enable to High-Z	—	t_{OEZ}	—	8	ns

* : Asynchronous Access Time is from the last of either stable addresses or the falling edge of $\overline{ADV}$.

• **Hardware Reset ($\overline{RESET}$)**

Parameter	Symbol		Value		Unit
	JEDEC	Standard	Min	Max	
$\overline{RESET}$ Pin Low (During Embedded Algorithms) to Read Mode *1	—	t_{READY}	—	20	μs
$\overline{RESET}$ Pulse Width	—	t_{RP}	500	—	ns
Reset High Time Before Read *2	—	t_{RH}	200	—	ns
Power On/Off Time	—	t_{PS}	0	—	ns

*1 : Access Time is from the last of either stable addresses.

*2 : Addresses are latched on the active edge of CLK.

Note : Test Conditions :
  Output Load : V_{CCQ}r =1.65 V to 1.95 V : 30 pF
  Input rise and fall times : 5 ns
  Input pulse levels : 0.0 V to V_{CC}f
  Timing measurement reference level : Input : $0.5 \times V_{CC}$f, Output : $0.5 \times V_{CC}$f

• **Write (Erase/Program) Operations**

Parameter	Symbol		Value			Unit
	JEDEC	Standard	Min	Typ	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	56	—	—	ns
Address Setup Time	t_{AVWL}	t_{AS}	0	—	—	ns
Address Hold Time	t_{WLAX}	t_{AH}	20	—	—	ns
$\overline{ADV}$ Low Time	—	t_{AVDP}	10	—	—	ns
$\overline{CE}$f Low to $\overline{ADV}$ High	—	t_{CLAH}	10	—	—	ns
Data Setup Time	t_{DVWH}	t_{DS}	20	—	—	ns
Data Hold Time	t_{WHDX}	t_{DH}	0	—	—	ns
Read Recovery Time Before Write	t_{GHWL}	t_{GHWL}	0	—	—	ns
$\overline{CE}$f Hold Time	t_{WHEH}	t_{CH}	0	—	—	ns
Write Pulse Width	t_{EHWH}	t_{WP}	20	—	—	ns
Write Pulse Width High	t_{WHWL}	t_{WPH}	20	—	—	ns
Latency Between Read and Write Operations	—	$t_{SR/W}$	0	—	—	ns
Programming Operation[1]	t_{WHWH1}	t_{WHWH1}	—	6	—	µs
Sector Erase Operation[1, 2]	t_{WHWH2}	t_{WHWH2}	—	0.5	—	s
V_{CC}f Setup Time	—	t_{VCS}	50	—	—	µs
$\overline{CE}$f Setup Time to $\overline{WE}$	t_{ELWL}	t_{CS}	0	—	—	ns
$\overline{ADV}$ Set Up Time to CLK	—	t_{AVSC}	4	—	—	ns
$\overline{ADV}$ Hold Time to CLK	—	t_{AVHC}	6	—	—	ns
$\overline{ADV}$ Setup Time to $\overline{WE}$	—	t_{AVSW}	4	—	—	ns
$\overline{ADV}$ Hold Time to $\overline{WE}$	—	t_{AVHW}	6	—	—	ns
Address Setup Time to CLK	—	t_{ACS}	4	—	—	ns
Address Hold Time to CLK	—	t_{ACH}	6	—	—	ns
Address Setup Time to $\overline{ADV}$	—	t_{AAS}	4	—	—	ns
Address Hold Time to $\overline{ADV}$		t_{AAH}	6	—	—	ns
$\overline{WE}$ Low to CLK	—	t_{WLC}	0	—	—	ns
$\overline{ADV}$ High to $\overline{WE}$ Low	—	t_{AHWL}	5	—	—	ns
CLK to $\overline{WE}$ Low	—	t_{CWL}	5	—	—	ns
Erase Time-out TIme	—	t_{TOW}	50	—	—	µs

[1] : Not 100% tested.

[2] : See the "Erase and Programming Performance" section in "BS12DH" datasheet for more information.

Notes : • Does not include the preprogramming time.
        • Access Time is from the last of either stable addresses.
        • Addresses are latched on the active edge of CLK.

• **Erase and Programming Performance**

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector Erase Time	—	0.5	2	s	Excludes programming prior to erasure
Word Programming Time	—	6.0	100	µs	Excludes system level overhead
Chip Programming Time	—	50.3	200	s	Excludes system level overhead
Erase/Program Cycle	100,000	—	—	cycle	—

Notes : • Typical Erase Conditions : T$_A$ = +25°C, V$_{CC}$f = 1.8 V
      • Typical Program Conditions : T$_A$ = +25°C, V$_{CC}$f = 1.8 V, Data = checker
      • Test Conditions :
         Output Load : V$_{CCQ}$r =1.65 V to 1.95 V : 30 pF
         Input rise and fall times : 5 ns
         Input pulse levels : 0.0 V to V$_{CC}$f
         Timing measurement reference level : Input: 0.5 × V$_{CC}$f, Output : 0.5 × V$_{CC}$f

• **Synchronous Burst Mode Read (Latched By Rising Active CLK)**

7 cycles for initial access shown.

Notes : • Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles.
       • The device is in synchronous mode.
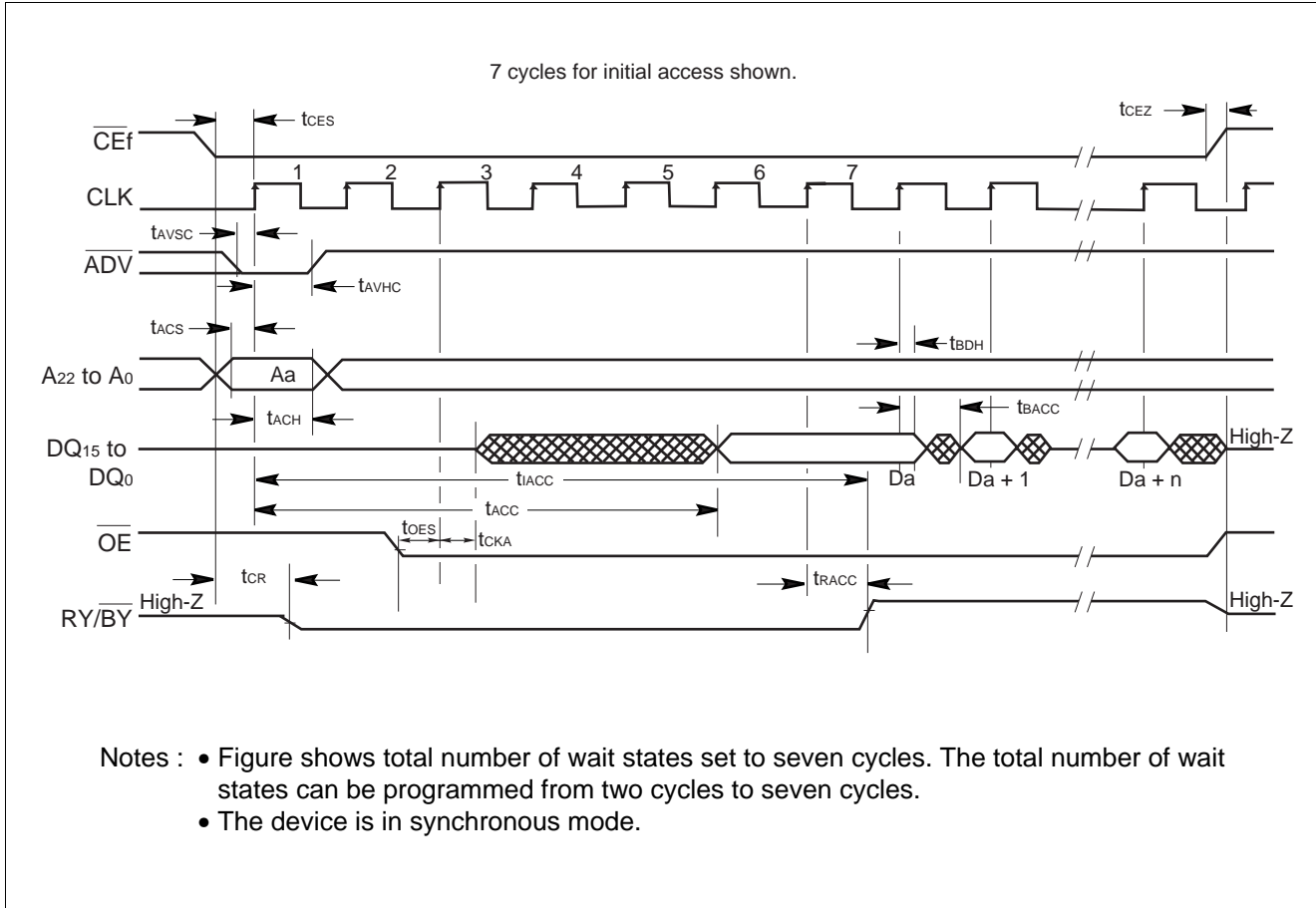
• **Synchronous Burst Mode Read (Latched By Falling Active CLK)**

4 cycles for initial access shown.
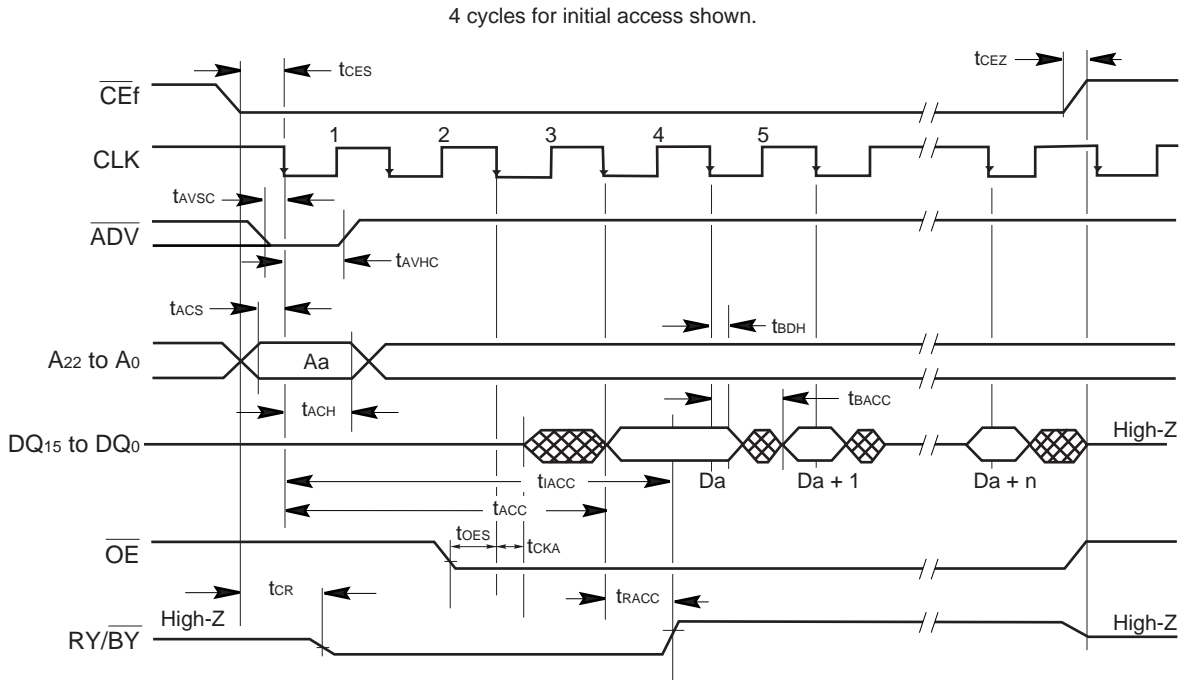
Notes : • Figure shows total number of wait states set to four cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active falling edge.
 • The device is in synchronous mode.

• **8-word Linear Burst**

Note : Figure assumes 7 wait states for initial access, synchronous read. D_0 to D_7 in data waveform indicate the order of data within a given 8-word address range, from lowest to highest. See "Requirements for Synchronous (Burst) Read Operation". The Set Configuration Register command sequence has been written with $A_{18} = 1$; device will output RY/$\overline{BY}$ with valid data.
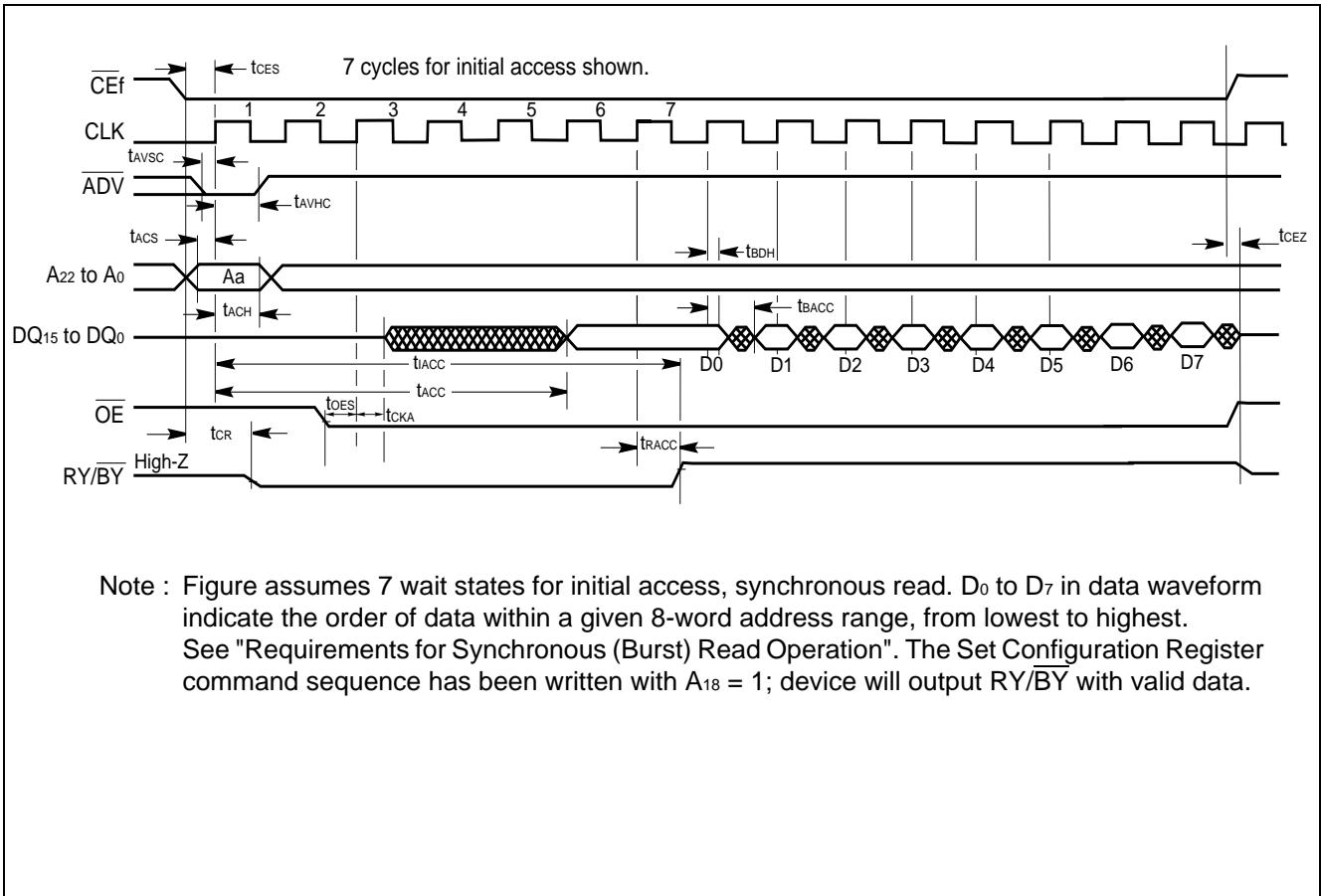
• **8-word Linear Burst with Wrap Around**
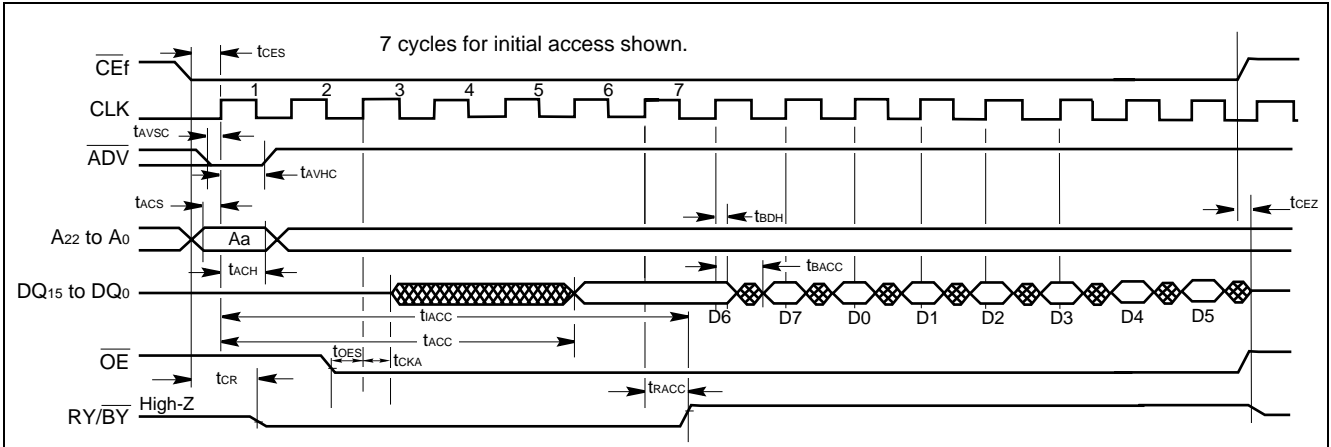
Note : Figure assumes 7 wait states for initial access, synchronous read. D_0 to D_7 in data waveform indicate the order of data within a given 8-word address range, from lowest to highest. Starting address in figure is the 7th address in range (A_6). See "Requirements for Synchronous (Burst) Read Operation". The Set Configuration Register command sequence has been written with $A_{18} = 1$; device will output RY/$\overline{BY}$ with valid data.

• **Linear Burst with RY/BY Set One Cycle Before Data**

6 wait cycles for initial access shown.

Note : Figure assumes 6 wait states for initial access, 66 MHz clock, and synchronous read.
The Set Configuration Register command sequence has been written with $A_{18} = 0$; device
will output RY/BY one cycle before valid data.

• **Burst Suspend**

Note : The Set Configuration Register command sequence must be written with A_{18} =1; device will output RY/$\overline{BY}$ with valid data. The clock during Burst Suspend is "Don't care".

• **Burst Suspend prior to Initial Access**
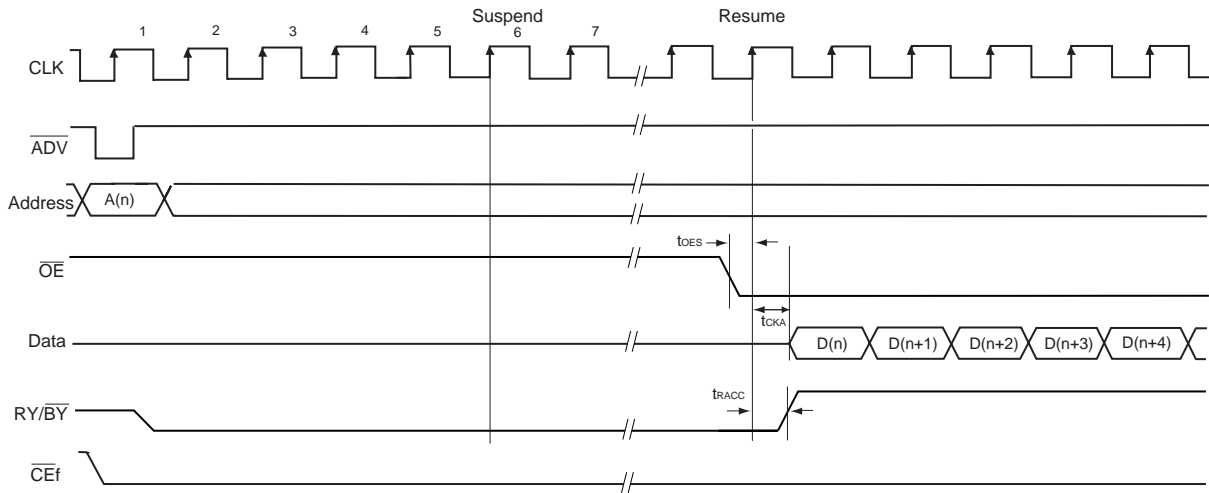
Note : Figure assumes 6 wait states for initial access and synchronous read. The Set Configuration Register command sequence must be written with A_{18}=1; device will output RY/$\overline{BY}$ with valid data. The clock during Burst Suspend is "Don't care".

41

• **Read Cycle for Continuous Suspend**
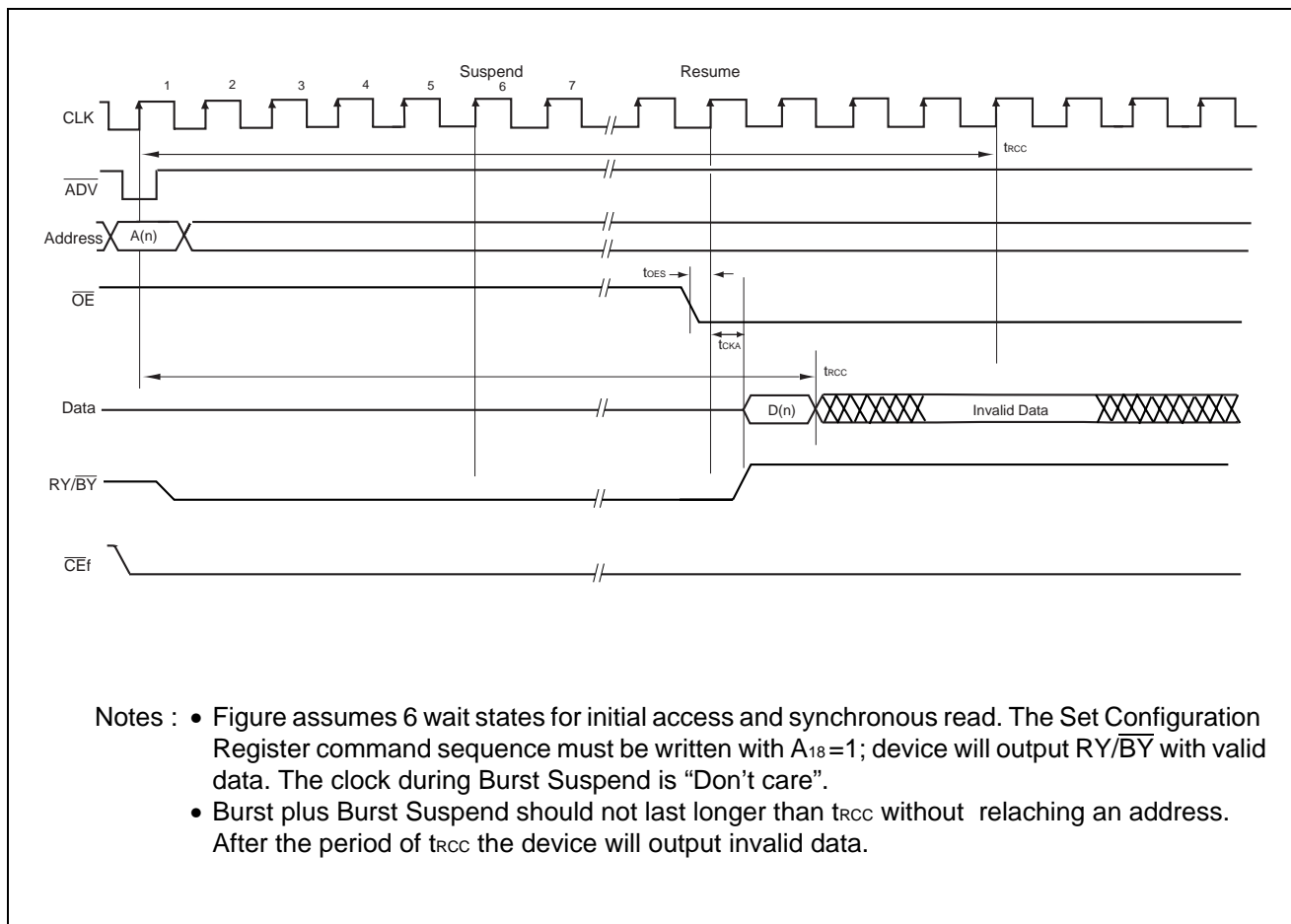
Notes : • Figure assumes 6 wait states for initial access and synchronous read. The Set Configuration Register command sequence must be written with $A_{18}=1$; device will output RY/$\overline{BY}$ with valid data. The clock during Burst Suspend is "Don't care".
• Burst plus Burst Suspend should not last longer than t_{RCC} without relaching an address. After the period of t_{RCC} the device will output invalid data.

• **Asynchronous Mode Read**

Address

Address Stable

t_{RC}

t_{ACC}

$\overline{CEf}$

$\overline{OE}$

t_{OE}

t_{CEZ}

t_{OEZ}

t_{OEH}

$\overline{WE}$

t_{CE}

t_{OH}

Outputs

High-Z

Outputs Valid

High-Z
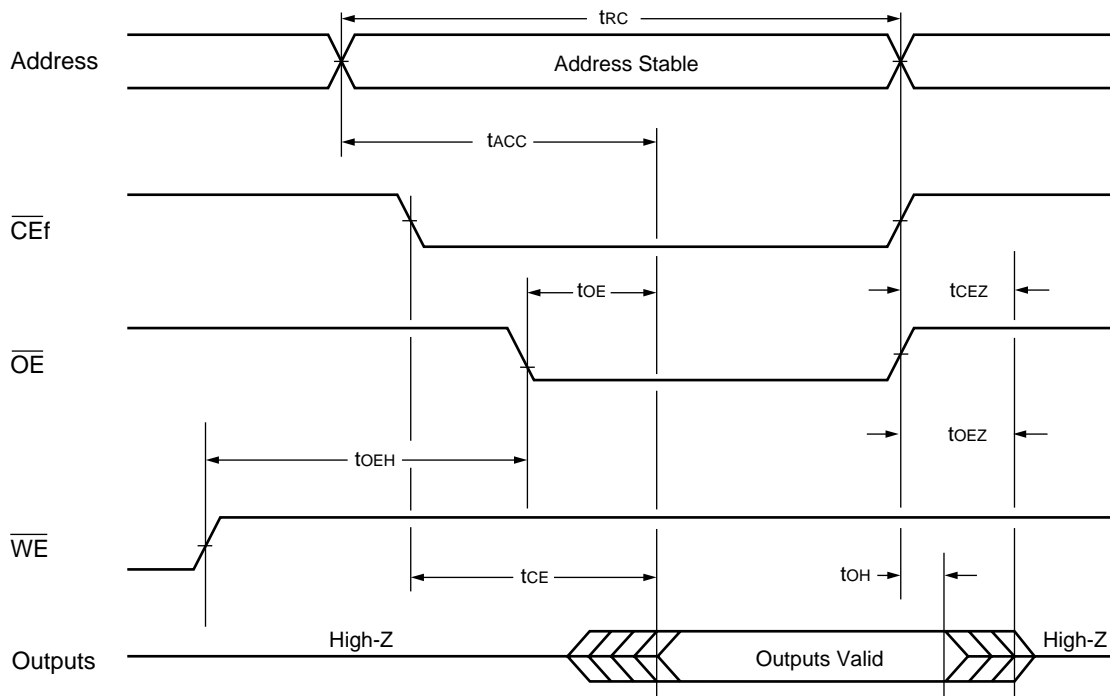
Notes : • $\overline{ADV}$ is assumed to be V_{IL}.
• Configuration Register is set to Asynchronous mode.

• **Reset Timings**
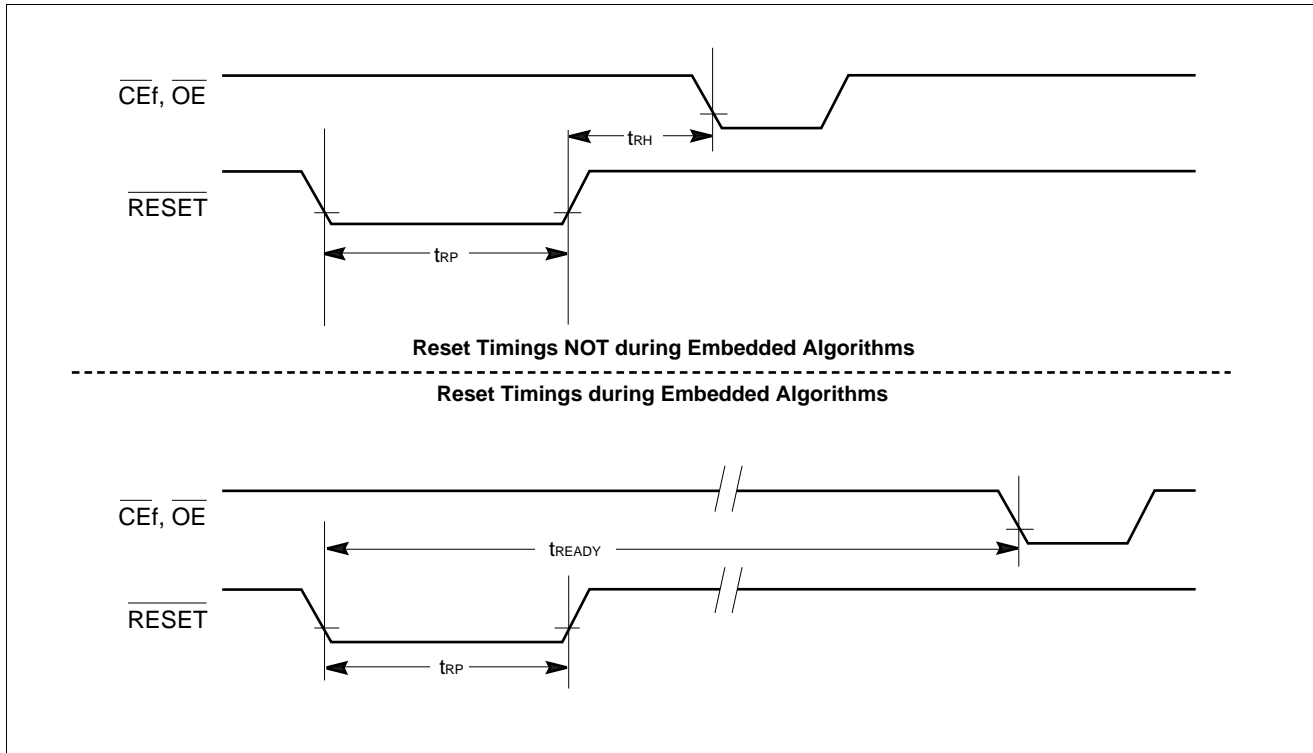
• **Power On/Off Timings (128M Burst Flash)**
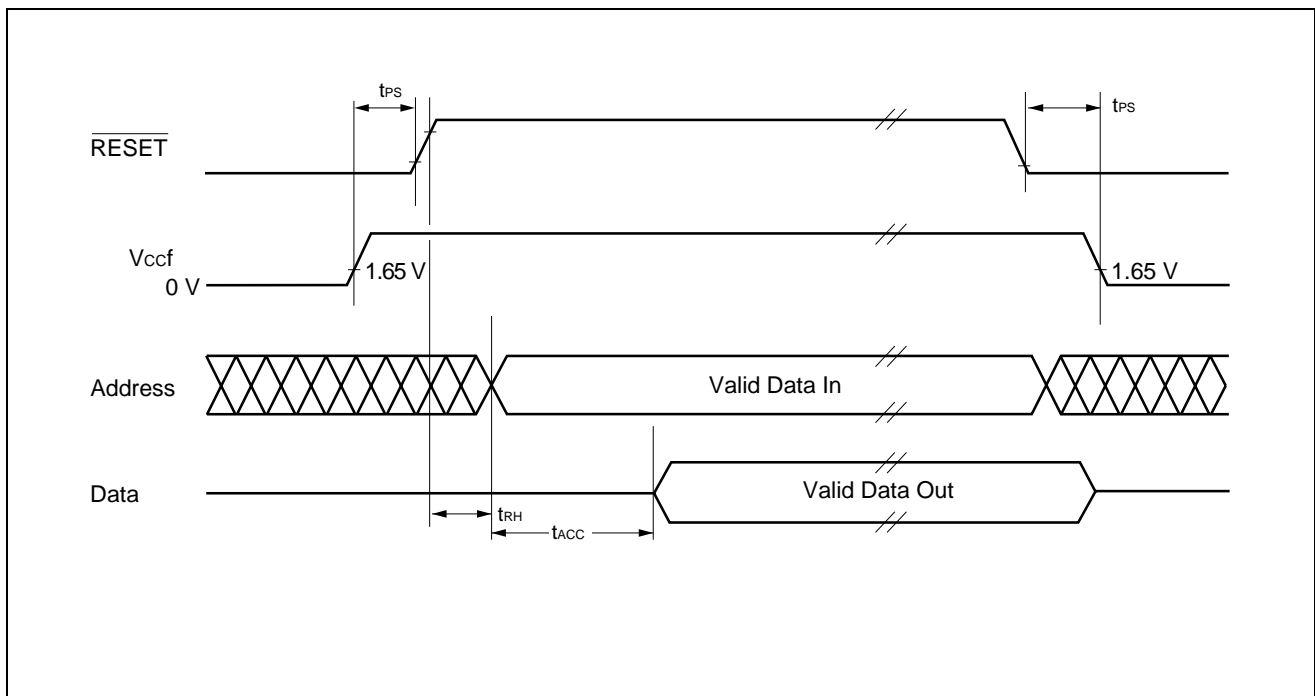
• **Program Operation Timings at Asynchronous Mode ($\overline{\text{WE}}$ latch)**
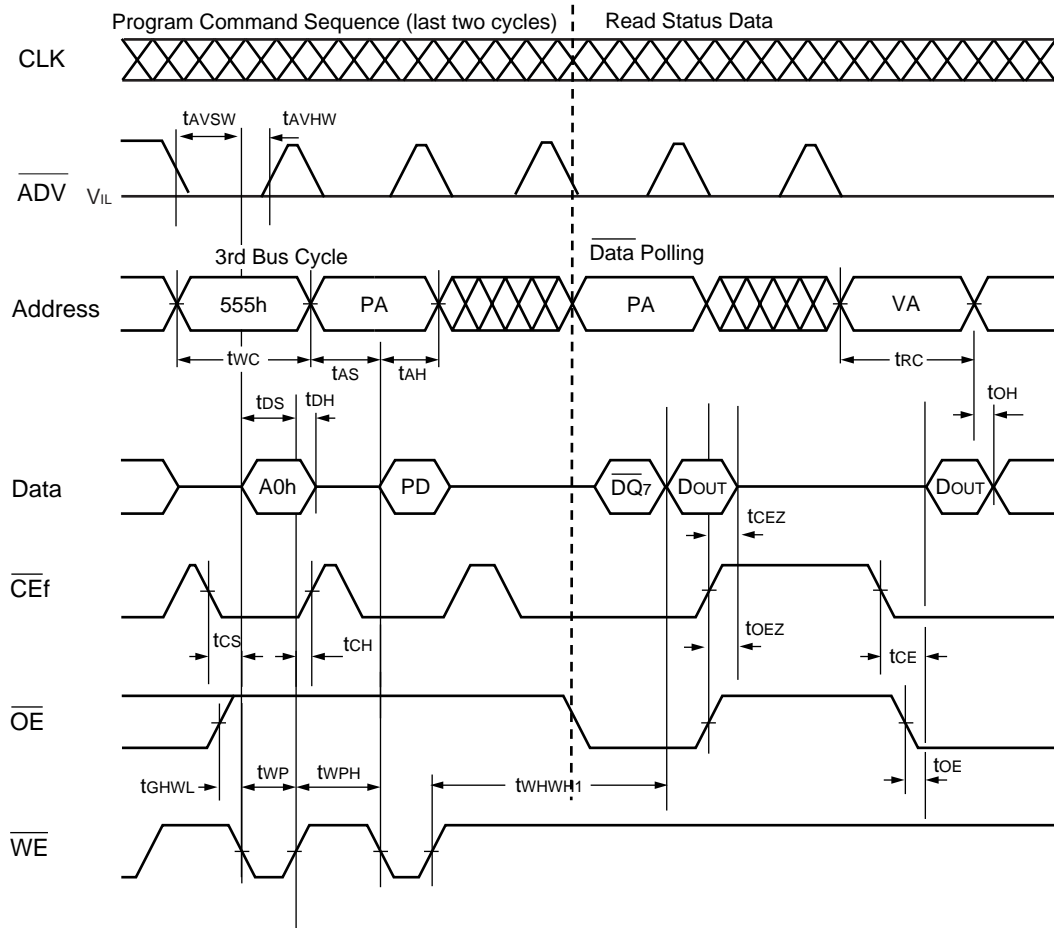
Notes : • PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
           • "In progress" and "complete" refer to status of program operation.
           • A_{22} to A_{12} are don't care during command sequence unlock cycles.
           • CLK is "Don't care".
           • Configuration Register is set to Asynchronous mode.

• **Program Operation Timings at Asynchronous Mode (ADV latch)**
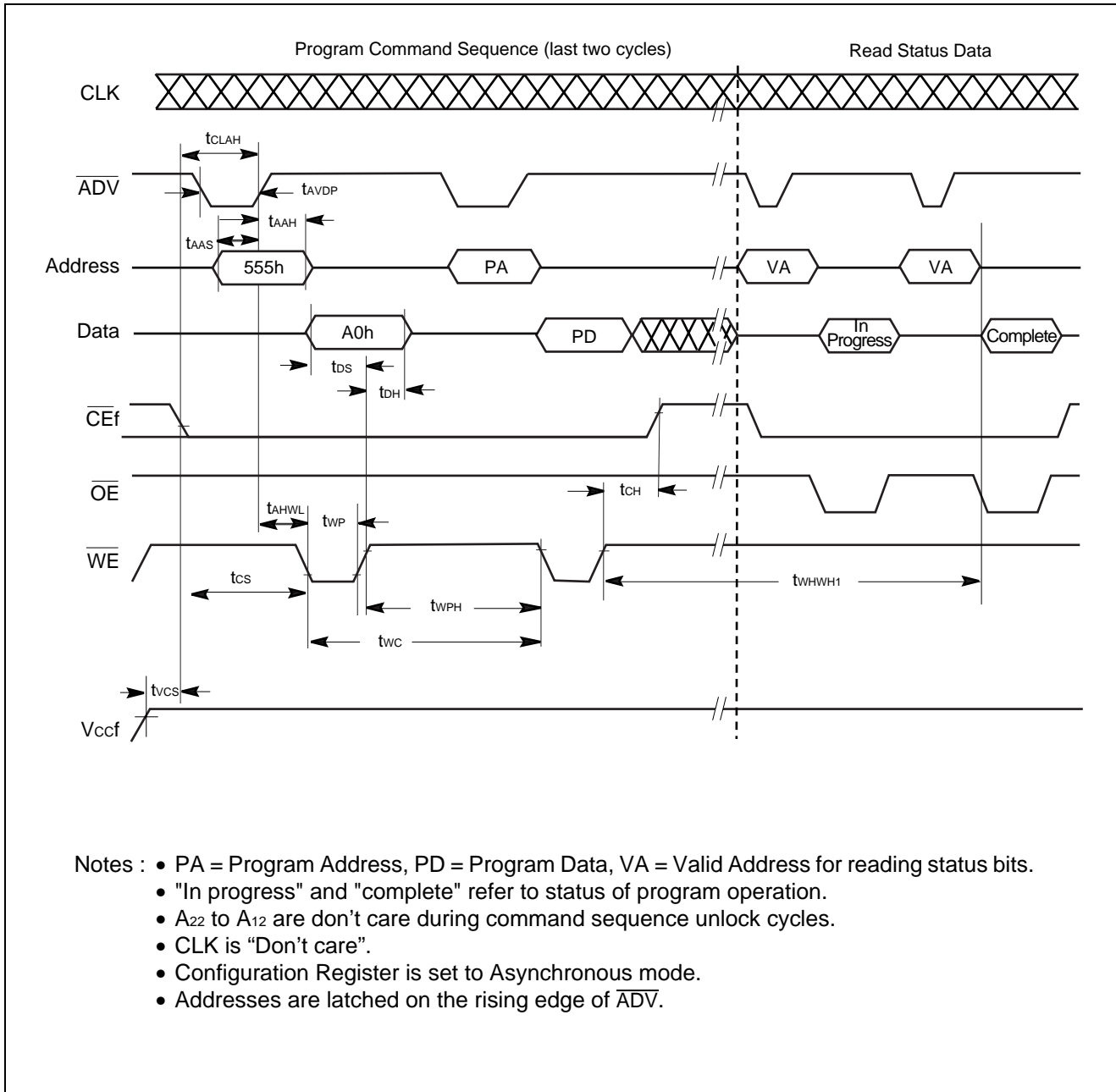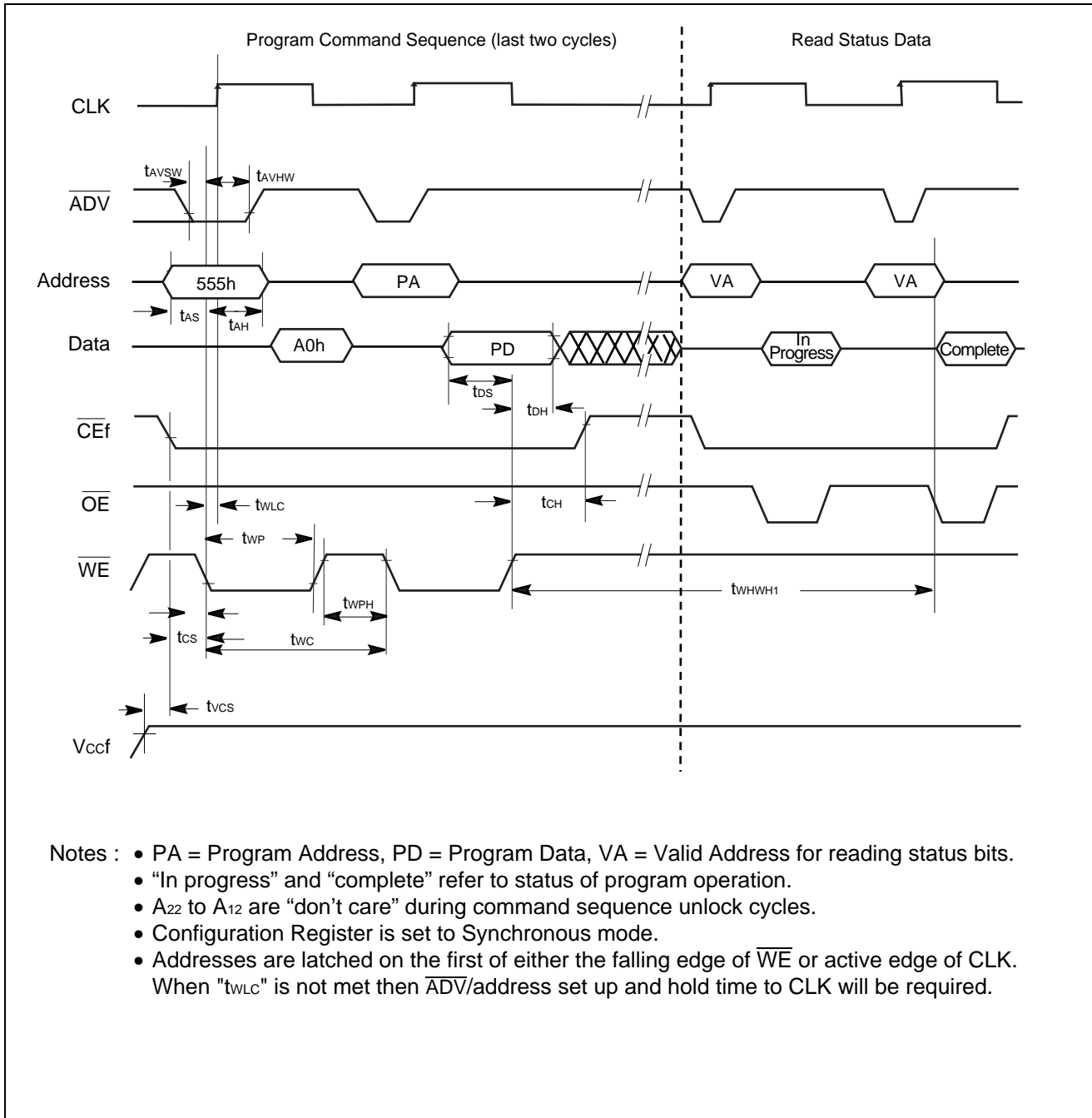
Notes : • PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
• "In progress" and "complete" refer to status of program operation.
• A_{22} to A_{12} are don't care during command sequence unlock cycles.
• CLK is "Don't care".
• Configuration Register is set to Asynchronous mode.
• Addresses are latched on the rising edge of ADV.

• **Program Operation Timings at Synchronous Mode ($\overline{WE}$ latch)**

Notes : • PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
         • "In progress" and "complete" refer to status of program operation.
         • A_{22} to A_{12} are "don't care" during command sequence unlock cycles.
         • Configuration Register is set to Synchronous mode.
         • Addresses are latched on the first of either the falling edge of $\overline{WE}$ or active edge of CLK.
           When "t_{WLC}" is not met then $\overline{ADV}$/address set up and hold time to CLK will be required.

• **Program Operation Timings at Synchronous Mode (CLK latch)**
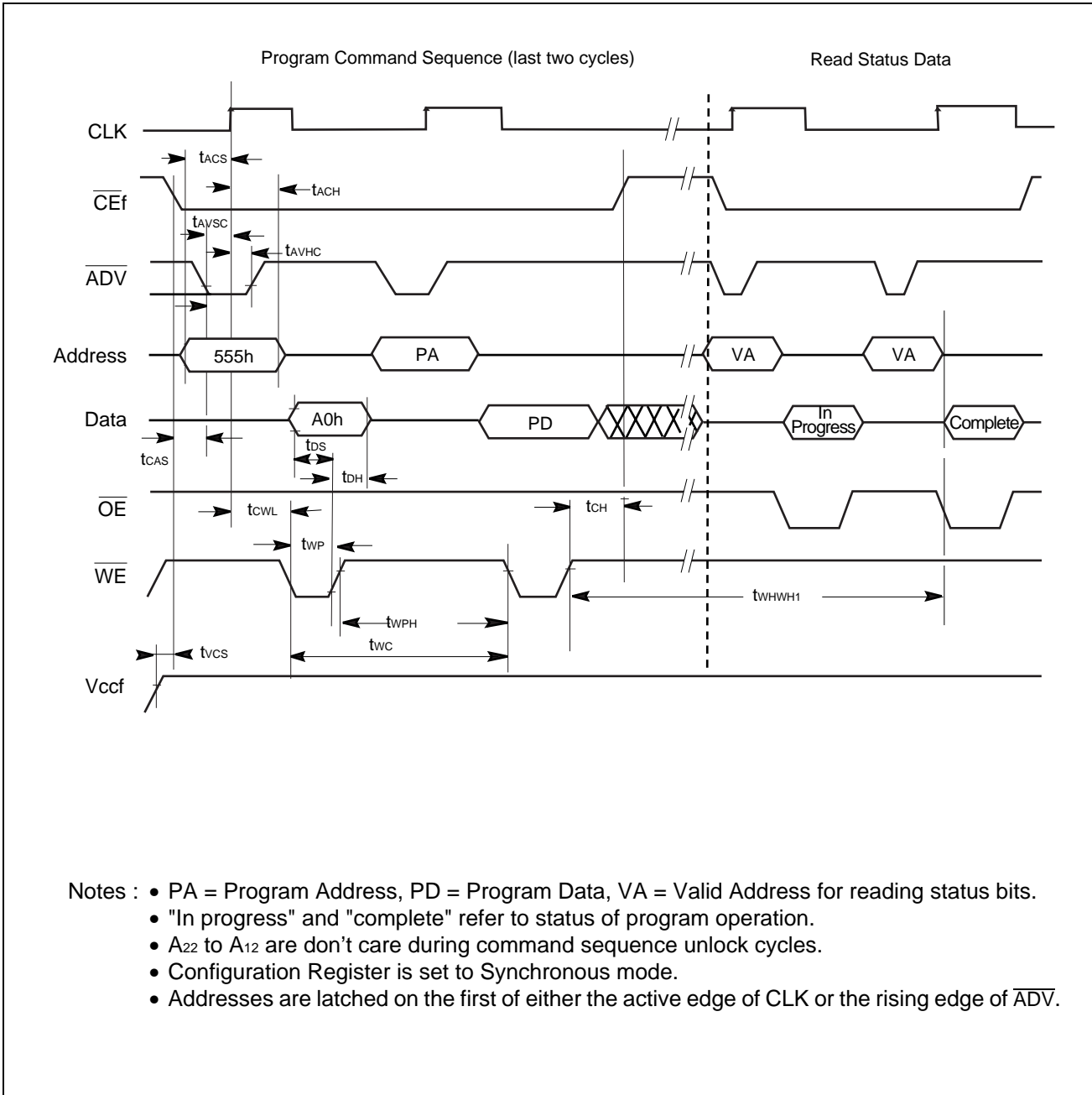
Notes :
• PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
• "In progress" and "complete" refer to status of program operation.
• A_{22} to A_{12} are don't care during command sequence unlock cycles.
• Configuration Register is set to Synchronous mode.
• Addresses are latched on the first of either the active edge of CLK or the rising edge of $\overline{ADV}$.

• **Chip/Sector Erase Command Sequence**

Notes : • SA is the sector address for Sector Erase.
• Address bits A_{22} to A_{12} are don't cares during unlock cycles in the command sequence.
• This timing is for Synchronous mode.
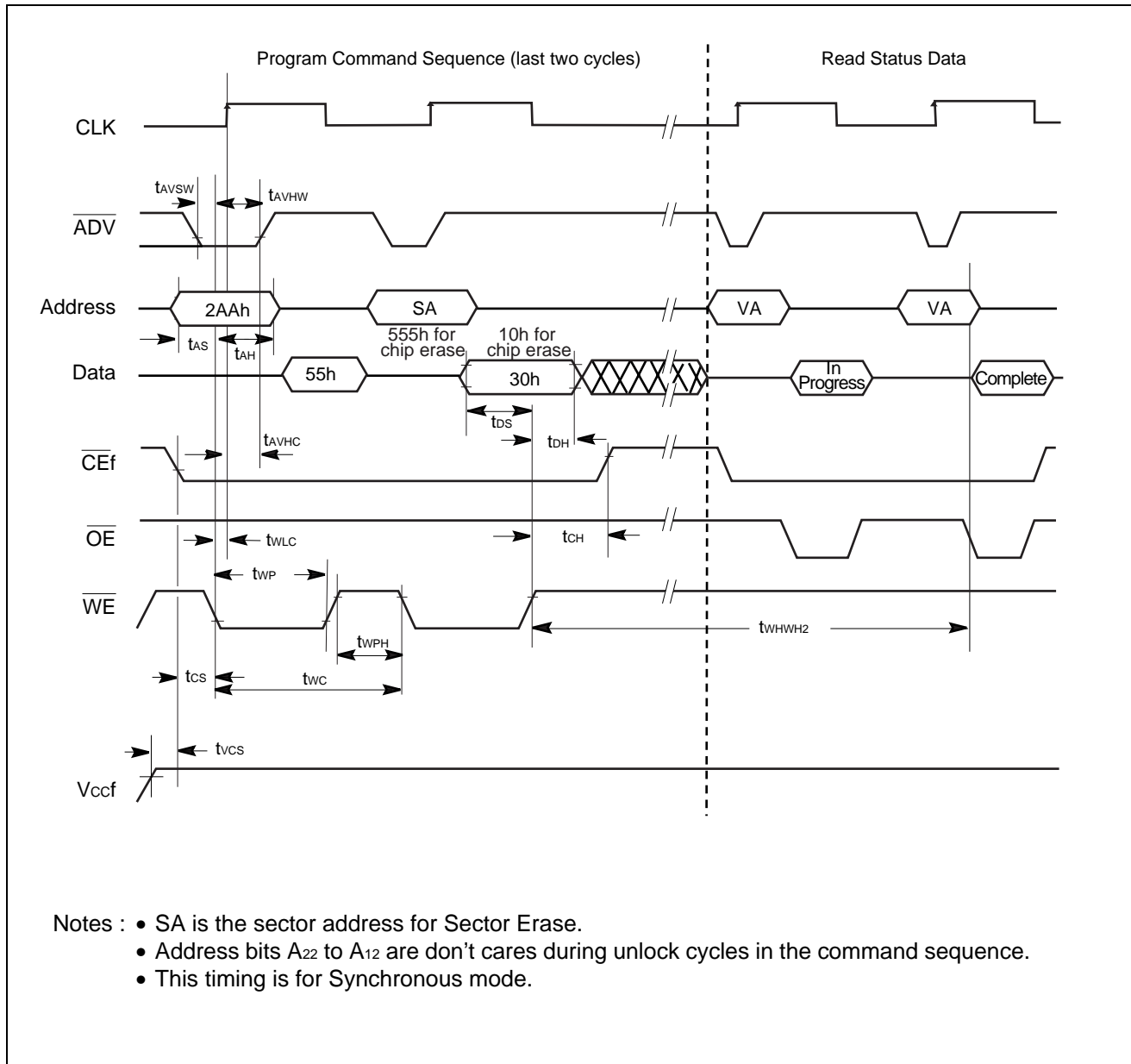
- $\overline{\text{Data}}$ Polling Timings/Toggle Bit Timings (During Embedded Algorithm)

Notes :
- Status reads in figure are shown as asynchronous mode.
- VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and $\overline{\text{Data}}$ Polling will output true data and the toggle bits will stop toggling.
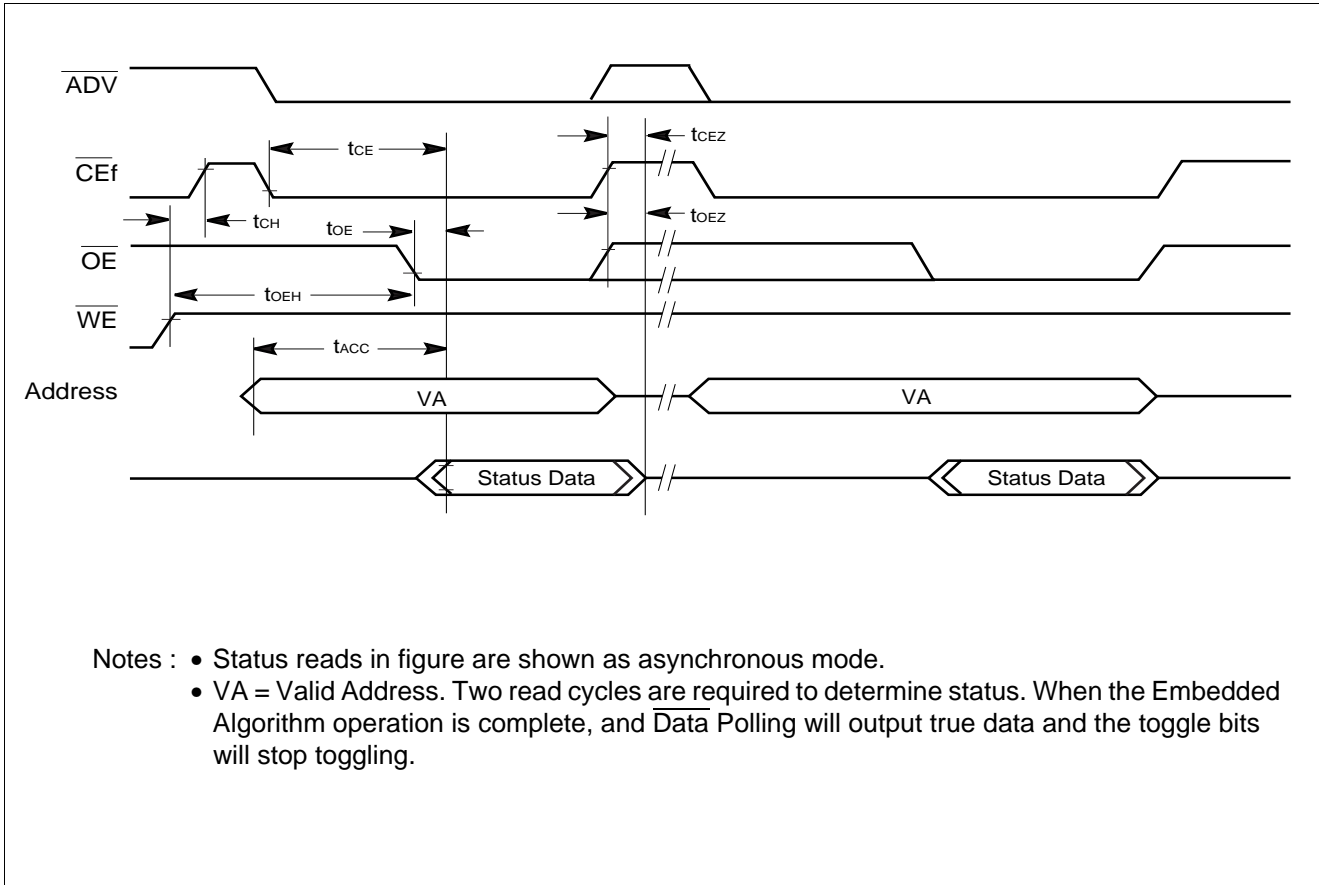
• **Synchronous Data Polling Timings/Toggle Bit Timings**
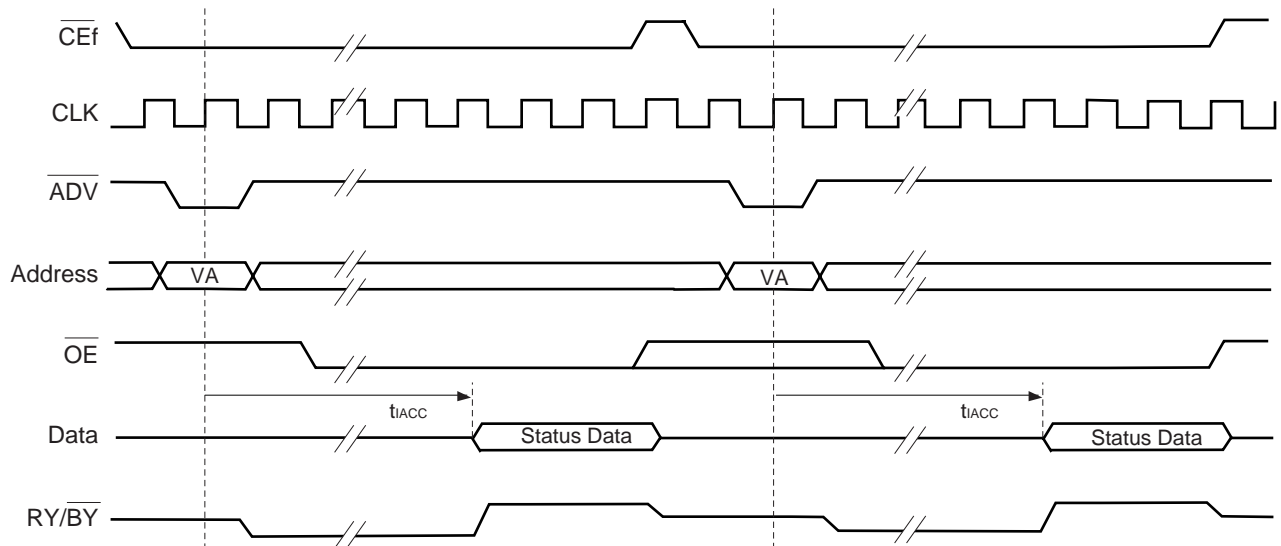
Notes : • The timings are similar to synchronous read timings.
         • VA = Valid Address. Two read cycles are required to determine status. When the Embedded
           Algorithm operation is complete, the toggle bits will stop toggling.
         • RY/$\overline{BY}$ is active with data (A_{18} = 0 in the Burst Mode Configuration Register). When A_{18} = 1
           in the Burst Mode Configuration Register, RY/$\overline{BY}$ is active one clock cycle before data.

- **Example of Wait States Insertion (Non-Handshaking Device)**
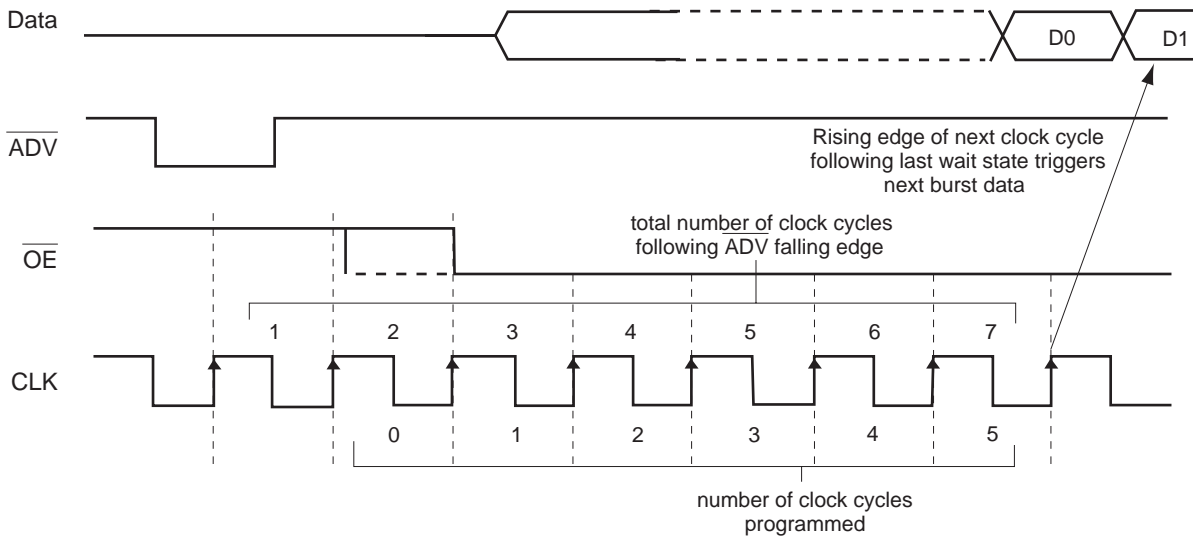
Wait State Decoding Addresses:
A_{14}, A_{13}, A_{12} = "101" $\Rightarrow$ 5 programmed, 7 total
A_{14}, A_{13}, A_{12} = "100" $\Rightarrow$ 4 programmed, 6 total
A_{14}, A_{13}, A_{12} = "011" $\Rightarrow$ 3 programmed, 5 total
A_{14}, A_{13}, A_{12} = "010" $\Rightarrow$ 2 programmed, 4 total
A_{14}, A_{13}, A_{12} = "001" $\Rightarrow$ 1 programmed, 3 total
A_{14}, A_{13}, A_{12} = "000" $\Rightarrow$ 0 programmed, 2 total

Note : Figure assumes address D0 is not at an address boundary, active clock edge is rising, and wait state is set to "101".

- **Bank-to-Bank Read/Write Cycle Timings**

Note : Breakpoints in waveforms indicate that system may alternately read array data from the "non-busy bank" while checking the status of the program or erase operation in the "busy" bank. The system should read status twice to ensure valid information.
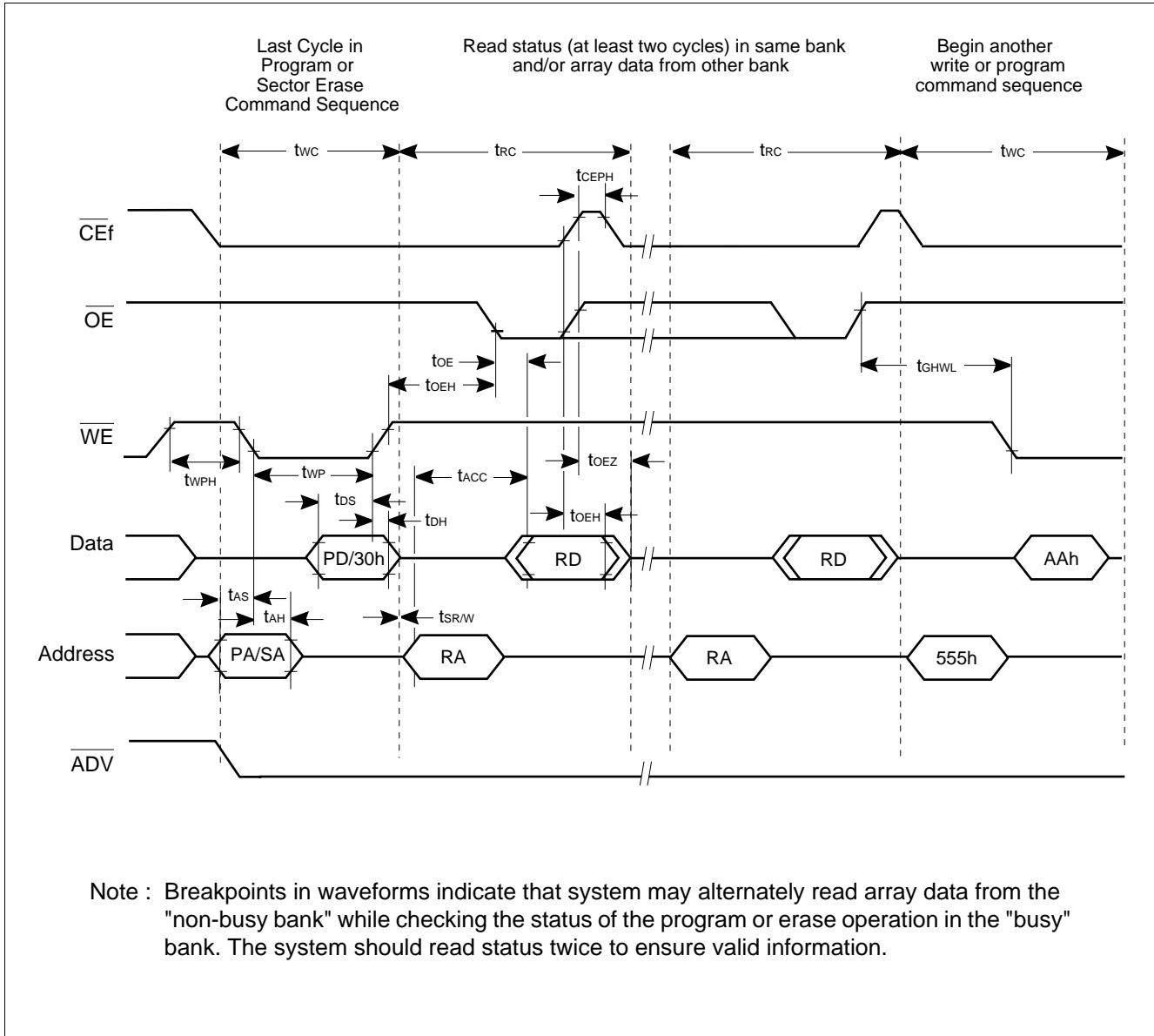
■ 128M FCRAM CHARACTERISTICS for MCP

1. State Diagram
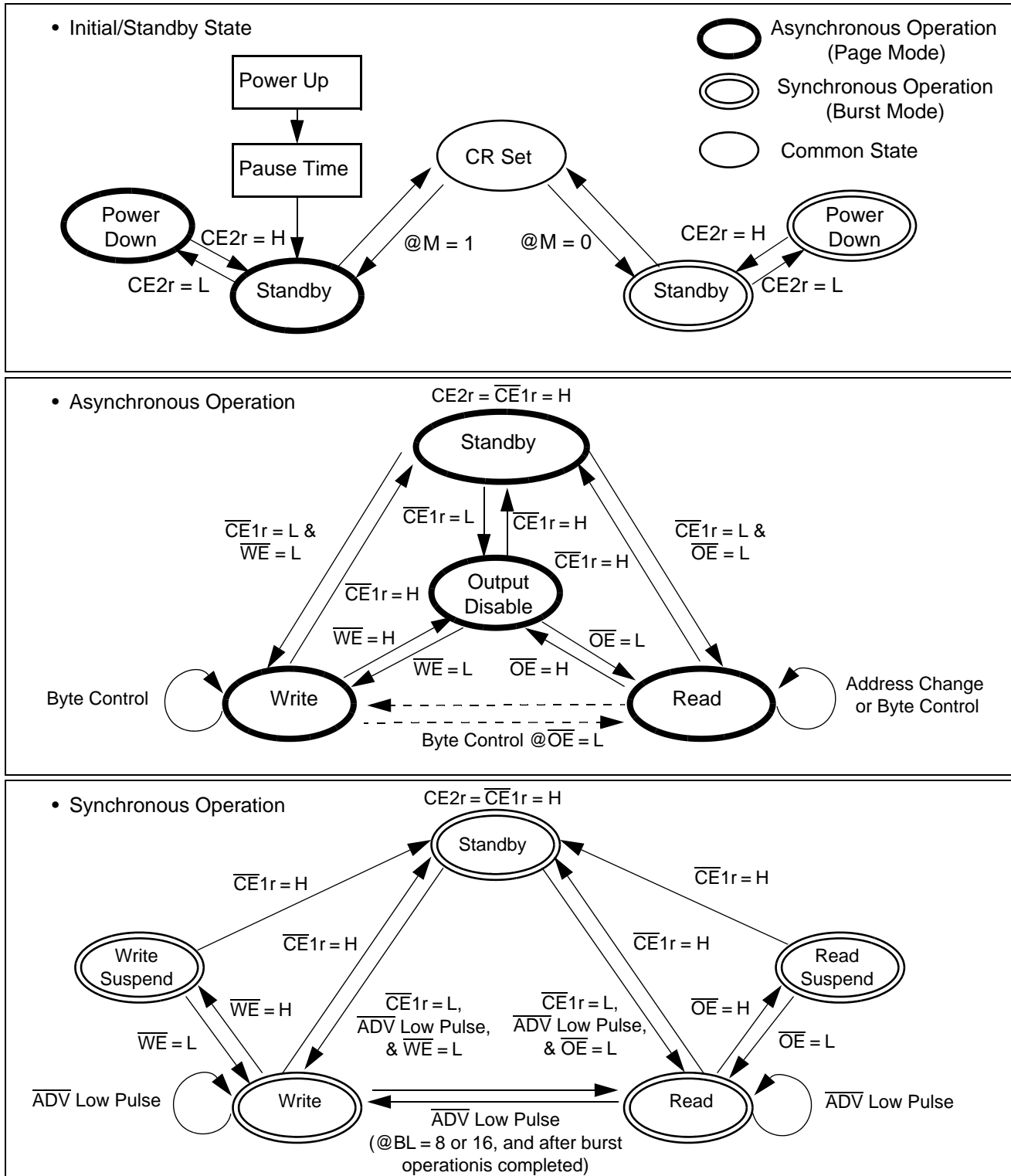
Note : Assuming all the parameters specified in "3. AC Characteristics" in "■ 128M FCRAM CHARACTERISTICS for MCP" are satisfied. Refer to "2. Functial Description" and "3. AC Characteristics" for details.

2. Functional Description

This device supports asynchronous page read & normal write operation and synchronous burst read & burst write operation for faster memory access and features three kinds of power down modes for power saving as user configuable option.

• Power-up

It is required to follow the power-up timing to start executing proper device operation. Refer to POWER-UP Timing. After Power-up, the device defaults to asynchronous page read & normal write operation mode with sleep power down feature.

• Configuration Register

The Configuration Register (CR) is used to configure the type of device function among optional features. Each selection of features is set through CR Set sequence after Power-up. If CR Set sequence is not performed after power-up, the device is configured for asynchronous operation with sleep power down feature as default configuration.

• CR Set Sequence

The CR Set requires total 6 read/write operation with unique address. Between each read/write operation requires that device being in standby mode. Following table shows the detail sequence.

Cycle #	Operation	Address	Data
1st	Read	7FFFFFh (MSB)	Read Data (RDa)
2nd	Write	7FFFFFh	RDa
3rd	Write	7FFFFFh	RDa
4th	Write	7FFFFFh	X
5th	Write	7FFFFFh	X
6th	Read	Address Key	Read Data (RDb)

The first cycle is to read from most significant address (MSB).
The second and third cycle are to write back the data (RDa) read by first cycle. If the second or third cycle is written into the different address, the CR Set is cancelled and the data written by the second or third cycle is valid as a normal write operation.
The forth and fifth cycle is to write to MSB. The data of forth and fifth cycle is don't-care. If the forth or fifth cycle is written into different address, the CR Set is also cancelled but write data may not be written as normal write operation.
The last cycle is to read from specific address key for mode selection. And read data (RDb) is invalid.

Once this CR Set sequence is performed from an initial CR set to the other new CR set, the written data stored in memory cell array may be lost. So, it should perform the CR Set sequence prior to regular read/write operation if necessary to change from default configuration.

• **Address Key**

The address key has the following format.

Address Pin	Register Name	Function	Key	Description	Note
A_{22} to A_{21}	—	—	1	Unused bits must be 1	*1
A_{20} to A_{19}	PS	Partial Size	00	32M Partial	
			01	16M Partial	
			10	Reserved for future use	*2
			11	Sleep [Default]	
A_{18} to A_{16}	BL	Burst Length	000	Reserved for future use	*2
			001	Reserved for future use	*2
			010	8 words	
			011	16 words	
			100	Reserved for future use	*2
			101	Reserved for future use	*2
			110	Reserved for future use	*2
			111	Continuous	
A_{15}	M	Mode	0	Synchronous Mode (Burst Read / Write)	*3
			1	Asynchronous Mode[Default] (Page Read / Normal Write)	*4
A_{14} to A_{12}	RL	Read Latency	000	Reserved for future use	*2
			001	3 clocks	
			010	4 clocks	
			011	5 clocks	
			1xx	Reserved for future use	*2
A_{11}	BS	Burst Sequence	0	Reserved for future use	*2
			1	Sequential	
A_{10}	SW	Single Write	0	Burst Read & Burst Write	
			1	Burst Read & Single Write	*5
A_9	VE	Valid Clock Edge	0	Falling Clock Edge	
			1	Rising Clock Edge	
A_8	—	—	1	Unused bits muse be 1	*1
A_7	WC	Write Control	0	$\overline{WE}$ Single Clock Pulse Control without Write Suspend Function	*5
			1	$\overline{WE}$ Level Control with Write Suspend Function	
A_6 to A_0	—	—	1	Unused bits must be 1	*1

*1 : A_{22}, A_{21}, A_8, and A_6 to A_0 must be all "1" in any cases.

*2 : It is prohibited to apply this key.

*3 : If M=0, all the registers must be set with appropriate Key input at the same time.

*4 : If M=1, PS must be set with appropriate Key input at the same time. Except for PS, all the other key inputs must be "1".

*5 : Burst Read & Single Write is not supported at $\overline{WE}$ Single Clock Pulse Control.

• **Power Down**

The Power Down is low power idle state controlled by CE2r. CE2r Low drives the device in power down mode and mains low power idle state as long as CE2r is kept low. CE2r High resume the device from power down mode.

This device has three power down modes, Sleep, 16M Partial, and 32M Partial.
The selection of power down mode is set through CR Set sequence. Each mode has following data retention features.

Mode	Data Retention Size	Retention Address
Sleep [default]	No	N/A
16M Partial	16M bit	000000h to 0FFFFFh
32M Partial	32M bit	000000h to 1FFFFFh

The default state is Sleep and it is the lowest power consumption but all data will be lost once CE2 is brought to Low for Power Down. It is not required to perform CR Set sequence to set to Sleep mode after power-up in case of asynchronous operation.

- **Burst Read/Write Operation**

Synchronous burst read/write operation provides faster memory access that synchronized to microcontroller or system bus frequency. Configuration Register Set is required to perform burst read & write operation after power-up. Once CR Set sequence is performed to select synchronous burst mode, the device is configured to synchro-nous burst read/write operation mode with corresponding RL and BL that is set through CR Set sequence together with operation mode. In order to perform synchronous burst read & write operation, it is required to control new signals, CLK, $\overline{ADV}$ and $\overline{WAIT}$ that Low Power SRAMs don't have.
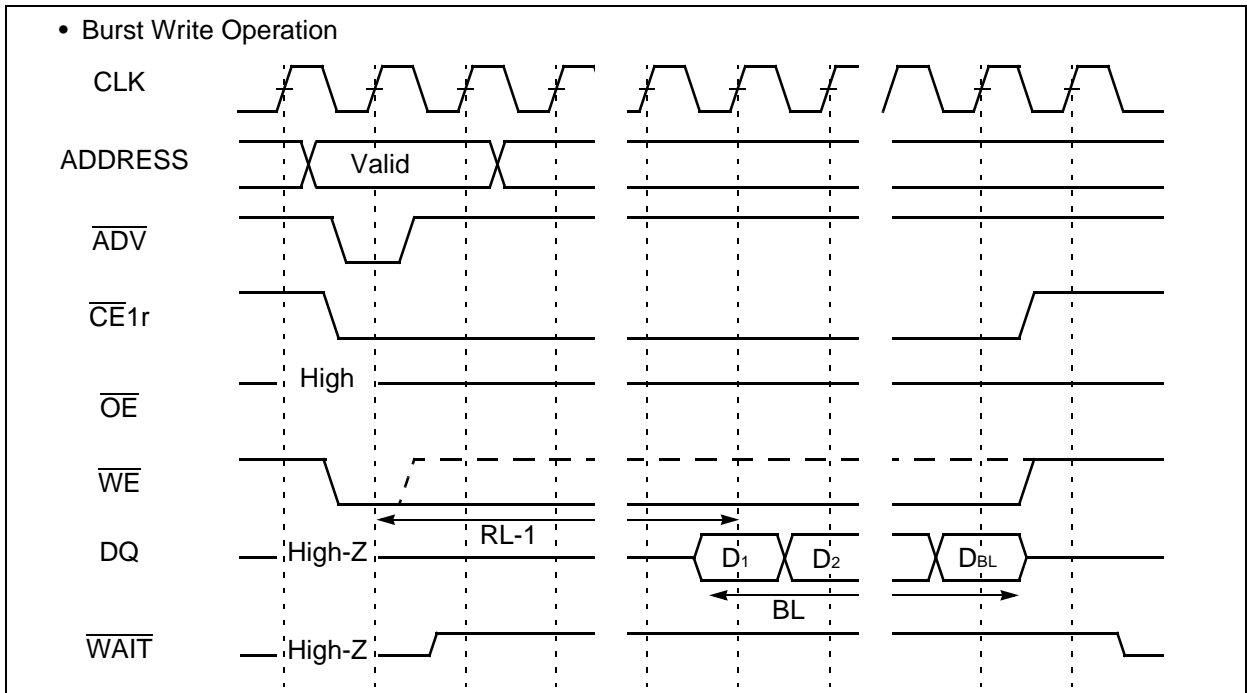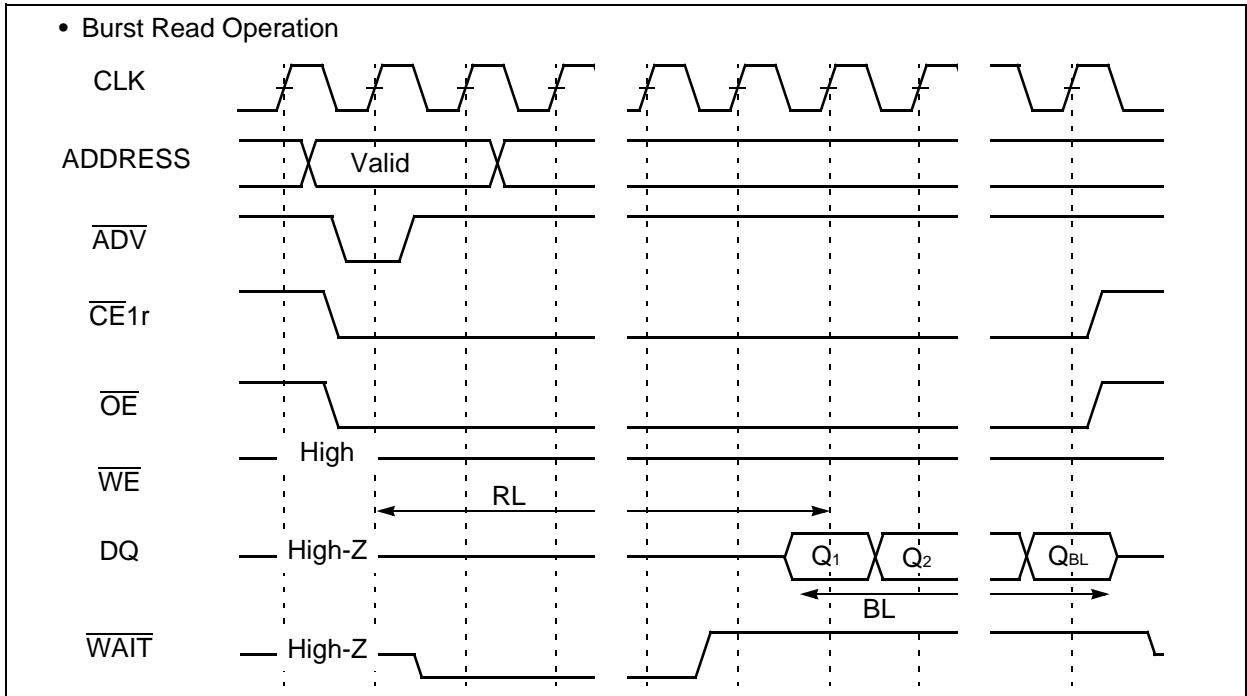
• **CLK Input Function**

The CLK is input signal to synchronize memory to microcontroller or system bus frequency during synchronous burst read & write operation. The CLK input increments device internal address counter and the valid edge of CLK is referred for latency counts from address latch, burst write data latch, and burst read data out. During synchronous operation mode, CLK input must be supplied except for standby state and power down state. CLK is don't care during asynchronous operation.

• $\overline{\text{ADV}}$ **Input Function**

The $\overline{\text{ADV}}$ is input signal to indicate valid address presence on address inputs. It is applicable to synchronous operation as well as asynchronous operation. $\overline{\text{ADV}}$ input is active during $\overline{\text{CE}}$1r = L and $\overline{\text{CE}}$1r = H disables $\overline{\text{ADV}}$ input. All the address are determined on the positive edge of $\overline{\text{ADV}}$.

During synchronous burst read/write operation, $\overline{\text{ADV}}$ = H disables all address inputs. Once $\overline{\text{ADV}}$ is brought to High after valid address latch, it is inhibited to bring $\overline{\text{ADV}}$ Low until the end of burst or until burst operation is terminated. $\overline{\text{ADV}}$ Low pulse is mandatory for synchronous burst read/write operation mode to latch the valid address input.

During asynchronous operation, $\overline{\text{ADV}}$ = H also disables all address inputs. $\overline{\text{ADV}}$ can be tied to Low during asynchronous operation and it is not necessary to control $\overline{\text{ADV}}$ to High.

• $\overline{\text{WAIT}}$ **Output Function**

The $\overline{\text{WAIT}}$ is output signal to indicate data bus status when the device is operating in synchronous burst mode.

During burst read operation, $\overline{\text{WAIT}}$ output is enabled after specified time duration from $\overline{\text{OE}}$ = L. $\overline{\text{WAIT}}$ output Low indicates data out at next clock cycle is invalid, and $\overline{\text{WAIT}}$ output becomes High one clock cycle prior to valid data out. During $\overline{\text{OE}}$ read suspend, $\overline{\text{WAIT}}$ output doesn't indicate data bus status but carries the same level from previous clock cycle (kept High) except for read suspend on the final data output. If final read data out is suspended, $\overline{\text{WAIT}}$ output become high impedance after specified time duration from $\overline{\text{OE}}$ = H.

During burst write operation, $\overline{\text{WAIT}}$ output is enabled to High level after specified time duration from $\overline{\text{WE}}$ = L and kept High for entire write cycles including $\overline{\text{WE}}$ write suspend. The actual write data latching starts on the appropriate clock edge with respect to Valid Click Edge, Read Latency and Burst Length. During $\overline{\text{WE}}$ write suspend, $\overline{\text{WAIT}}$ output doesn't indicate data bus status but carries the same level from previous clock cycle (kept High) except for write suspend on the final data input. If final write data in is suspended, $\overline{\text{WAIT}}$ output become high impedance after specified time duration from $\overline{\text{WE}}$ = H.

This device doesn't incur additional delay against accrossing device-row boundary or internal refresh orepation. Therefore, the burst operation is always started after fixed latency with respect to Read Latency. And there is no $\overline{\text{WAIT}}$ting cycle asserted in the middle of burst operation except for burst suspend by $\overline{\text{OE}}$ brought to High or $\overline{\text{WE}}$ brought to High. Thus, once $\overline{\text{WAIT}}$ output is enabled and brought to High, $\overline{\text{WAIT}}$ output keep High level until the end of burst or until the burst operation is terminated.

When the device is operating in asynchronous mode, $\overline{\text{WAIT}}$ output is always in High Impedance.

• **Latency**

Read Latency (RL) is the number of clock cycles between the address being latched and first read data becoming available during synchronous burst read operation. It is set through CR Set sequence after power-up. Once specific RL is set through CR Set sequence, write latency, that is the number of clock cycles between address being latched and first write data being latched, is automatically set to RL-1. The burst operation is always started after fixed latency with respect to Read Latency set in CR.
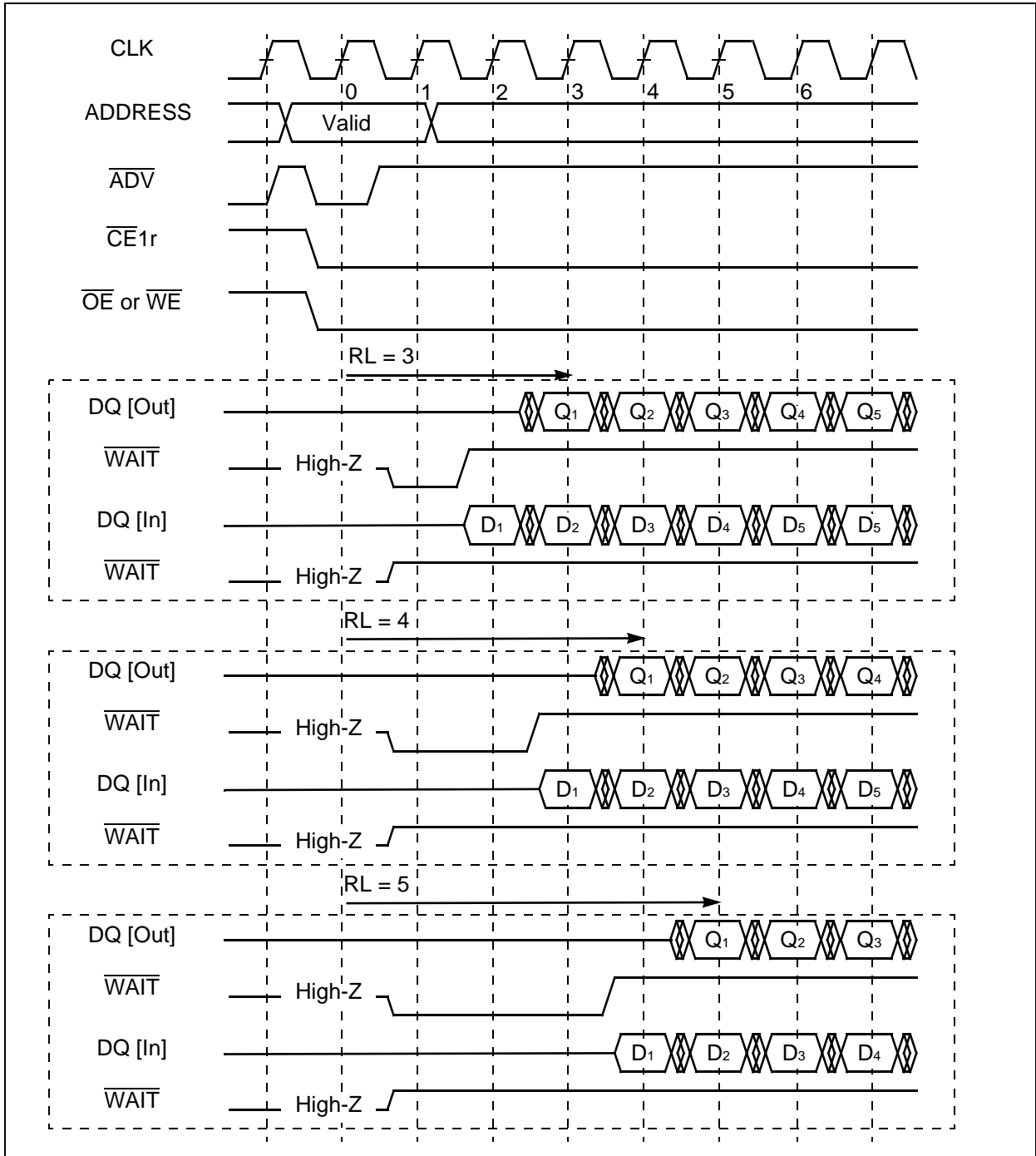
- **Address Latch by $\overline{ADV}$**

The $\overline{ADV}$ indicates valid address presence on address inputs. During synchronous burst read/write operation mode, all the address are determined on the positive edge of $\overline{ADV}$ when $\overline{CE}1r$ = L. The specified minimum value of $\overline{ADV}$ = L setup time and hold time against valid edge of clock where RL count begin must be satisfied for appropriate RL counts. Valid address must be determined with specified setup time against either the negative edge of $\overline{ADV}$ or negative edge of $\overline{CE}1r$ whichever comes late. And the determined valid address must not be changed during $\overline{ADV}$ = L period.

- **Burst Length**

Burst Length is the number of word to be read or write during synchronous burst read/write operation as the result of a single address latch cycle. It can be set on 8, 16 words boundary or continuous for entire address through CR Set sequence. The burst type is sequential that is incremental decoding scheme within a boundary address. Starting from initial address being latched, device internal address counter assign +1 to the previous address until reaching the end of boundary address and then wrap round to least significant address (= 0). After completing read data out or write data latch for the set burst length, operation automatically ended except for continuous burst length. When continuous burst length is set, read/write is endless unless it is terminated by the positive edge of $\overline{CE}1r$.

- **Single Write**

Single Write is synchronous write operation with Burst Length =1. The device can be configured either to "Burst Read & Single Write" or to "Burst Read & Burst Write" through CR set sequence. Once the device is configured to "Burst Read & Single Write" mode, the burst length for syncronous write operation is always fixed 1 regardless of BL values set in CR, while burst length for read is in accordance with BL values set in CR.

- **Write Control**

The device has two type of $\overline{WE}$ singal control method, "$\overline{WE}$ Level Control" and "$\overline{WE}$ Single Clock Pulse Control", for synchronous write operation. It is configured through CR set sequence.
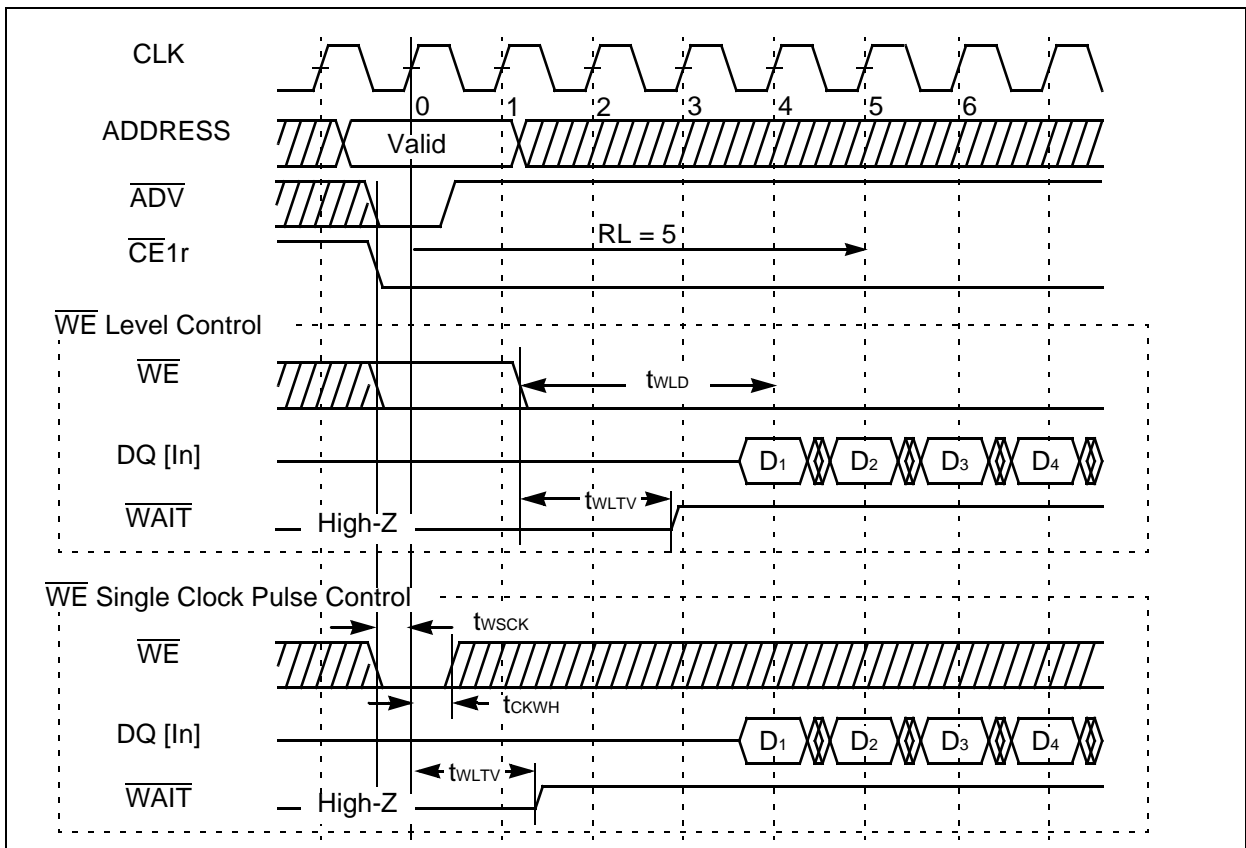
• **Burst Read Suspend**

Burst read operation can be suspended by $\overline{OE}$ High pulse. During burst read operation, $\overline{OE}$ brought to High suspends burst read operation. Once $\overline{OE}$ is brought to High with the specified set up time against clock where the data being suspended, the device internal counter is suspended, and the data output become high impedance after specified time duration. It is inhibited to suspend the first data out at the beginning of burst read.

$\overline{OE}$ brought to Low resumes burst read operation. Once $\overline{OE}$ is brought to Low, data output become valid after specified time duration, and internal address counter is reactivated. The last data out being suspended as the result of $\overline{OE}$ = H and first data out as the result of $\overline{OE}$ = L are the from the same address.
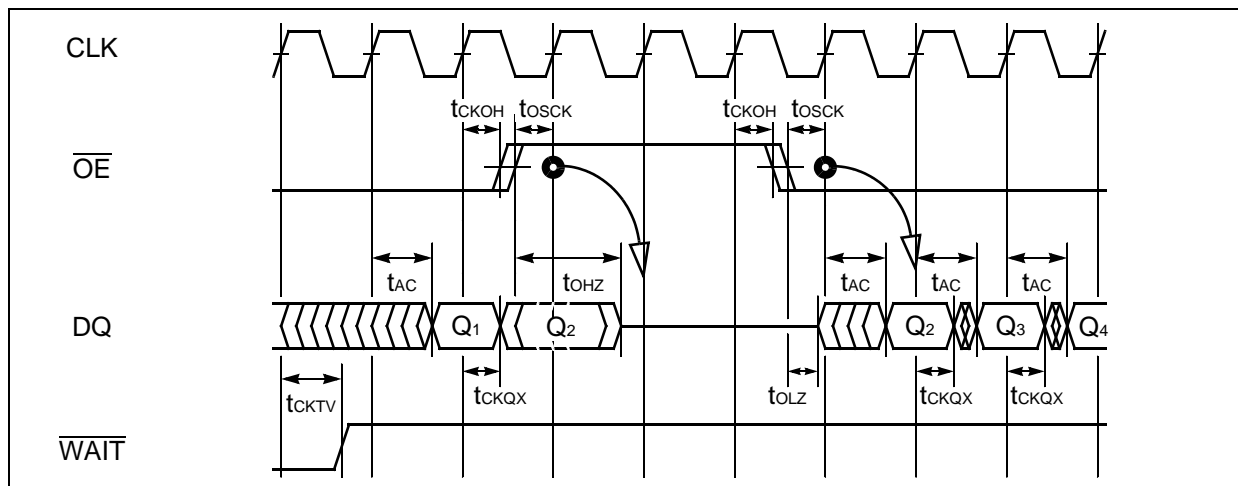
• **Burst Write Suspend**

Burst write operation can be suspended by $\overline{WE}$ High pulse. During burst write operation, $\overline{WE}$ brought to High suspends burst write operation. Once $\overline{WE}$ is brought to High with the specified set up time against clock where the data being suspended, device internal counter is suspended, data input is ignored. It is inhibited to suspend the first data input at the beginning of burst write.

$\overline{WE}$ brought to Low resumes burst write operation. Once $\overline{WE}$ is brought to Low, data input become valid after specified time duration, and internal address counter is reactivated. The write address of the cycle where data being suspended and the first write address as the result of $\overline{WE}$ = L are the same address.

Burst write suspend function is available when the device is operating in $\overline{WE}$ level controlled burst write only.
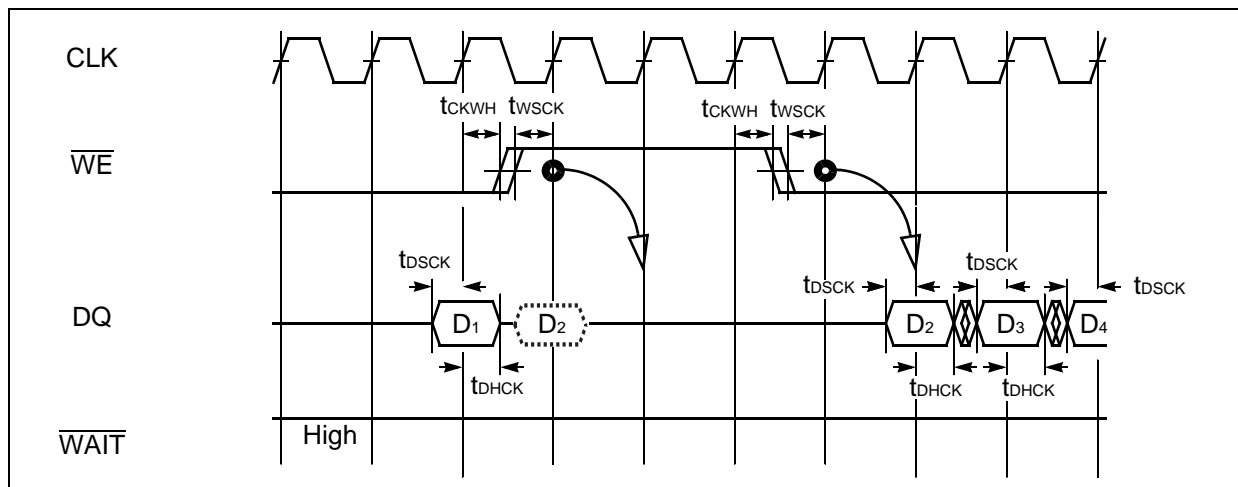
• **Burst Read Termination**

Burst read operation can be terminated by $\overline{CE}1r$ brought to High. If BL is set on Continuous, burst read operation is continued endless unless terminated by $\overline{CE}1r$ = H. It is inhibited to terminate burst read before first data out is completed. In order to guarantee last data output, the specified minimum value of $\overline{CE}1r$ = L hold time from clock edge must be satisfied. After termination, the specified minimum recovery time is required to start new access.

CLK
ADDRESS — Valid
$\overline{ADV}$ — t_{TRB}
t_{CKCLH} — t_{CHZ}
$\overline{CE}1r$
t_{CKOH} — t_{OHZ}
$\overline{OE}$
$\overline{WAIT}$ — High-Z
t_{AC} — t_{CKQX}
DQ — Q_1 Q_2
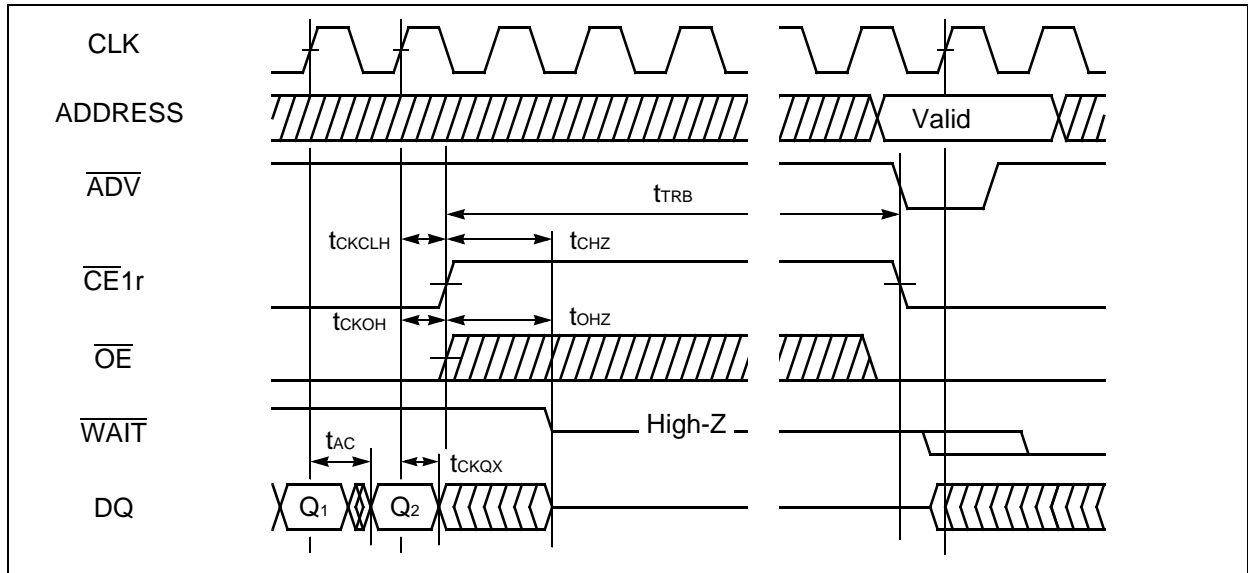
• **Burst Write Termination**

Burst write operation can be terminated by $\overline{CE}1r$ brought to High. If BL is set on Continuous, burst write operation is continued endless unless terminated by $\overline{CE}1r$ = H. It is inhibited to terminate burst write before first data in is completed. In order to guarantee last write data being latched, the specified minimum values of $\overline{CE}1r$ = L hold time from clock edge must be satisfied. After termination, the specified minimum recovery time is required to start new access.

CLK
ADDRESS — Valid
$\overline{ADV}$ — t_{TRB}
t_{CKCLH} — t_{CHZ}
$\overline{CE}1r$
t_{CKWH}
$\overline{WE}$
$\overline{WAIT}$ — High-Z
t_{DSCK} t_{DSCK}
DQ — D_1 D_2
t_{DHCK} t_{DHCK}
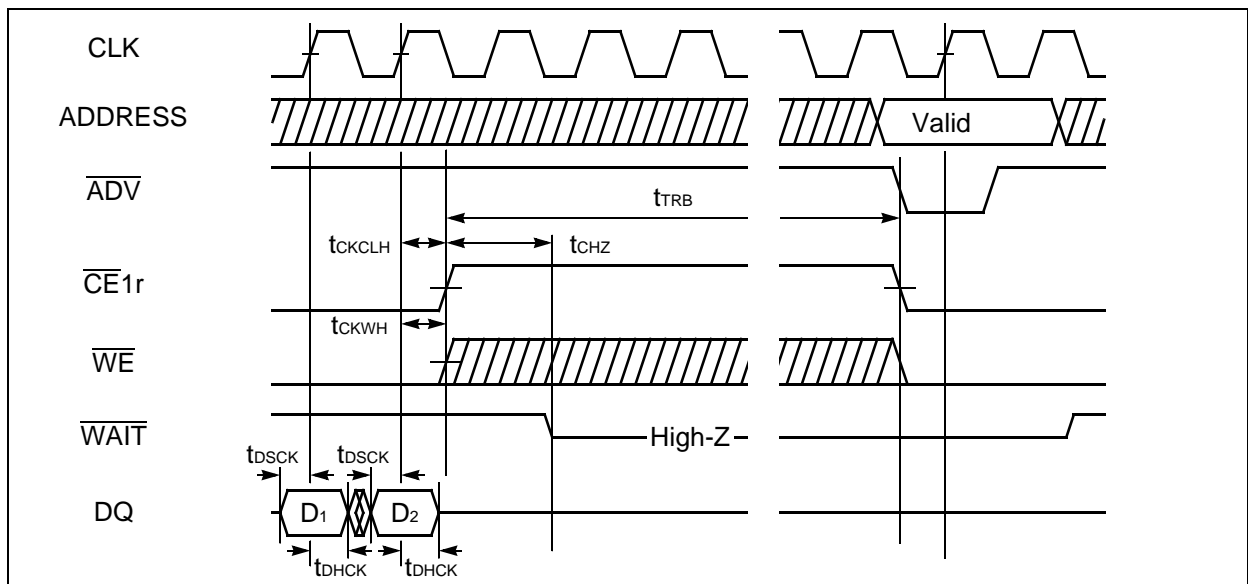
3. AC Characteristics (Under Recommended Operating Conditions unless otherwise noted)

• Asynchronous Read Operation (Page mode)

Parameter	Symbol	Value Min	Value Max	Unit	Notes
Read Cycle Time	t_{RC}	70	1000	ns	*1, *2
$\overline{CE}$1r Access Time	t_{CE}	—	70	ns	*3
$\overline{OE}$ Access Time	t_{OE}	—	40	ns	*3
Address Access Time	t_{AA}	—	70	ns	*3, *5
$\overline{ADV}$ Access Time	t_{AV}		70	ns	*3
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	—	30	ns	*3
Page Address Access Time	t_{PAA}	—	20	ns	*3, *6
Page Read Cycle Time	t_{PRC}	20	1000	ns	*1, *6, *7
Output Data Hold Time	t_{OH}	5	—	ns	*3
$\overline{CE}$1r Low to Output Low-Z	t_{CLZ}	5	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	0	—	ns	*4
$\overline{LB}$, $\overline{UB}$ Low to Output Low-Z	t_{BLZ}	0	—	ns	*4
$\overline{CE}$1r High to Output High-Z	t_{CHZ}	—	20	ns	*3
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	20	ns	*3
$\overline{LB}$, $\overline{UB}$ High to Output High-Z	t_{BHZ}	—	20	ns	*3
Address Setup Time to $\overline{CE}$1r Low	t_{ASC}	–5	—	ns	
Address Setup Time to $\overline{OE}$ Low	t_{ASO}	10	—	ns	
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*8
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	5	—	ns	
Address Invalid Time	t_{AX}	—	10	ns	*5, *9
Address Hold Time from $\overline{CE}$1r High	t_{CHAH}	–5	—	ns	*10
Address Hold Time from $\overline{OE}$ High	t_{OHAH}	–5	—	ns	
$\overline{CE}$1r High Pulse Width	t_{CP}	15	—	ns	

*1 : Maximum value is applicable if $\overline{CE}$1r is kept at Low without change of address input of A_3 to A_{22}.
If needed by system operation, please contact local FUJITSU representative for the relaxation of 1µs limitation.

*2 : Address should not be changed within minimum t_{RC}.

*3 : The output load 50 pF with 50 Ω termination to V_{CCQ}r × 0.5 V.

*4 : The output load 5pF without any other load.

*5 : Applicable to A_3 to A_{22} when $\overline{CE}$1r is kept at Low.

*6 : Applicable only to A_0, A_1 and A_2 when $\overline{CE}$1r is kept at Low for the page address access.

*7 : In case Page Read Cycle is continued with keeping $\overline{CE}$1r stays Low, $\overline{CE}$1r must be brought to High within 4 µs. In other words, Page Read Cycle must be closed within 4 µs.

*8 : t_{VPL} is specified from the negative edge of either $\overline{CE}$1r or $\overline{ADV}$ whichever comes late.

*9 : Applicable when at least two of address inputs among applicable are switched from previous state.

*10 : t_{RC} (Min) and t_{PRC} (Min) must be satisfied.

- **Asynchronous Write Operation**

Parameter	Symbol	Value Min	Value Max	Unit	Notes
Write Cycle Time	t_{WC}	70	1000	ns	*1, *2
Address Setup Time	t_{AS}	0	—	ns	*3
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*4
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	5	—	ns	
$\overline{CE}1r$ Write Pulse Width	t_{CW}	45	—	ns	*3
$\overline{WE}$ Write Pulse Width	t_{WP}	45	—	ns	*3
$\overline{LB}$, $\overline{UB}$ Write Pulse Width	t_{BW}	45	—	ns	*3
$\overline{CE}1r$ Write Recovery Time	t_{WRC}	15	—	ns	*5
$\overline{WE}$ Write Recovery Time	t_{WR}	15	1000	ns	*5
$\overline{LB}$, $\overline{UB}$ Write Recovery Time	t_{BR}	15	1000	ns	*5
Data Setup Time	t_{DS}	15	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
$\overline{OE}$ High to $\overline{CE}1r$ Low Setup Time for Write	t_{OHCL}	–5	—	ns	*6
$\overline{OE}$ High to Address Setup Time for Write	t_{OES}	0	—	ns	*7
$\overline{LB}$, $\overline{UB}$ Write Pulse Overlap	t_{BWO}	30	—	ns	
$\overline{CE}1r$ High Pulse Width	t_{CP}	15	—	ns	

*1 : Maximum value is applicable if $\overline{CE}1r$ is kept at Low without any address change. If the relaxation is needed by system operation, please contact local FUJITSU representative for the relaxation of 1µs limitation.

*2 : Minimum value must be equal or greater than the sum of write pulse (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WRC}, t_{WR} or t_{BR}).

*3 : Write pulse is defined from High to Low transition of $\overline{CE}1r$, $\overline{WE}$ or $\overline{LB}$ / $\overline{UB}$, whichever occurs last.

*4 : t_{VPL} is specified from the negative edge of either $\overline{CE}1r$ or $\overline{ADV}$ whichever comes late.

*5 : Write recovery is defined from Low to High transition of $\overline{CE}1r$, $\overline{WE}$ or $\overline{LB}$ / $\overline{UB}$, whichever occurs first.

*6 : If $\overline{OE}$ is Low after minimum t_{OHCL}, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High within 5 ns after $\overline{CE}1r$ is brought to Low. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met.

*7 : If $\overline{OE}$ is Low after new address input, read cycle is initiated. In other word, $\overline{OE}$ must be brought to High at the same time or before new address valid. Once read cycle is initiated, new write pulse should be input after minimum t_{RC} is met and data bus is in High-Z.

- **Synchoronous Operation - Clock Input (Burst mode)**

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Clock Period	RL = 5	t_{CK}	13	—	ns	*1
	RL = 4		18	—	ns	*1
	RL = 3		30	—	ns	*1
Clock High Time		t_{CKH}	4	—	ns	
Clock Low Time		t_{CKL}	4	—	ns	
Clock Rise/Fall Time		t_{CKT}	—	3	ns	*2

*1 : Clock period is defined between valid clock edge.

*2 : Clock rise/fall time is defined between V_{IH} Min and V_{IL} Max.

- **Synchronous Operation - Address Latch (Burst mode)**

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Address Setup Time to $\overline{ADV}$ Low	t_{ASVL}	–5	—	ns	*1
Address Setup Time to $\overline{CE}1r$ Low	t_{ASCL}	–5	—	ns	*1
Address Hold Time from $\overline{ADV}$ High	t_{AHV}	5	—	ns	
$\overline{ADV}$ Low Pulse Width	t_{VPL}	10	—	ns	*2
$\overline{ADV}$ Low Setup Time to CLK	t_{VSCK}	5	—	ns	*3
$\overline{ADV}$ Low Setup Time to $\overline{CE}1r$ Low	t_{VLCL}	5	—	ns	*1
$\overline{CE}1$ Low Setup Time to CLK	t_{CLCK}	5	—	ns	*3
$\overline{ADV}$ Low Hold Time from CLK	t_{CKVH}	1	—	ns	*3
Burst End $\overline{ADV}$ High Hold Time from CLK	t_{VHVL}	13	—	ns	

*1 : t_{ASCL} is applicable if $\overline{CE}1$ brought to Low after $\overline{ADV}$ is brought to Low under the condition where t_{VLCL} is satisfied. The both of t_{ASCL} and t_{ASVL} must be satisfied if t_{VLCL} is not satisfied.

*2 : t_{VPL} is specified from the negative edge of either $\overline{CE}1$ or $\overline{ADV}$ whichever comes late.

*3 : Applicable to the 1st valid clock edge.

- **Synchronous Read Operation (Burst mode)**

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Burst Read Cycle Time		t_{RCB}	—	8000	ns	
CLK Access Time		t_{AC}	—	11	ns	*1
Output Hold Time from CLK		t_{CKQX}	3	—	ns	*1
$\overline{CE}$1r Low to $\overline{WAIT}$ Low		t_{CLTL}	5	20	ns	*1
$\overline{OE}$ Low to $\overline{WAIT}$ Low		t_{OLTL}	0	20	ns	*1
$\overline{ADV}$ Low to $\overline{WAIT}$ Low		t_{VLTL}	0	20	ns	*1
CLK to $\overline{WAIT}$ Valid Time		t_{CKTV}	—	11	ns	*1
$\overline{WAIT}$ Valid Hold Time from CLK		t_{CKTX}	3	—	ns	*1
$\overline{CE}$1r Low to Output Low-Z		t_{CLZ}	5	—	ns	*2
$\overline{OE}$ Low to Output Low-Z		t_{OLZ}	0	—	ns	*2
$\overline{LB}$, $\overline{UB}$ Low to Output Low-Z		t_{BLZ}	0	—	ns	*2
$\overline{CE}$1r High to Output High-Z		t_{CHZ}	—	20	ns	*1
$\overline{OE}$ High to Output High-Z		t_{OHZ}	—	20	ns	*1
$\overline{LB}$, $\overline{UB}$ High to Output High-Z		t_{BHZ}	—	20	ns	*1
$\overline{CE}$1r High to $\overline{WAIT}$ High-Z		t_{CHTZ}	—	20	ns	*1
$\overline{OE}$ High to $\overline{WAIT}$ High-Z		t_{OHTZ}	—	20	ns	*1
$\overline{OE}$ Low Setup Time to 1st Data-out		t_{OLQ}	30	—	ns	
$\overline{UB}$, $\overline{LB}$ Setup Time to 1st Data-out		t_{BSQ}	26	—	ns	*3
$\overline{OE}$ Setup Time to CLK		t_{OSCK}	5	—	ns	
$\overline{OE}$ Hold Time from CLK		t_{CKOH}	5	—	ns	
Burst End $\overline{CE}$1r Low Hold Time from CLK		t_{CKCLH}	5	—	ns	
Burst End $\overline{UB}$, $\overline{LB}$ Hold Time from CLK		t_{CKBH}	5	—	ns	
Burst Terminate Recovery Time	BL = 8,16	t_{TRB}	26	—	ns	*4
	BL = Continuous		70	—	ns	*4

*1 : The output load 50 pF with 50 Ω termination to V_{CCQ}r × 0.5 V.

*2 : The output load 5 pF without any other load.

*3 : Once they are determined, they must not be changed until the end of burst.

*4 : Defined from the Low to High transition of $\overline{CE}$1r to the High to Low transition of either $\overline{ADV}$ or $\overline{CE}$1r whichever occurs late.

- **Synchronous Write Operation (Burst mode)**

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Burst Write Cycle Time		t_{WCB}	—	8000	ns	
Data Setup Time to Clock		t_{DSCK}	5	—	ns	
Data Hold Time from CLK		t_{DHCK}	3	—	ns	
$\overline{WE}$ Low Setup Time to 1st Data In		t_{WLD}	30	—	ns	
$\overline{UB}$, $\overline{LB}$ Setup Time for Write		t_{BS}	–5	—	ns	*1
$\overline{WE}$ Setup Time to CLK		t_{WSCK}	5	—	ns	
$\overline{WE}$ Hold Time from CLK		t_{CKWH}	5	—	ns	
$\overline{CE}$1r Low to $\overline{WAIT}$ High		t_{CLTH}	5	20	ns	*2
$\overline{WE}$ Low to $\overline{WAIT}$ High		t_{WLTH}	0	20	ns	*2
$\overline{CE}$1r High to $\overline{WAIT}$ High-Z		t_{CHTZ}	—	20	ns	*2
$\overline{WE}$ High to $\overline{WAIT}$ High-Z		t_{WHTZ}	—	20	ns	*2
Burst End $\overline{CE}$1r Low Hold Time from CLK		t_{CKCLH}	5	—	ns	
Burst End $\overline{CE}$1r High Setup Time to next CLK		t_{CHCK}	5	—	ns	
Burst End $\overline{UB}$, $\overline{LB}$ Hold Time from CLK		t_{CKBH}	5	—	ns	
Burst Write Recovery Time		t_{WRB}	26		ns	*3
Burst Terminate Recovery Time	BL = 8,16	t_{TRB}	26	—	ns	*4
	BL = Continuous	t_{TRB}	70	—	ns	*4

*1 : Defined from the valid input edge to the High to Low transition of either $\overline{ADV}$, $\overline{CE}$1r, or $\overline{WE}$, whichever occurs last. And once they are determined, they must not be changed until the end of burst.

*2 : The output load 50 pF with 50 Ω termination to V_{CCQ}r × 0.5 V.

*3 : The output load 5 pF without any other load.

*4 : Defined from the valid clock edge where last data-in being latched at the end of burst write to the High to Low transition of either $\overline{ADV}$ or $\overline{CE}$1r whichever occurs late for the next access.

*5 : Defined from the Low to High transition of $\overline{CE}$1r to the High to Low transition of either $\overline{ADV}$ or $\overline{CE}$1r whichever occurs late for the next access.

- **Power Down Parameters**

Parameter	Symbol	Value		Unit	Note
		Min	Max		
CE2r Low Setup Time for Power Down Entry	t_{CSP}	20	—	ns	*1
CE2r Low Hold Time after Power Down Entry	t_{C2LP}	70	—	ns	*1
$\overline{CE}$1r High Hold Time following CE2r High after Power Down Exit [SLEEP mode only]	t_{CHH}	300	—	µs	*1
$\overline{CE}$1r High Hold Time following CE2r High after Power Down Exit [not in SLEEP mode]	t_{CHHP}	1	—	µs	*2
$\overline{CE}$1r High Setup Time following CE2r High after Power Down Exit	t_{CHS}	0	—	ns	*1

*1 : Applicable also to power-up.

*2 : Applicable when Partial mode is set.

- **Other Timing Parameters**

Parameter	Symbol	Value		Unit	Note
		Min	Max		
$\overline{CE}$1r High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{CE}$1r High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	10	—	ns	*1
CE2r High Hold Time after Power-up	t_{C2HL}	50	—	µs	
$\overline{CE}$1r High Hold Time following CE2r High after Power-up	t_{CHH}	300	—	µs	
Input Transition Time (except for CLK)	t_T	1	25	ns	*2, *3

*1 : Some data might be written into any address location if t_{CHWX} (Min) is not satisfied.

*2 : Except for clock input transition time.

*3 : The Input Transition Time (t_T) at AC testing is shown in below. If actual t_T is longer than specified values, it may violate AC specification of some timing parameters.

• **AC Test Conditions**

Description		Symbol	Test Setup	Value	Unit	Note
Input High Level		V_{IH}	—	$V_{CCQ}r \times 0.8$	V	
Input Low Level		V_{IL}	—	$V_{CCQ}r \times 0.2$	V	
Input Timing Measurement Level		V_{REF}	—	$V_{CCQ}r \times 0.5$	V	
Input Transition Time	Async.	t_T	Between V_{IL} and V_{IH}	5	ns	
	Sync.			3	ns	

• **AC MEASUREMENT OUTPUT LOAD CIRCUIT**
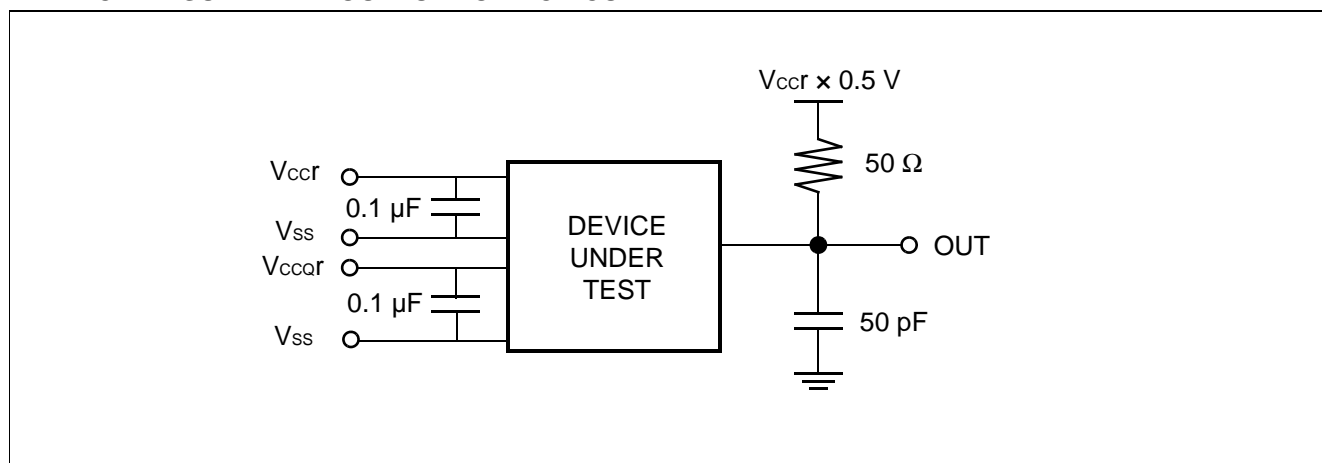
• **Asynchronous Read Timing #1-1 (Basic Timing)**

Note : This timing diagram assumes CE2r = H and $\overline{WE}$ = H.
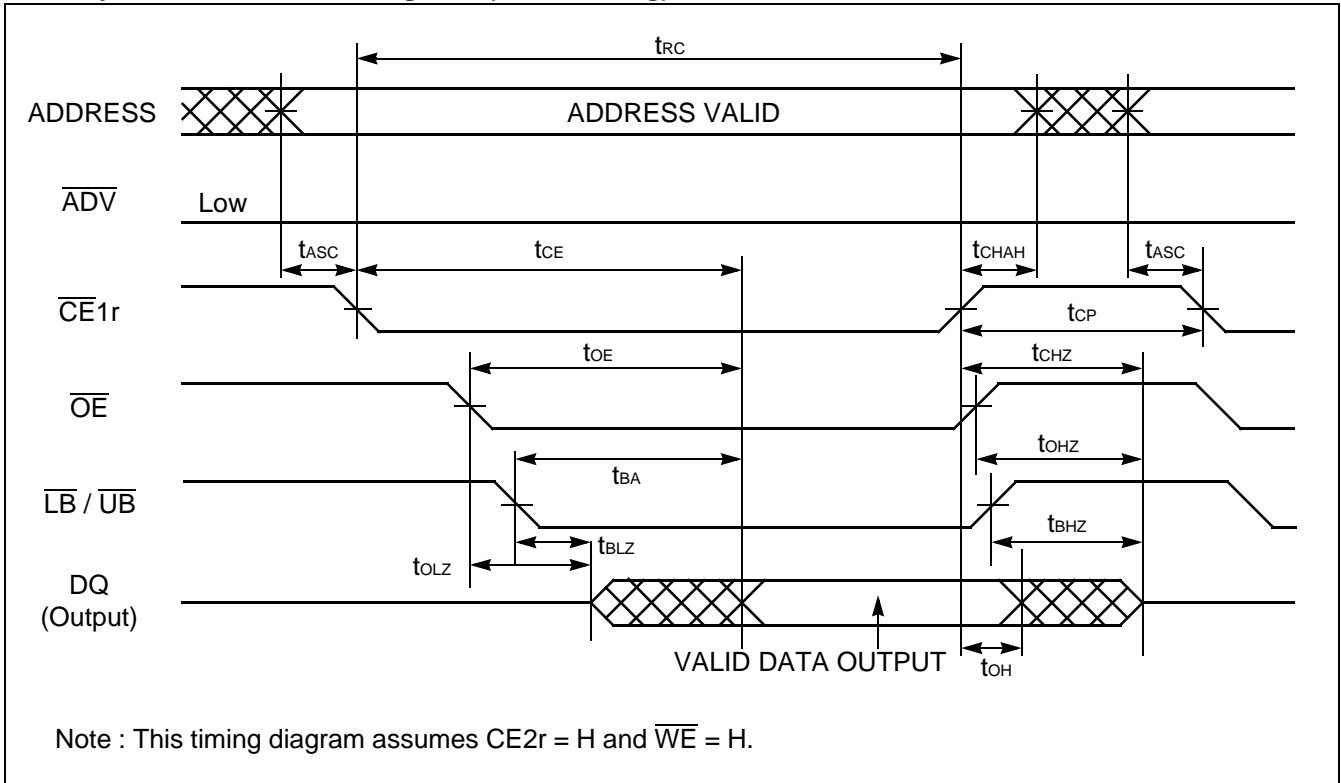
• **Asynchronous Read Timing #1-2 (Basic Timing)**

Note : This timing diagram assumes CE2r = H and $\overline{WE}$ = H.
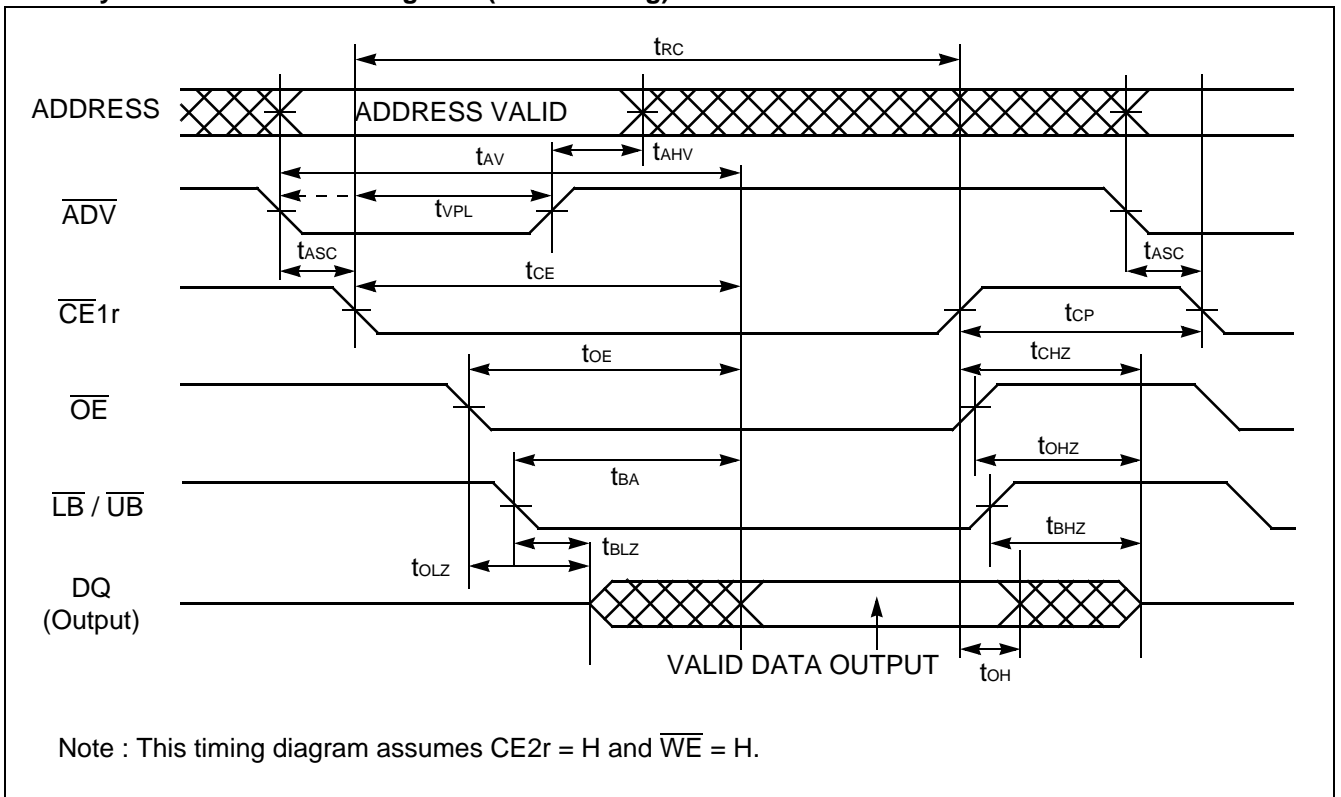
• **Asynchronous Read Timing #2 ($\overline{\text{OE}}$ & Address Access)**

Note : This timing diagram assumes CE2r = H, $\overline{\text{ADV}}$ = L and $\overline{\text{WE}}$ = H.
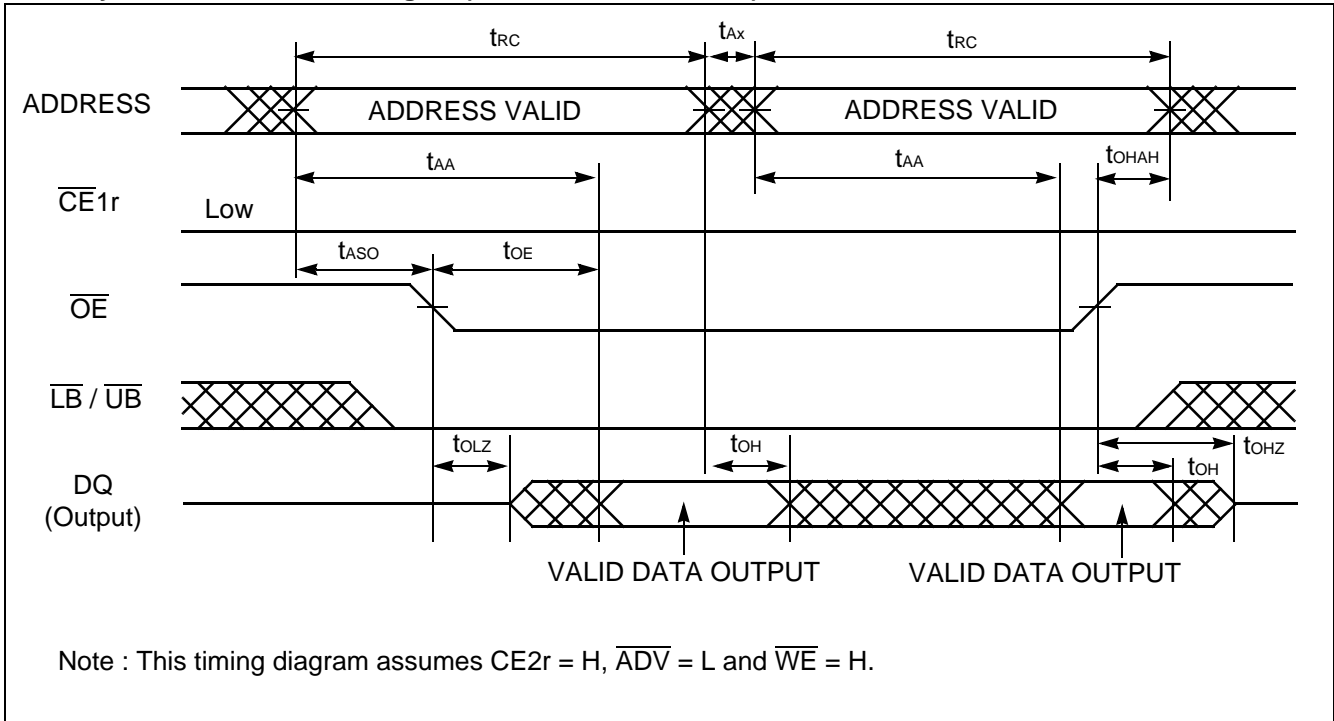
• **Asynchronous Read Timing #3 ($\overline{\text{LB}}$ / $\overline{\text{UB}}$ Byte Access)**

Note : This timing diagram assumes CE2r = H, $\overline{\text{ADV}}$ = L and $\overline{\text{WE}}$ = H.
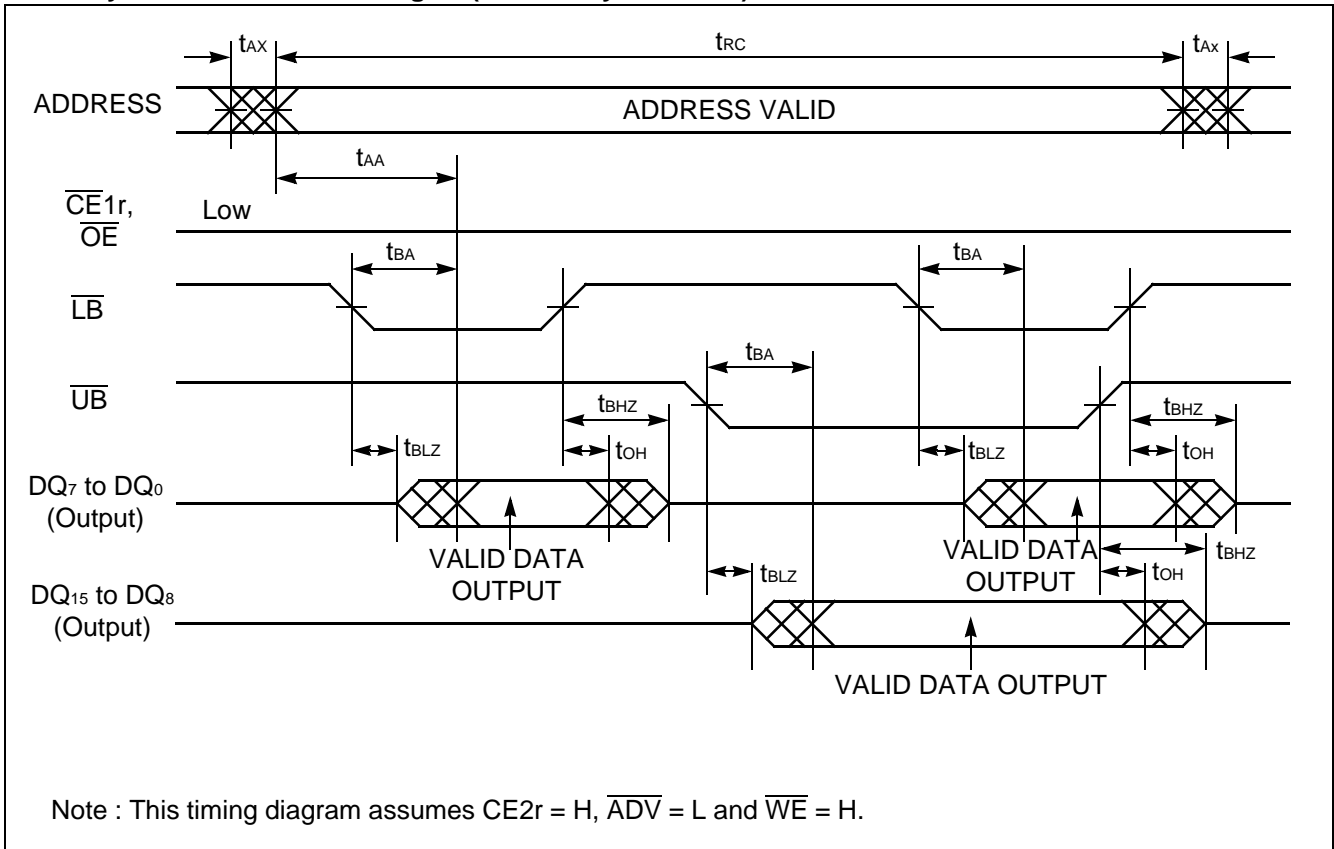
• **Asynchronous Read Timing #4 (Page Address Access after $\overline{CE}$1r Control Access)**

Note : This timing diagram assumes CE2r = H and $\overline{WE}$ = H.
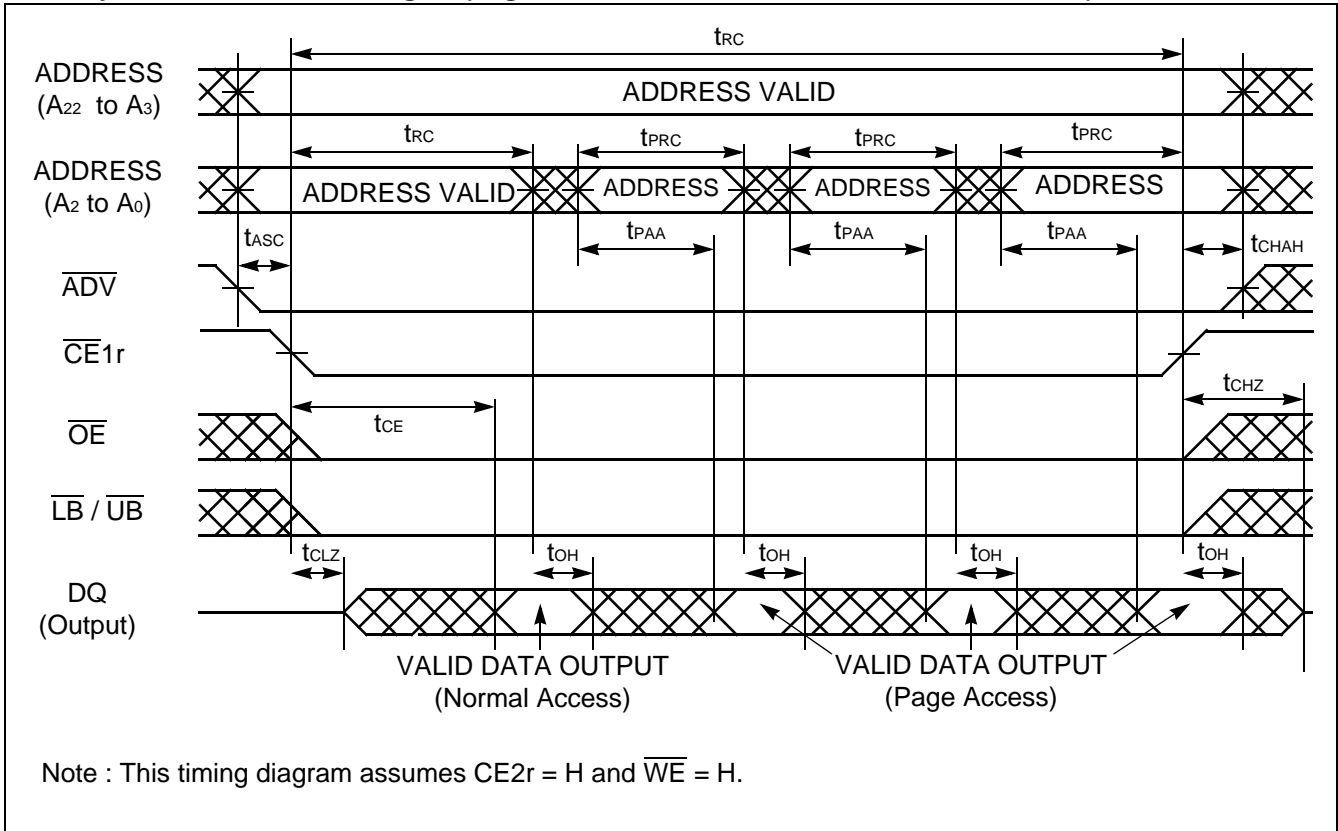
• **Asynchronous Read Timing #5 (Random and Page Address Access)**

Notes : • This timing diagram assumes CE2r = H, $\overline{ADV}$ = L and $\overline{WE}$ = H.
 • Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE}$1r and $\overline{OE}$ are Low.
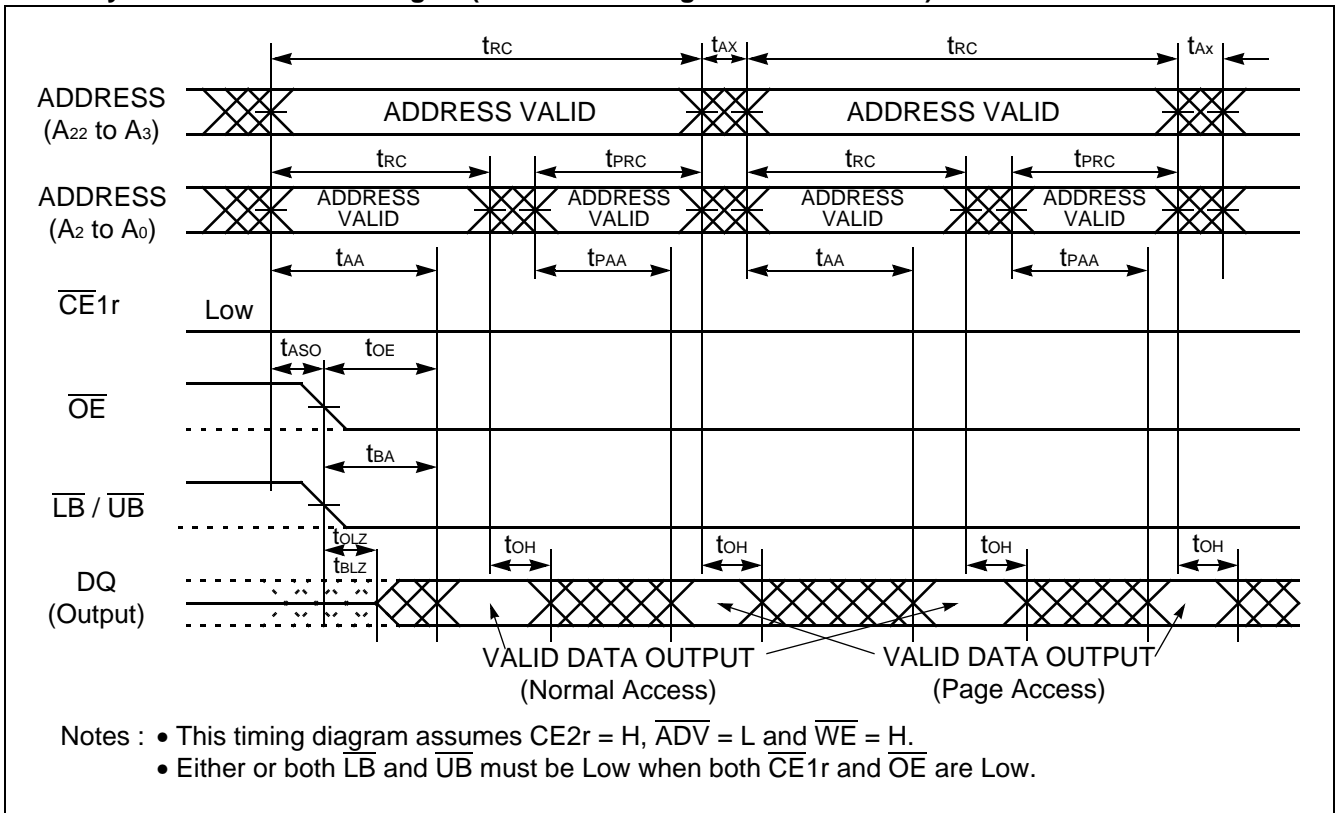
• **Asynchronous Write Timing #1-1 (Basic Timing)**

ADDRESS

ADDRESS VALID

t_{WC}

$\overline{ADV}$ Low

$\overline{CE}1r$

t_{AS} t_{CW} t_{WRC} t_{AS}

$\overline{WE}$

t_{AS} t_{WP} t_{WR} t_{AS}

$\overline{LB}, \overline{UB}$

t_{AS} t_{BW} t_{BR} t_{AS}

t_{OHCL}

$\overline{OE}$

t_{DS} t_{DH}

DQ (Input)

VALID DATA INPUT

Note : This timing diagram assumes CE2r = H and $\overline{ADV}$ = L.
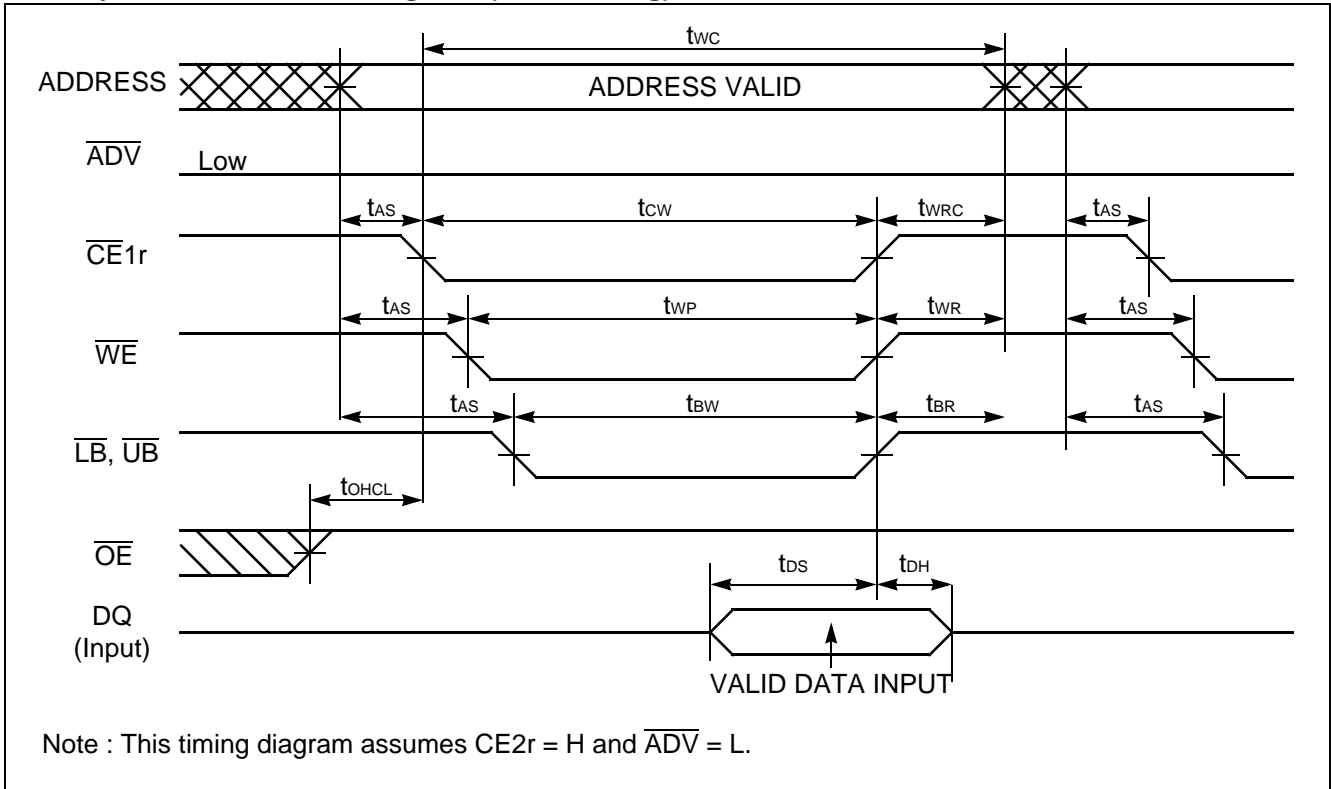
• **Asynchronous Write Timing #1-2 (Basic Timing)**

ADDRESS

ADDRESS VALID

t_{WC}

$\overline{ADV}$

$t_{VP04.3.12L}$ t_{AHV}

$\overline{CE}1r$

t_{AS} t_{CW} t_{WRC} t_{AS}

$\overline{WE}$

t_{AS} t_{WP} t_{WR} t_{AS}

$\overline{LB}, \overline{UB}$

t_{AS} t_{BW} t_{BR} t_{AS}

t_{OHCL}

$\overline{OE}$

t_{DS} t_{DH}

DQ (Input)

VALID DATA INPUT

Note : This timing diagram assumes CE2r = H.

74

- **Asynchronous Write Timing #2 ($\overline{WE}$ Control)**

Note : This timing diagram assumes CE2r = H and $\overline{ADV}$ = L.

- **Asynchronous Write Timing #3-1 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control)**

Note : This timing diagram assumes CE2r = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.
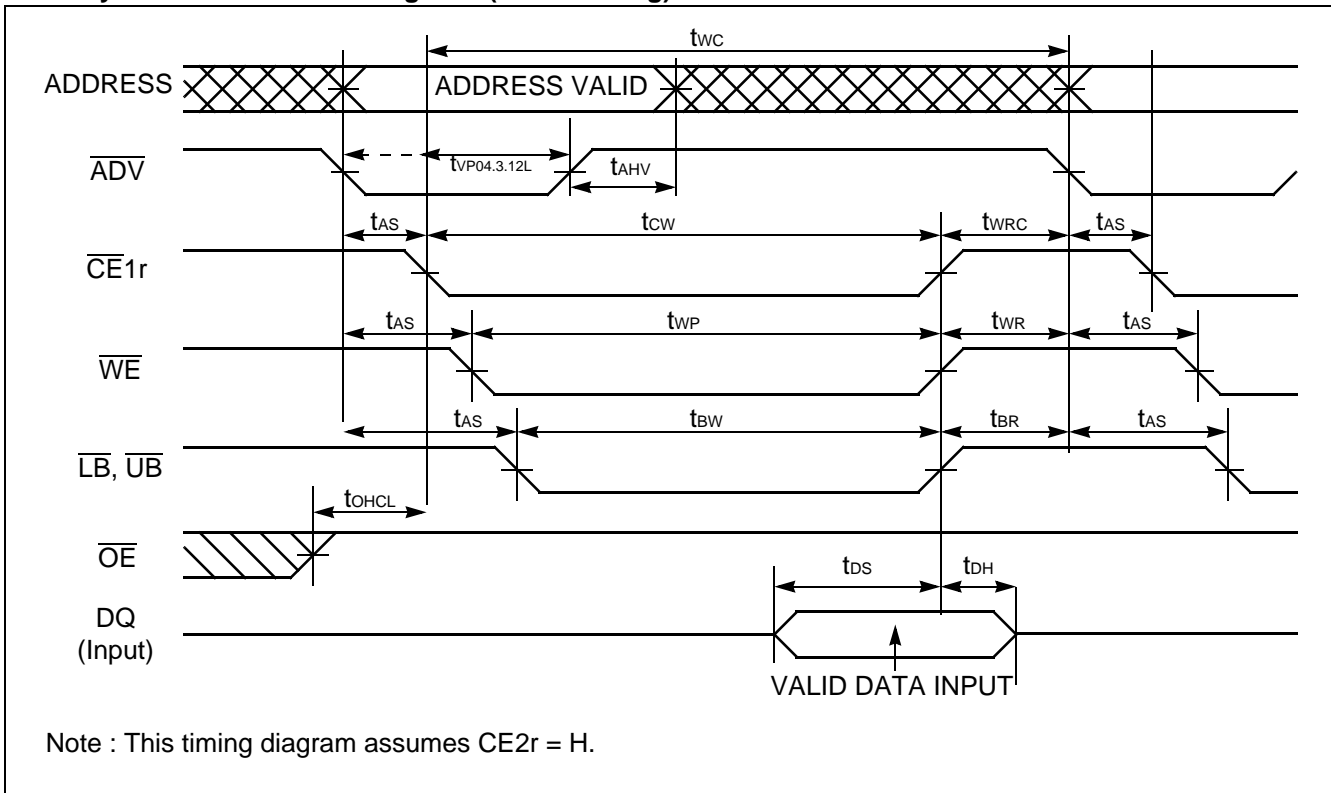
- **Asynchronous Write Timing #3-2 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control)**

Note : This timing diagram assumes CE2r = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.
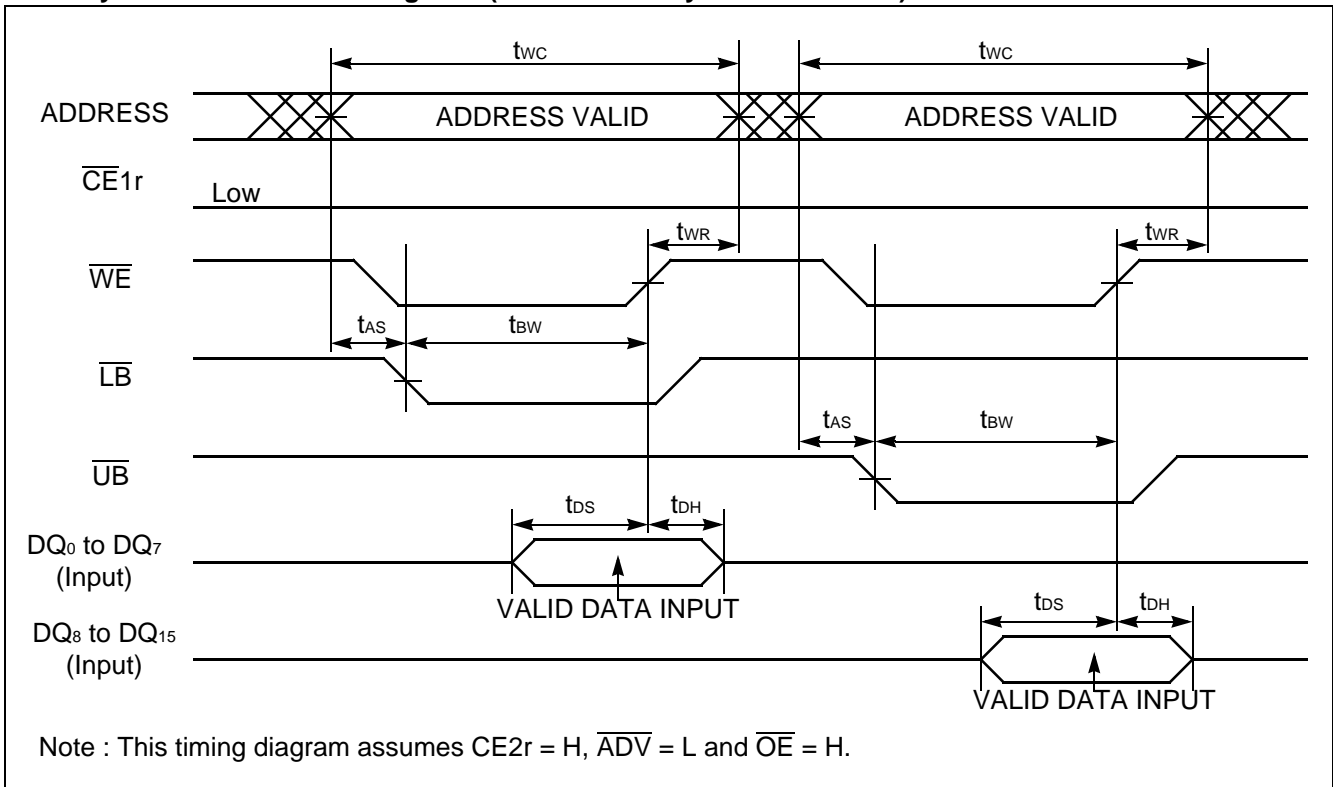
- **Asynchronous Write Timing #3-3 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control)**

Note : This timing diagram assumes CE2r = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.
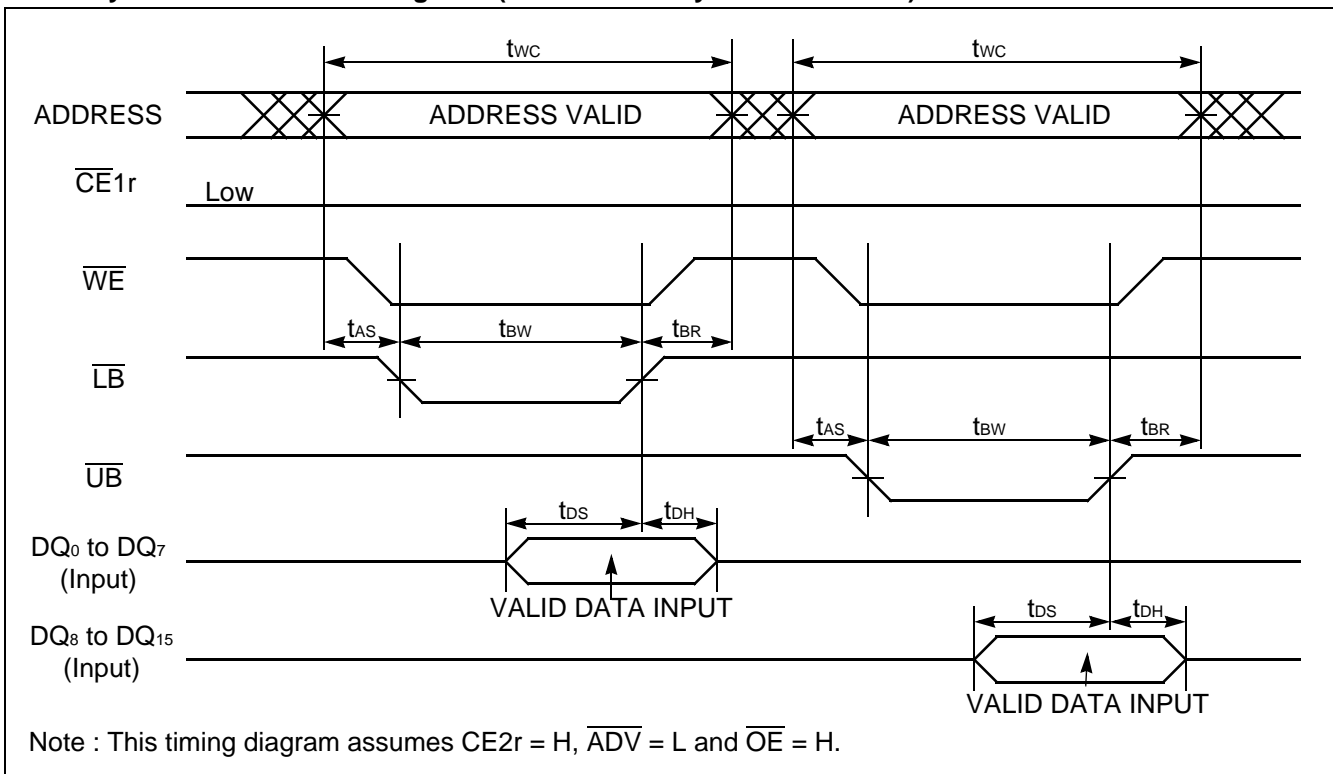
• **Asynchronous Write Timing #3-4 ($\overline{WE}$ / $\overline{LB}$ / $\overline{UB}$ Byte Write Control)**

Note : This timing diagram assumes CE2r = H, $\overline{ADV}$ = L and $\overline{OE}$ = H.
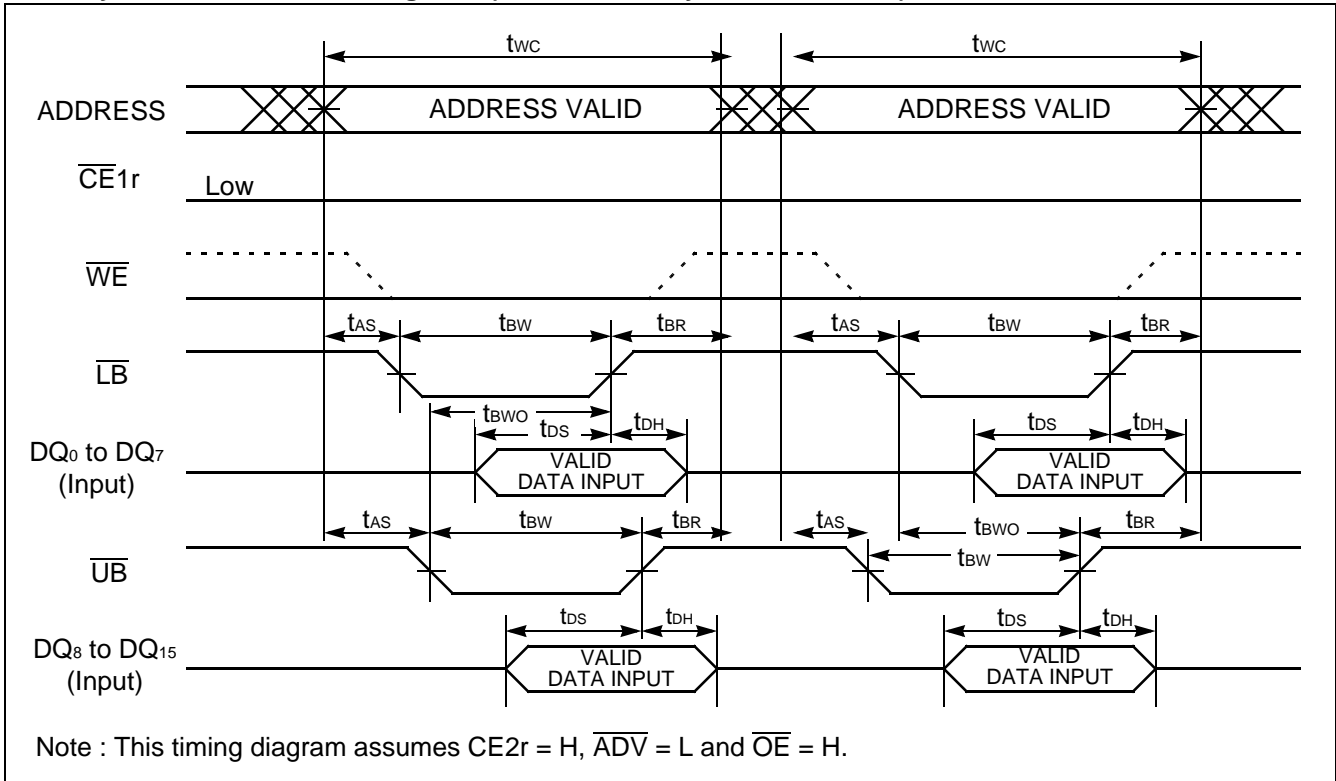
• **Asynchronous Read / Write Timing #1-1 ($\overline{CE}$1r Control)**

Notes : • This timing diagram assumes CE2r = H and $\overline{ADV}$ = L.
       • Write address is valid from either $\overline{CE}$1r or $\overline{WE}$ of last falling edge.
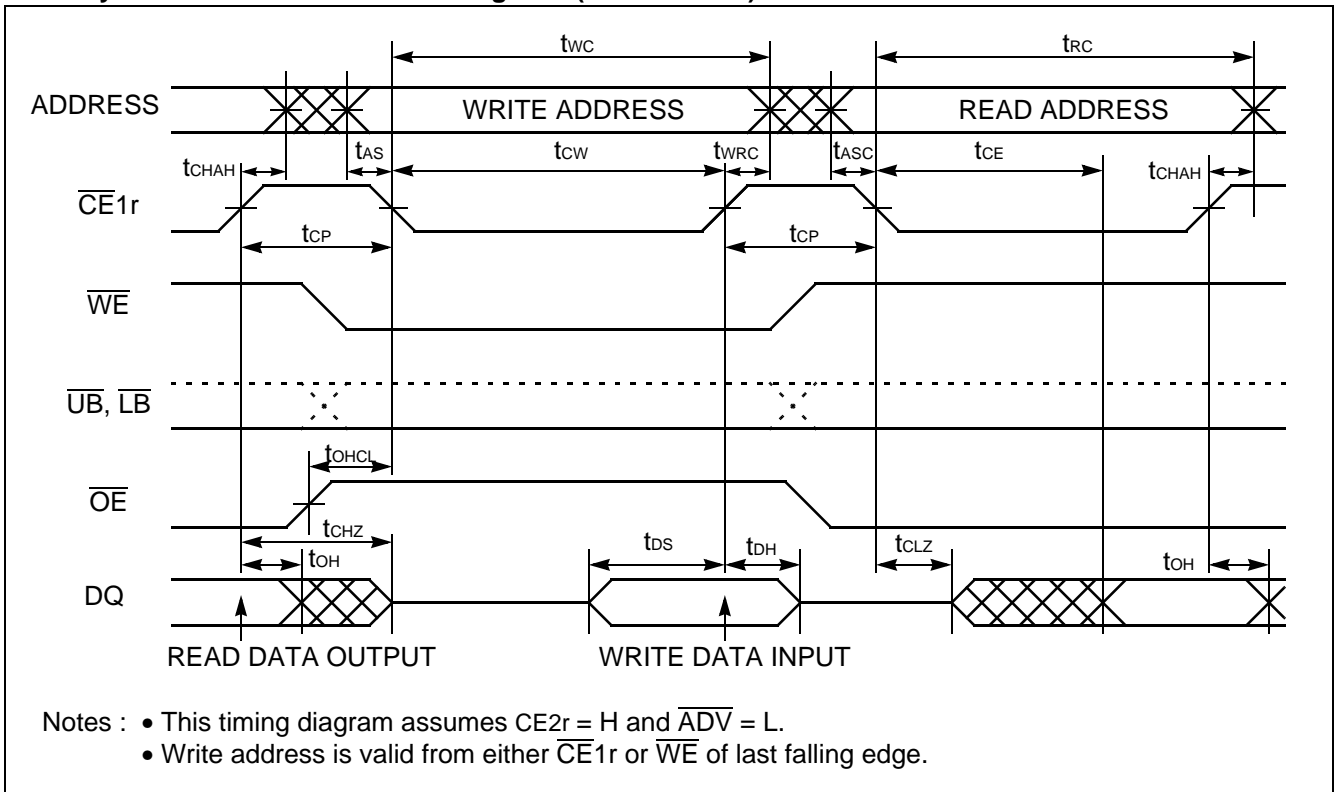
- **Asynchronous Read / Write Timing #1-2 ($\overline{CE}$1r / $\overline{WE}$ / $\overline{OE}$ Control)**
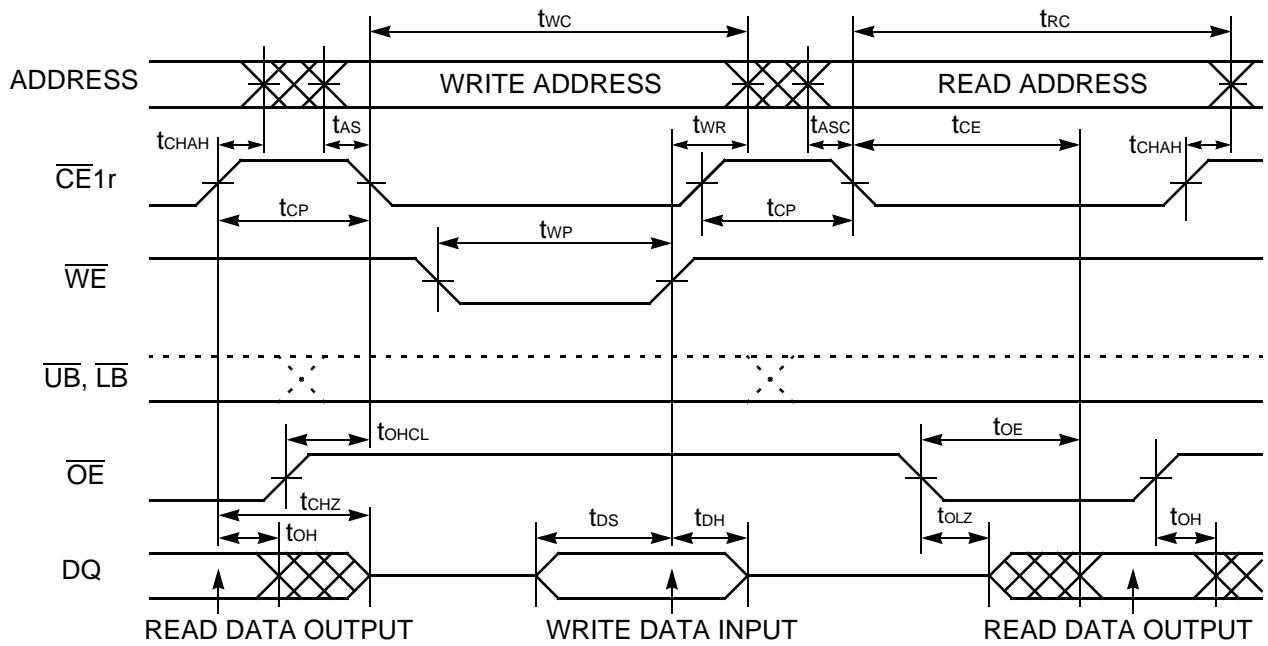
Notes : • This timing diagram assumes CE2r = H and $\overline{ADV}$ = L.
- $\overline{OE}$ can be fixed Low during write operation if it is $\overline{CE}$1r controlled write at Read-Write-Read sequence.

- **Asynchronous Read / Write Timing #2 ($\overline{OE}$, $\overline{WE}$ Control)**
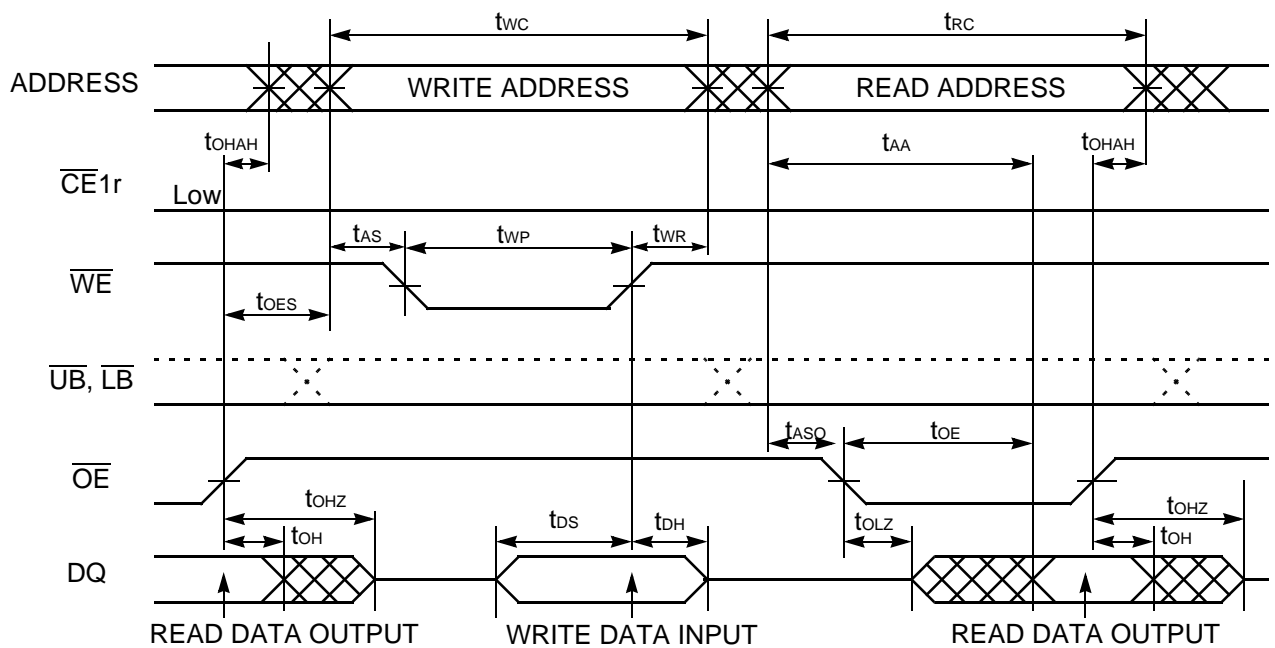
Notes : • This timing diagram assumes CE2r = H and $\overline{ADV}$ = L.
- $\overline{CE}$1r can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

- **Asynchronous Read / Write Timing #3 ($\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Control)**

t_{WC}

t_{RC}

ADDRESS   WRITE ADDRESS   READ ADDRESS

t_{AA}

$\overline{CE}1r$ Low t_{OHAH} t_{OHAH}

$\overline{WE}$

t_{OES} t_{AS} t_{BW} t_{BR} t_{BA}

$\overline{UB}$, $\overline{LB}$

t_{BHZ} t_{ASO}

$\overline{OE}$

t_{DS} t_{DH} t_{BLZ} t_{BHZ}

t_{OH} t_{OH}

DQ

READ DATA OUTPUT   WRITE DATA INPUT   READ DATA OUTPUT

Notes : • This timing diagram assumes CE2r = H and $\overline{ADV}$ = L.
  • $\overline{CE}1r$ can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

- **Clock Input Timing**

t_{CK}

CLK

t_{CK} t_{CKH} t_{CKL} t_{CKT} t_{CKT}

Notes : • Stable clock input must be required during $\overline{CE}1r$ = L.
  • t_{CK} is defined between valid clock edge.
  • t_{CKT} is defined between V_{IH} Min and V_{IL} Max.

• **Address Latch Timing (Synchronous Mode)**
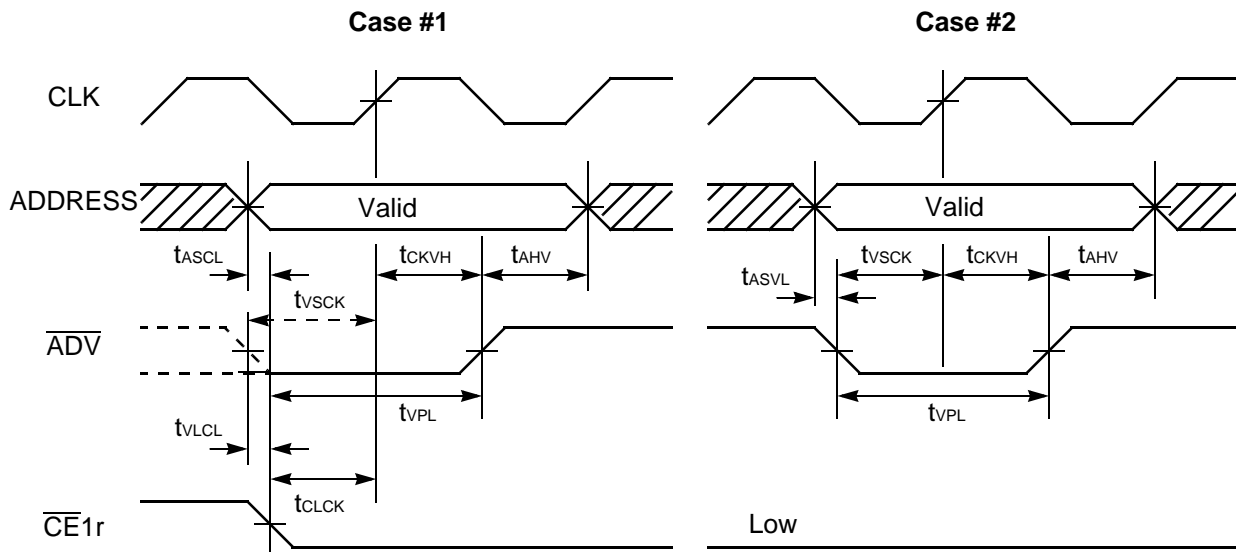
Notes : • Case #1 is the timing when $\overline{CE}$1r is brought to Low after $\overline{ADV}$ is brought to Low.
Case #2 is the timing when $\overline{ADV}$ is brought to Low after $\overline{CE}$1r is brought to Low.
• t$_{VPL}$ is specified from the negative edge of either $\overline{CE}$1r or $\overline{ADV}$ whichever comes late.
At least one valid clock edge must be input during $\overline{ADV}$ = L.
• t$_{VSCK}$ and t$_{CLCK}$ are applied to the 1st valid clock edge during $\overline{ADV}$ = L.

• **Synchronous Read Timing #1 (OE Control)**
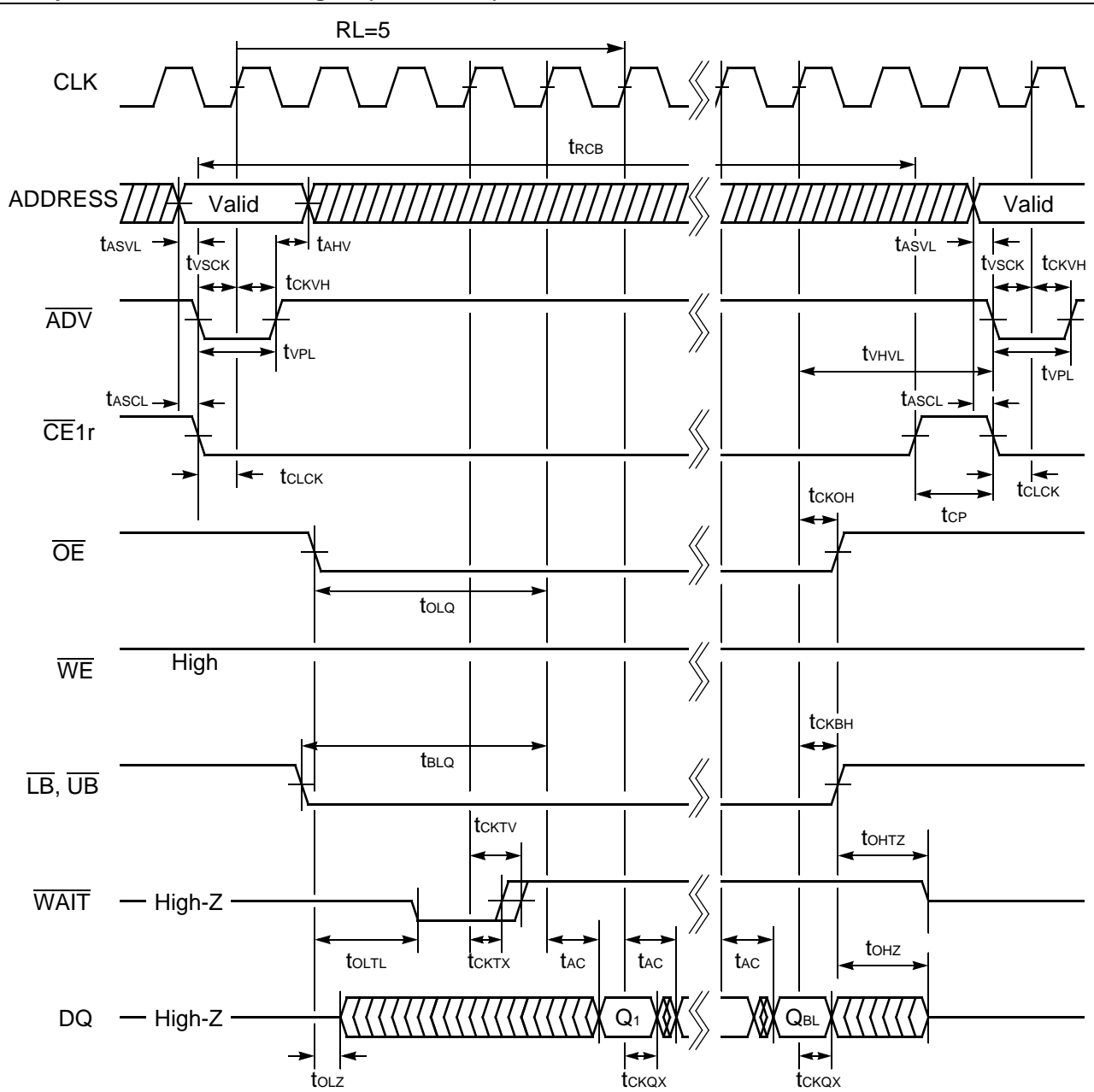
Note : This timing diagram assumes CE2r = H, the valid clock edge on rising edge and BL = 8 or 16.

- **Synchronous Read Timing #2 ($\overline{CE}$1r Control)**

Note : This timing diagram assumes CE2r = H, the valid clock edge on rising edge and BL = 8 or 16.
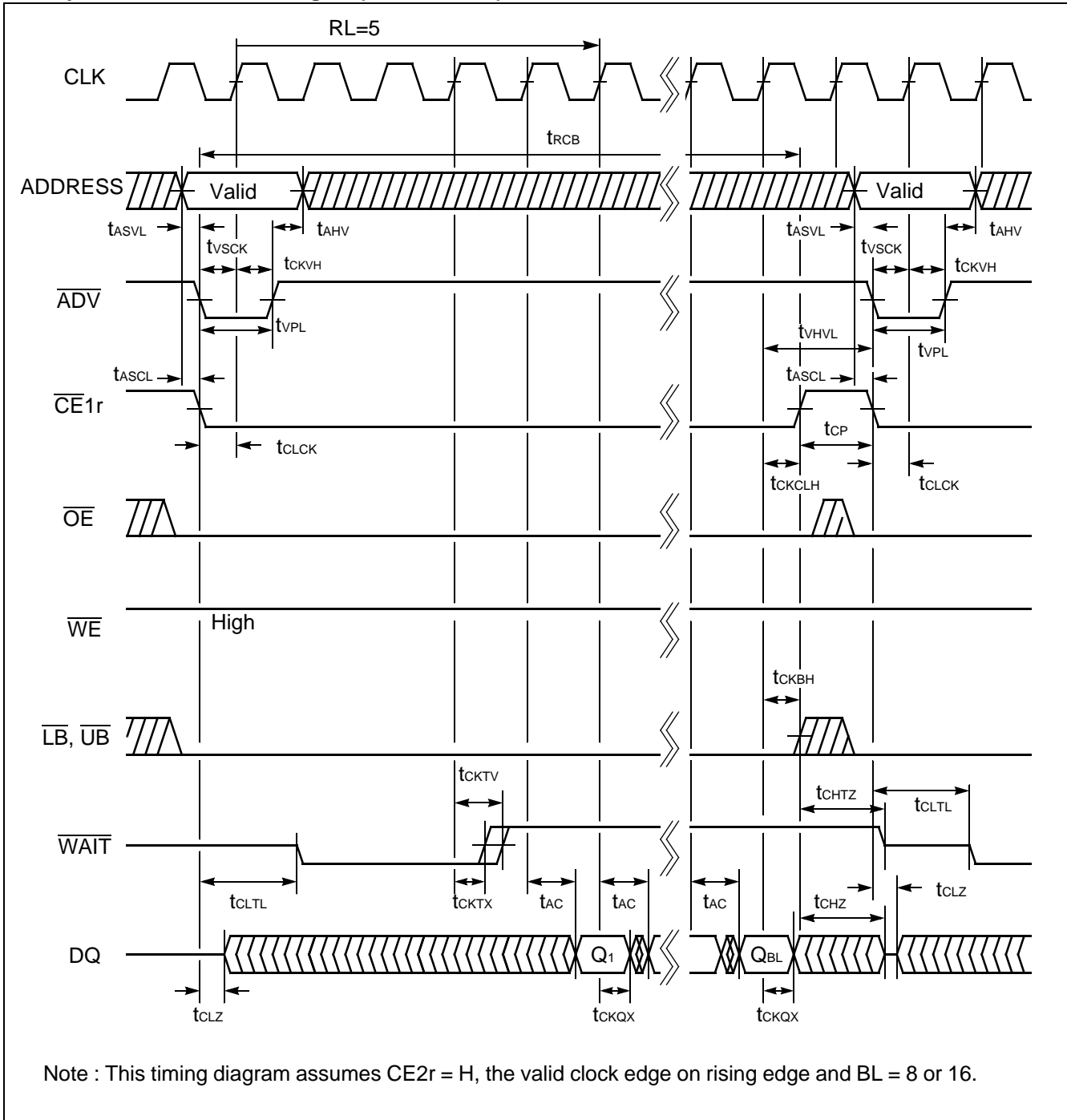
- **Synchronous Read Timing #3 ($\overline{\text{ADV}}$ Control)**
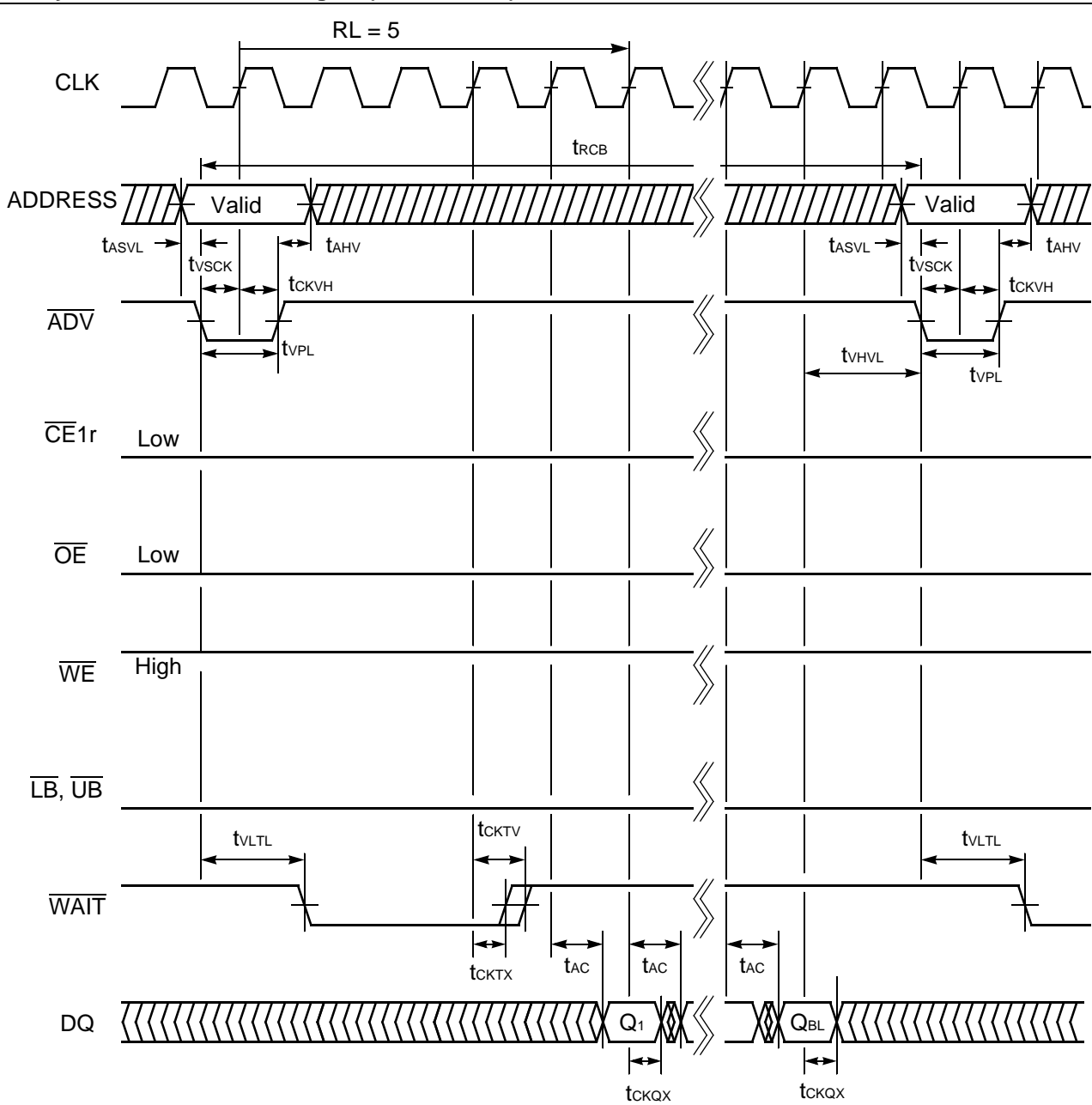
RL = 5

CLK

t_{RCB}

ADDRESS — Valid — Valid

t_{ASVL} t_{VSCK} t_{AHV} t_{ASVL} t_{VSCK} t_{AHV}

t_{CKVH} t_{CKVH}

$\overline{\text{ADV}}$

t_{VPL} t_{VHVL} t_{VPL}

$\overline{\text{CE}}$1r   Low

$\overline{\text{OE}}$ Low

$\overline{\text{WE}}$ High

$\overline{\text{LB}}$, $\overline{\text{UB}}$

t_{VLTL} t_{CKTV} t_{VLTL}

$\overline{\text{WAIT}}$

t_{CKTX} t_{AC} t_{AC} t_{AC}

DQ Q_1 Q_{BL}

t_{CKQX} t_{CKQX}

Note : This timing diagram assumes CE2r = H, the valid clock edge on rising edge and BL = 8 or 16.

• **Synchronous Write Timing #1 ($\overline{WE}$ Level Control)**

Note : This timing diagram assumes CE2r = H, the valid clock edge on rising edge and BL = 8 or 16.
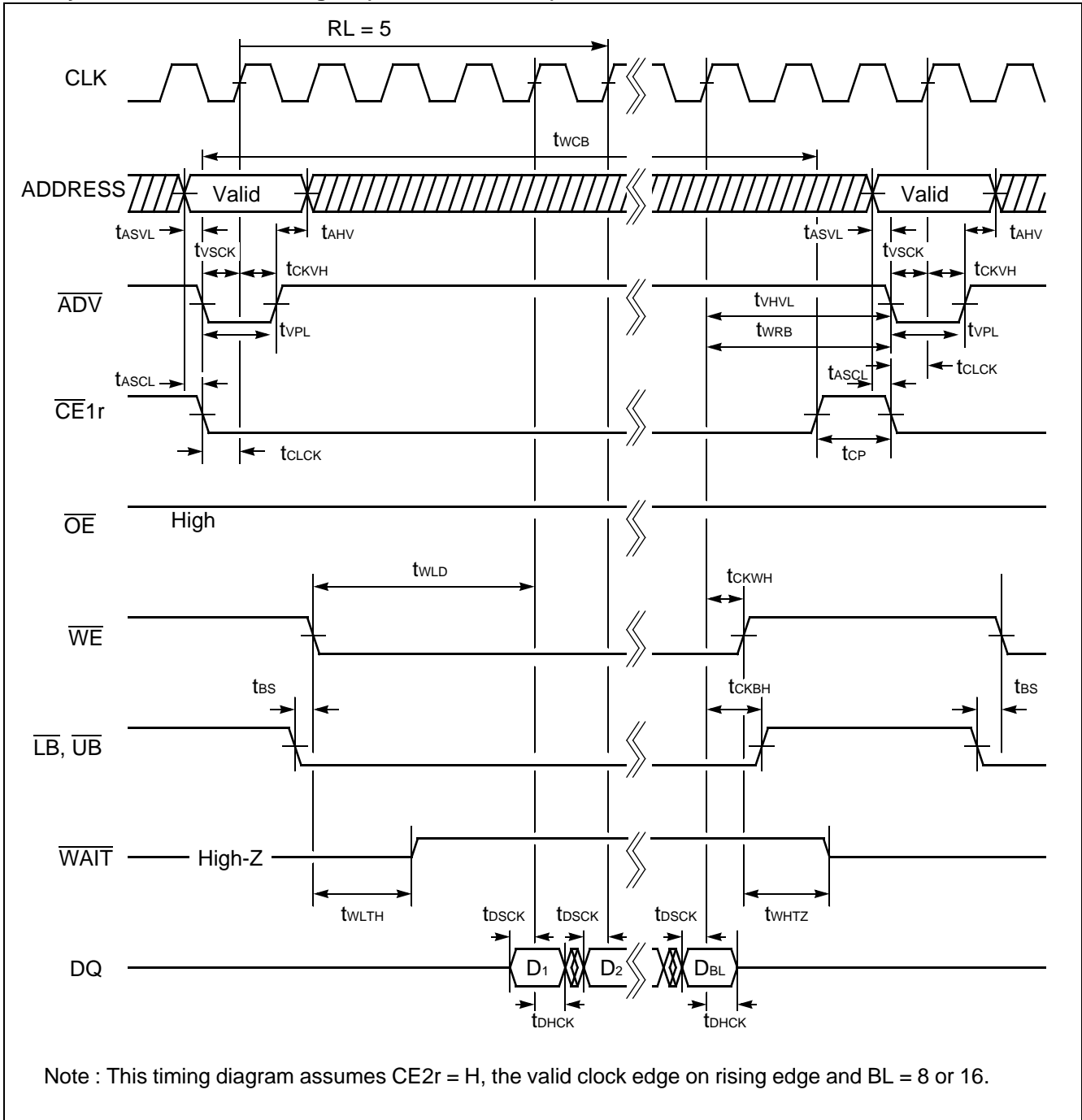
- **Synchronous Write Timing #2 ($\overline{WE}$ Single Clock Pulse Control)**
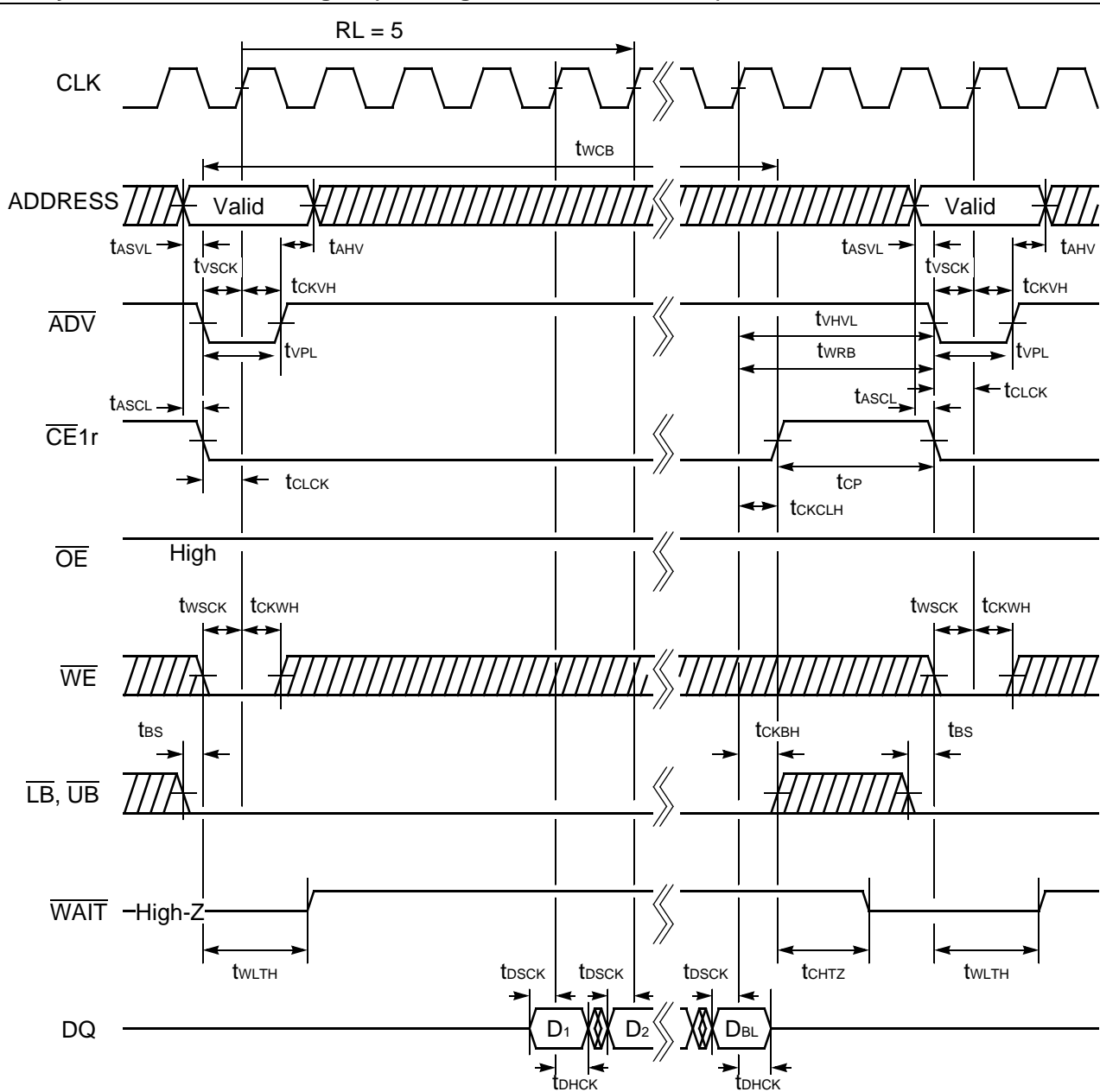
Note : This timing diagram assumes CE2r = H, the valid clock edge on rising edge and BL = 8 or 16.

• **Synchronous Write Timing #3 ($\overline{\text{ADV}}$ Control)**

Note : This timing diagram assumes CE2r = H, the valid clock edge on rising edge and BL = 8 or 16.
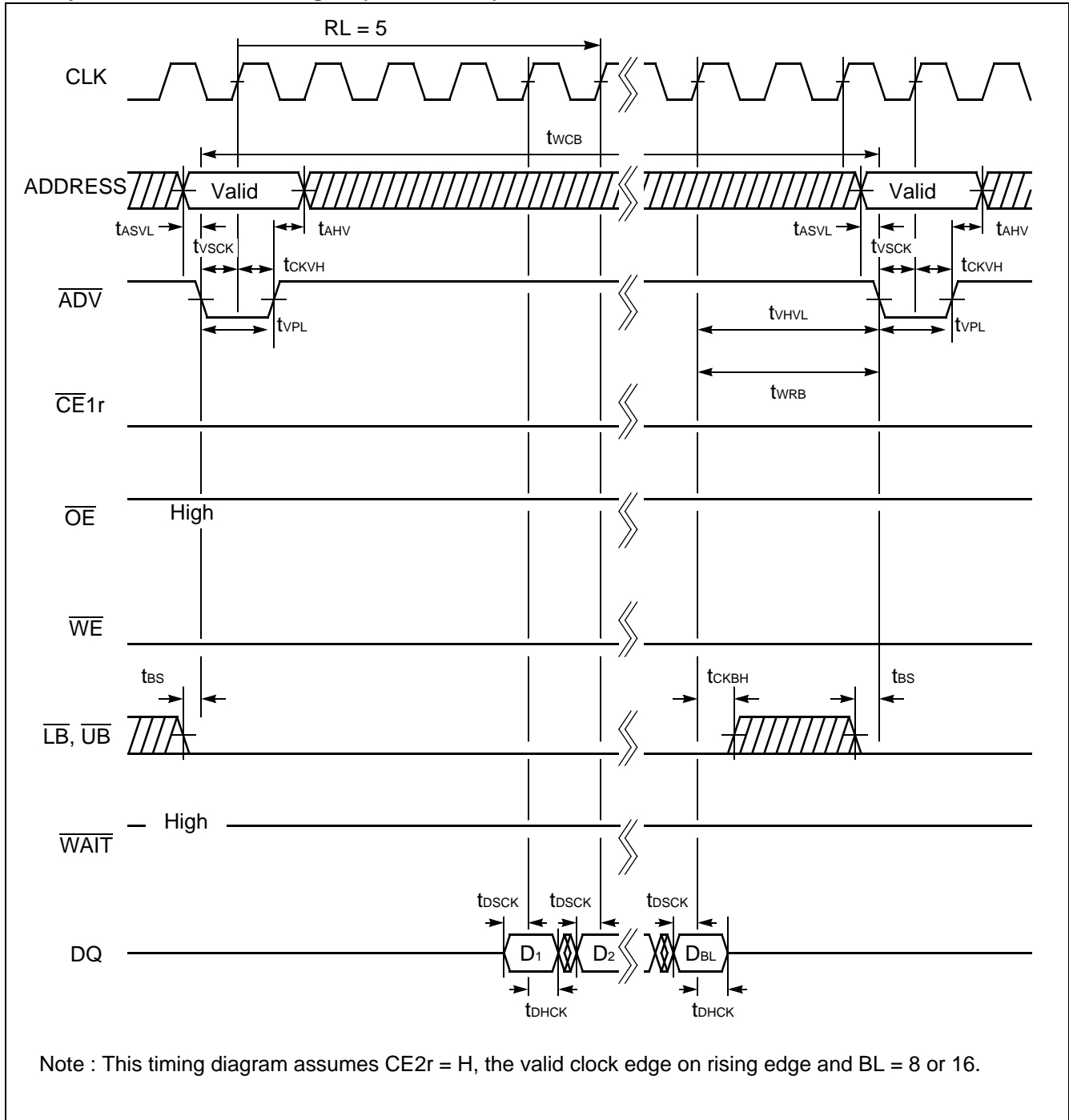
- **Synchronous Write Timing #4 ($\overline{\text{WE}}$ Level Control, Single Write)**
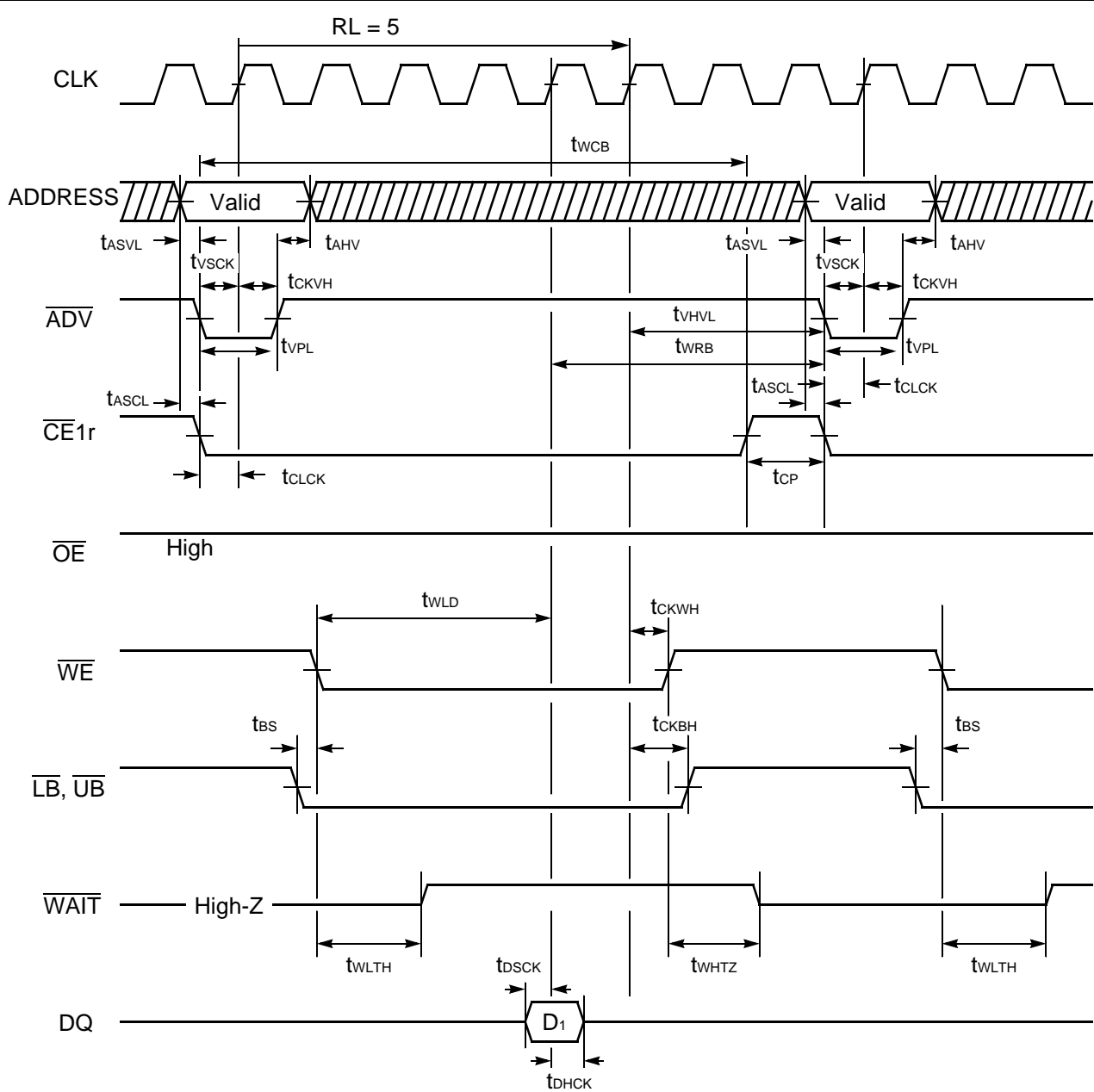
Notes : • This timing diagram assumes CE2r = H, the valid clock edge on rising edge and single write operation.
       • Write data is latched on the valid clock edge.

• **Synchronous Read to Write Timing #1 ($\overline{CE}$1 Control)**

Note : This timing diagram assumes CE2r = H, the valid clock edge on rising edge and BL = 8 or 16.
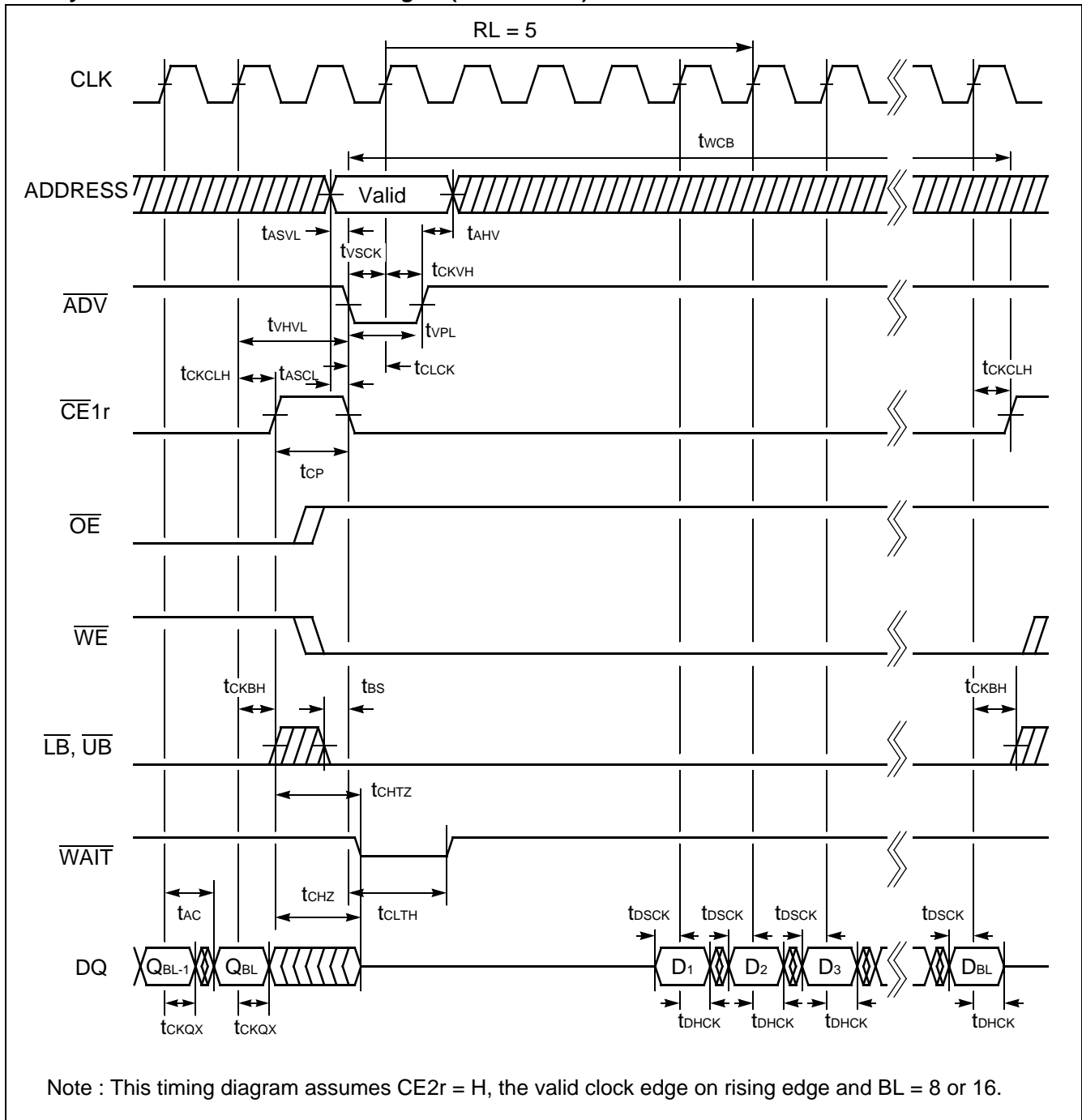
- **Synchronous Read to Write Timing #2($\overline{\text{ADV}}$ Control)**

Note : This timing diagram assumes CE2r = H, the valid clock edge on rising edge and BL = 8 or 16.
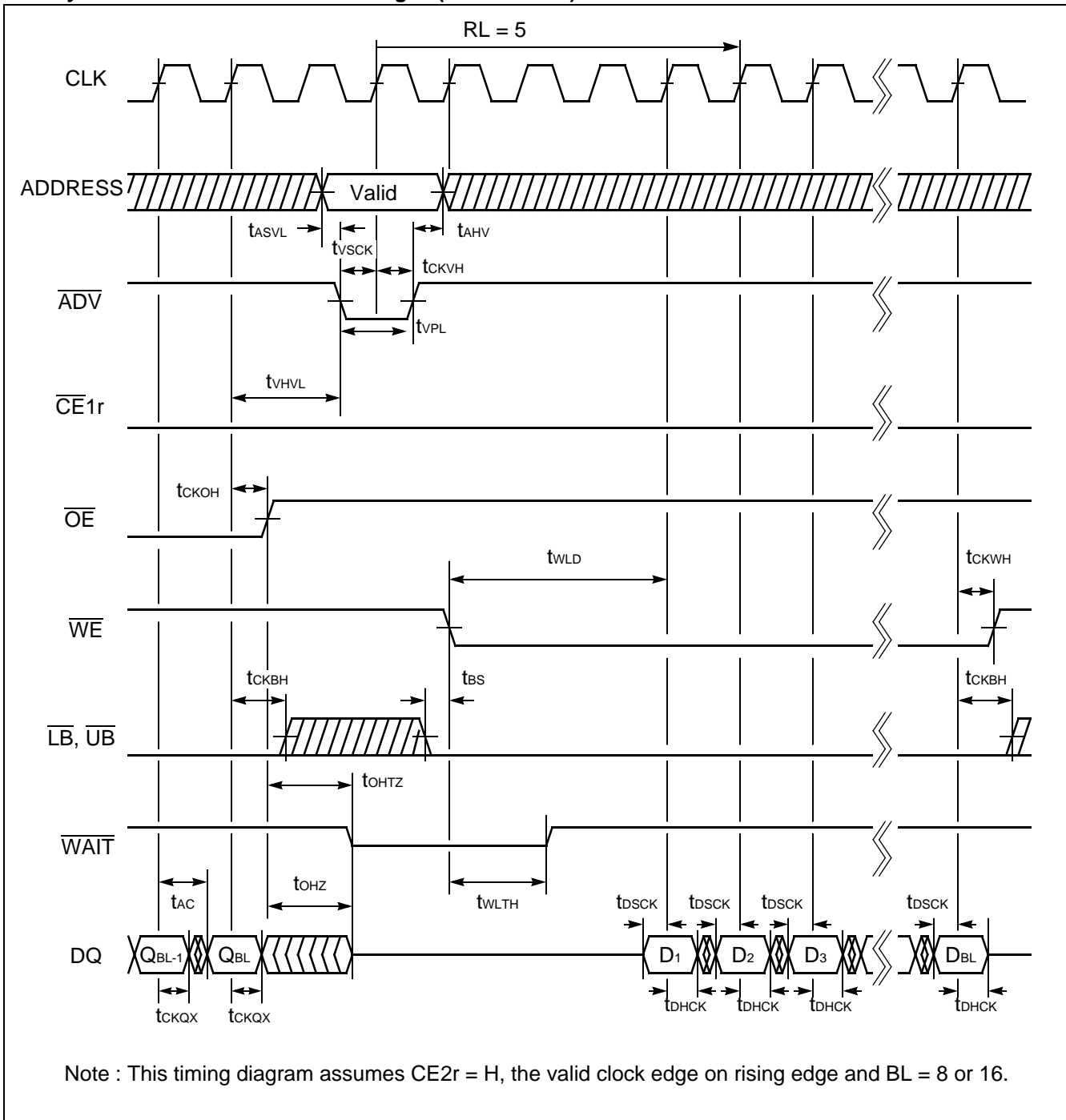
• **Synchronous Write to Read Timing #1 ($\overline{CE}$1r Control)**

Note : This timing diagram assumes CE2r = H, the valid clock edge on rising edge and BL = 8 or 16.
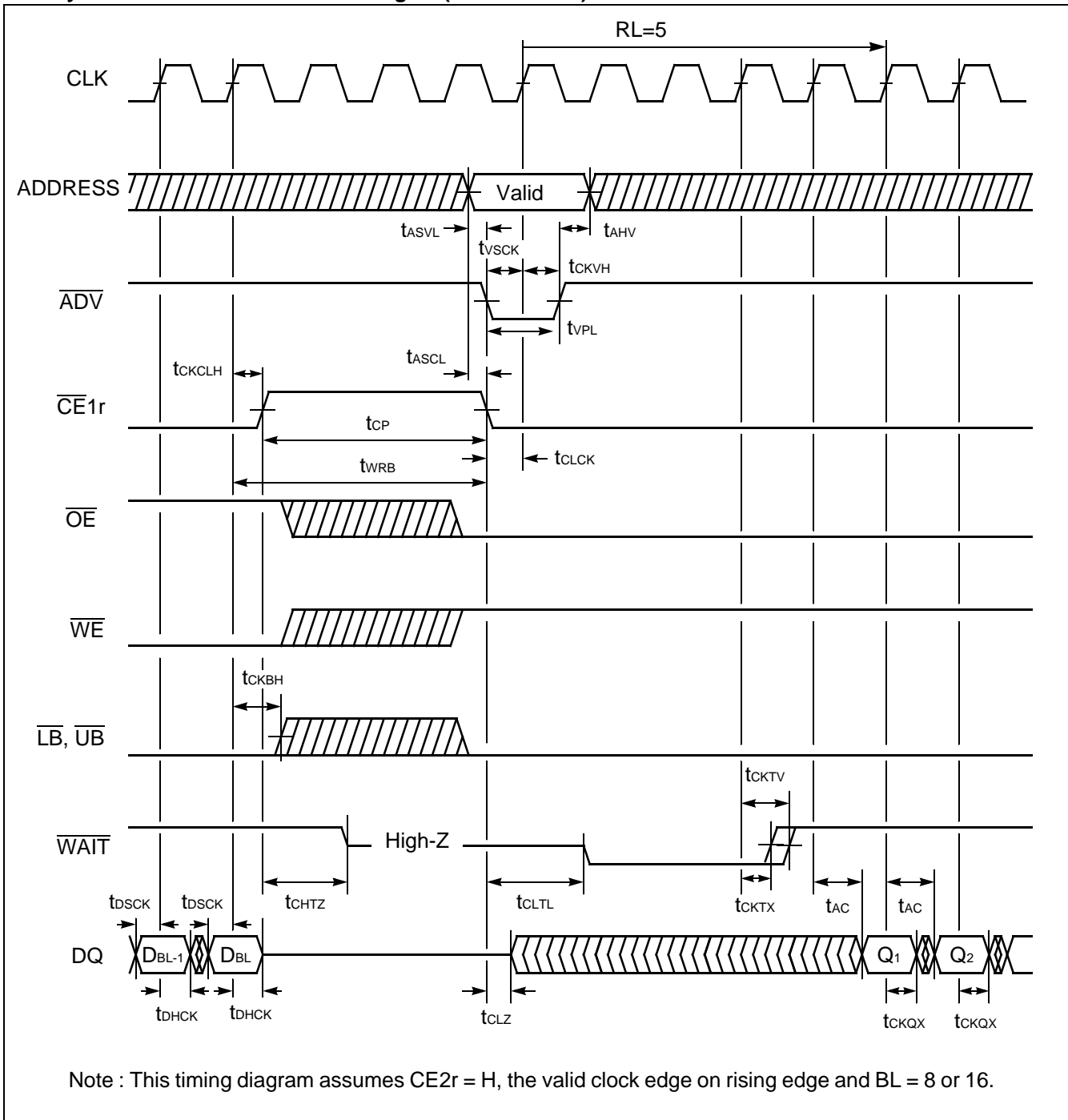
• **Synchronous Write to Read Timing #2 ($\overline{\text{ADV}}$ Control)**

Note : This timing diagram assumes CE2r = H, the valid clock edge on rising edge and BL = 8 or 16.

• **POWER-UP Timing #1**

CE1r   *2

    tCHH*3

CE2r   *2

VccQr   VccQ Min*1
    0 V

Vccr   Vcc Min*1,*2
    0 V
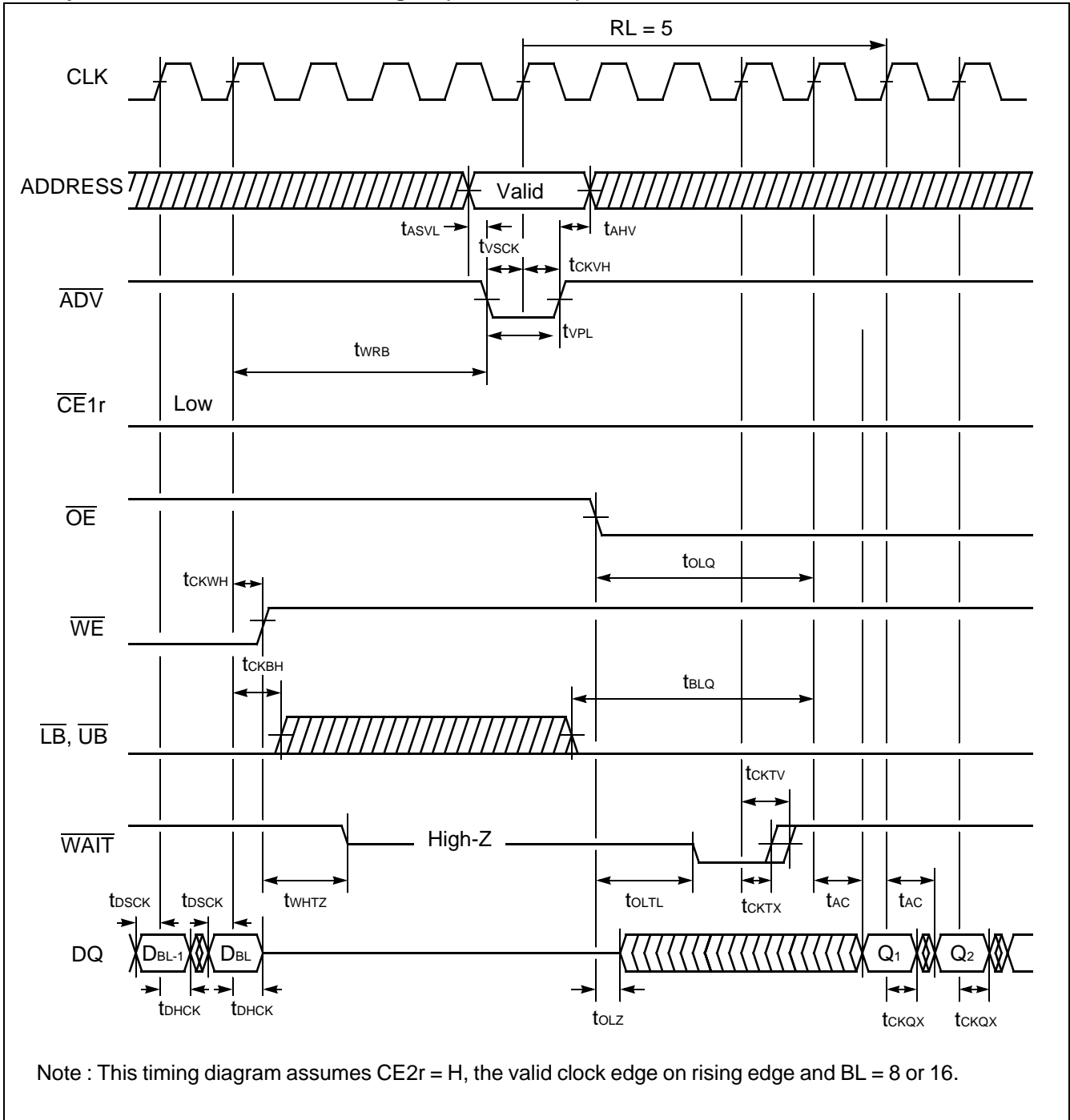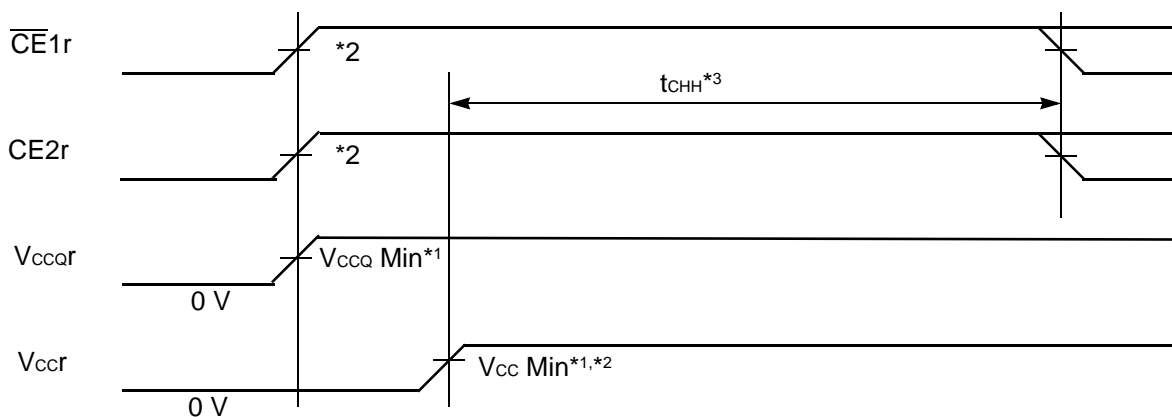
*1 : VccQr shall be applied and reach the specified minimum level prior to Vccr applied.
*2 : The both of CE1r and CE2r shall be brought to High together with VccQr prior to Vccr applied.
    Otherwise POWER-UP Timing#2 must be applied for proper operation.
*3 : The tCHH specifies after Vccr reaches specified minimum level and applicable to both CE1r and CE2r.

• **POWER-UP Timing #2**

CE1r   *3

    tC2HL*2   tCSP   tC2LP   tCHS   tCHH

CE2r

    tC2HL*2

VccQr   VccQr Min*1
    0 V

Vccr   Vccr Min*1
    0 V
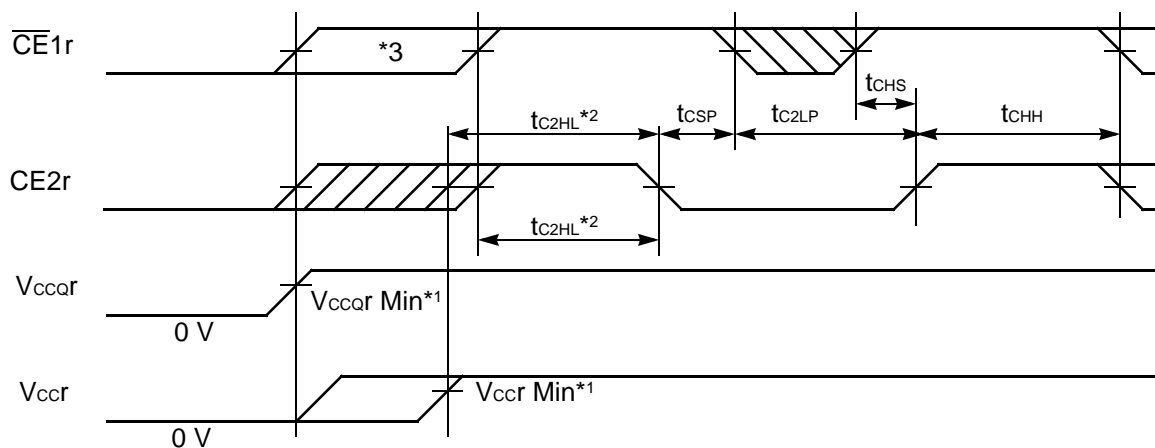
*1 : VccQr shall be applied and reach specified minimum level prior to Vcc applied.
*2 : The tC2HL specifies from CE2r Low to High transition after Vccr reaches specified minimum level.
    If CE2r became High prior to Vccr reached specified minimum level, tC2HL is defined from Vccr minimum.
*3 : CE1r shall be brought to High prior to or together with CE2r Low to High transition.

• POWER DOWN Entry and Exit Timing

$\overline{CE}$1r

CE2r

t_{CHS}

t_{CSP} t_{C2LP} t_{CHH} (t_{CHHP})

DQ   High-Z

Power Down Entry   Power Down Mode   Power Down Exit
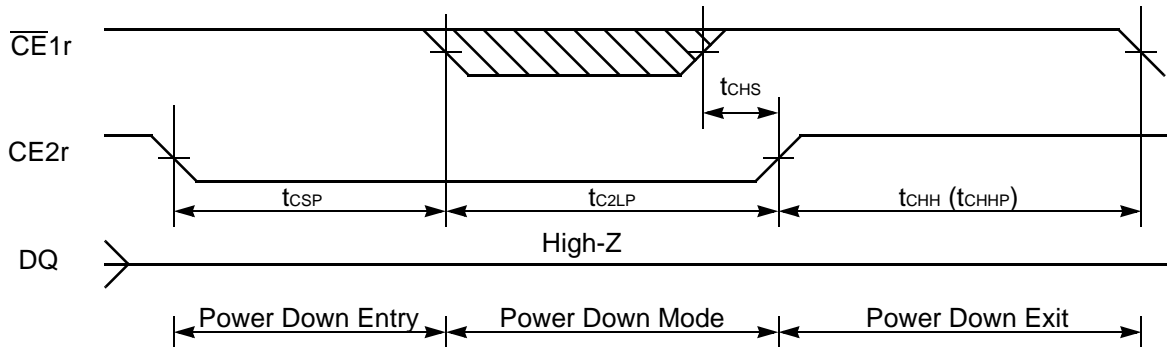
Note : This Power Down mode can be also used as a reset timing if POWER-UP timing above could not be satisfied and Power-Down program was not performed prior to this reset.

• Standby Entry Timing after Read or Write

$\overline{CE}$1r

t_{CHOX} t_{CHWX}

$\overline{OE}$

$\overline{WE}$

Active (Read)   Standby   Active (Write)   Standby
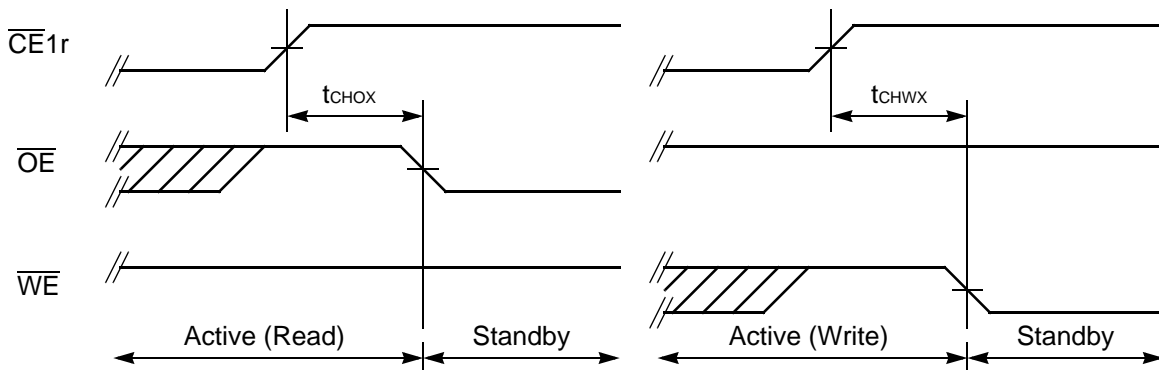
Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode.
If either of timing is not satisfied, it takes t_{RC} (Min) period for Standby mode from $\overline{CE}$1r Low to High transition.

93

• **Configuration Register Set Timing #1 (Asynchronous Operation)**
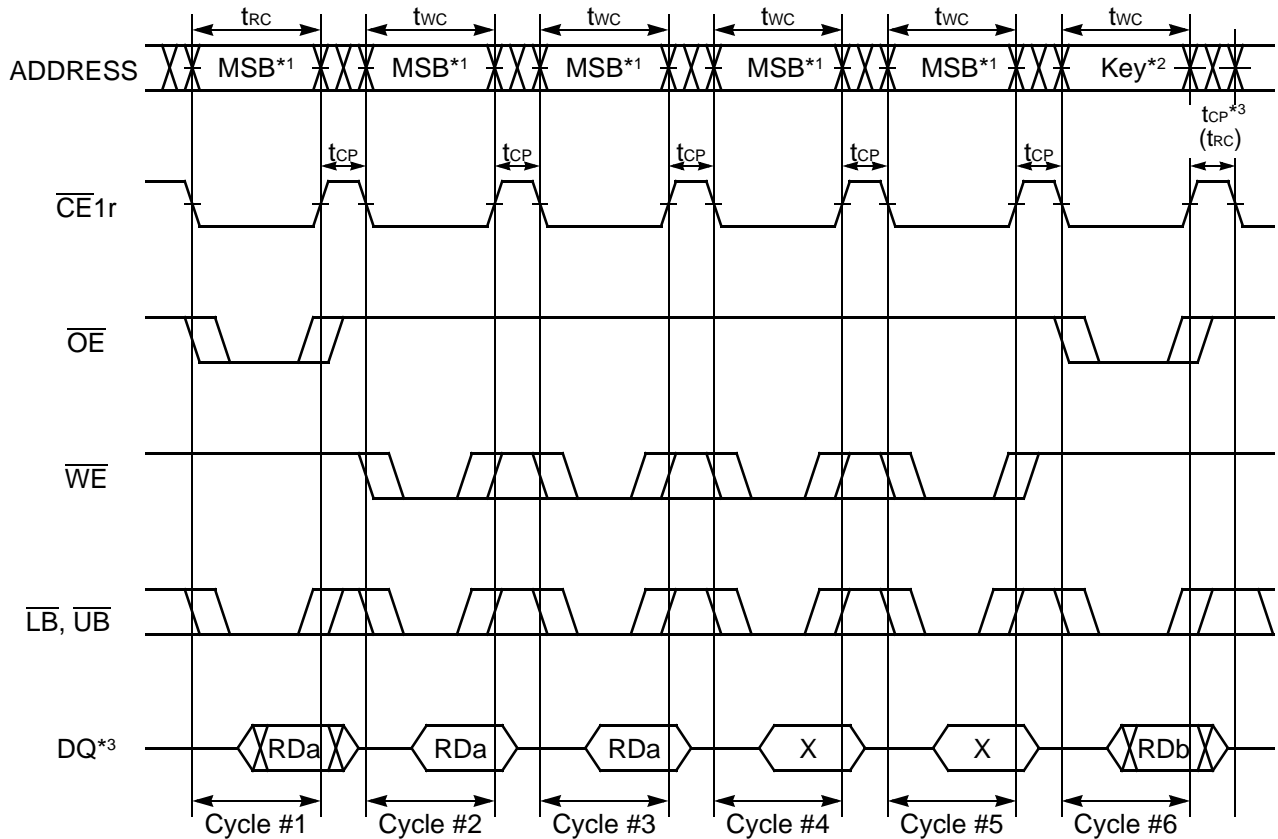
*1 : The all address inputs must be High from Cycle #1 to #5.
*2 : The address key must confirm the format specified in FUNCTIONAL DESCRIPTION. If not, the operation and data are not guaranteed.
*3 : After t_{CP} or t_{RC} following Cycle #6, the Configuration Register Set is completed and returned to the normal operation. t_{CP} and t_{RC} are applicable to returning to asynchronous mode and to synchronous mode respectively.

- $\overline{WE}$ Configuration Register Set Timing #2 (Synchronous Operation)
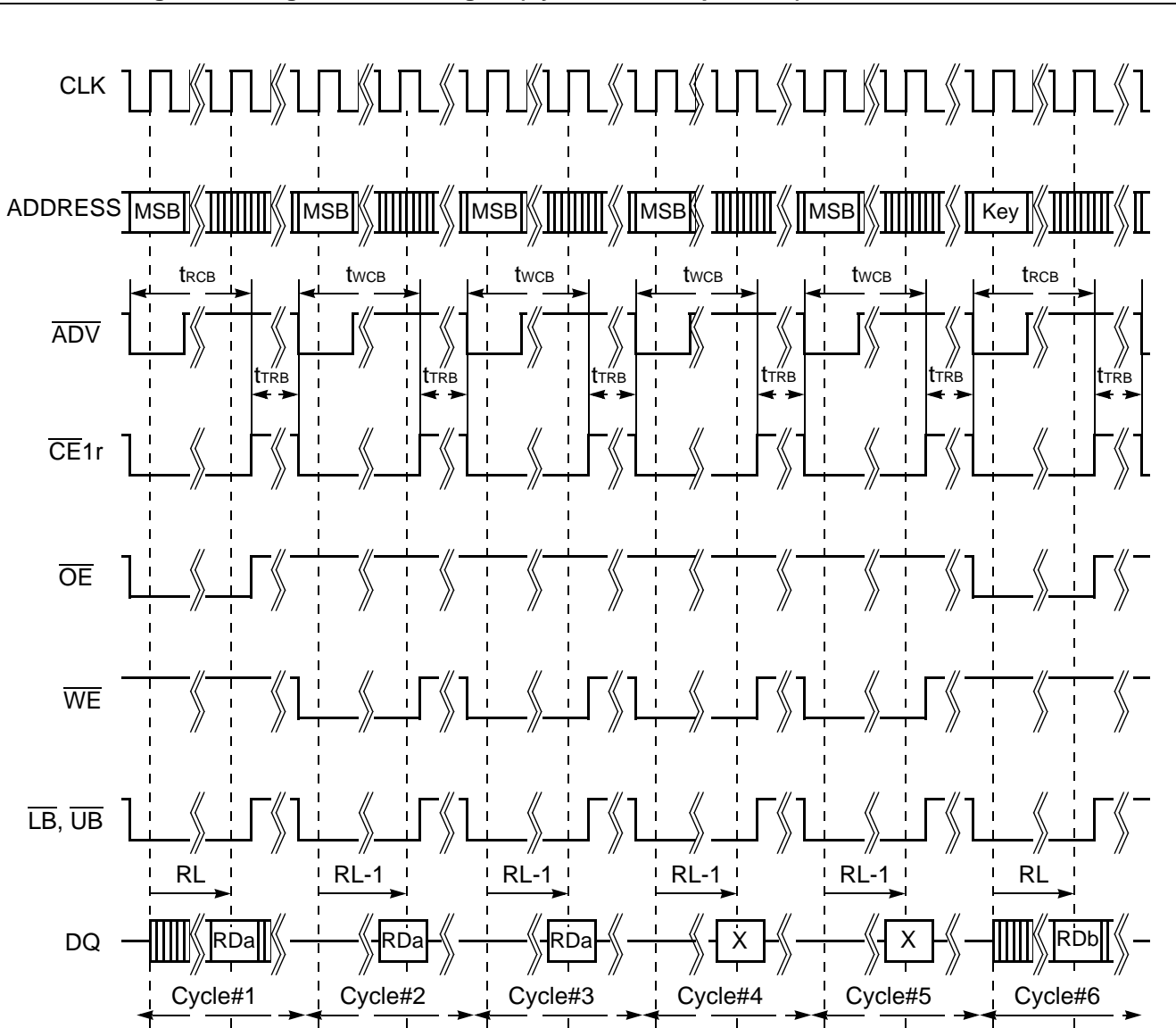
Notes : • The all address inputs must be High from Cycle #1 to #5.
• The address key must confirm the format specified in FUNCTIONAL DESCRIPTION. If not, the operation and data are not guaranteed.
• After t_{TRB} following Cycle #6, the Configuration Register Set is completed and returned to the normal operation.

■ PIN CAPACITANCE

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	$V_{IN} = 0$	—	—	20.0	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$	—	—	25.0	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	—	—	25.0	pF

Note: Test conditions T_A = +25°C, f = 1.0 MHz

■ HANDLING OF PACKAGE

Please handle this package carefully since the sides of package create acute angles.

■ CAUTION

- The high voltage (V_{ID}) cannot apply to address pins and control pins except $\overline{RESET}$. Exception is when autoselect and sector group protect function are used, then the high voltage (V_{ID}) can be applied to $\overline{RESET}$.

- Without the high voltage (V_{ID}) , sector group protection can be achieved by using "Extended Sector Group Protection" command.

■ ORDERING INFORMATION

MB84SF6H6H6L   2   -70   PBS

PACKAGE TYPE
    PBS = 115-ball BGA

SPEED OPTION

Device Revision
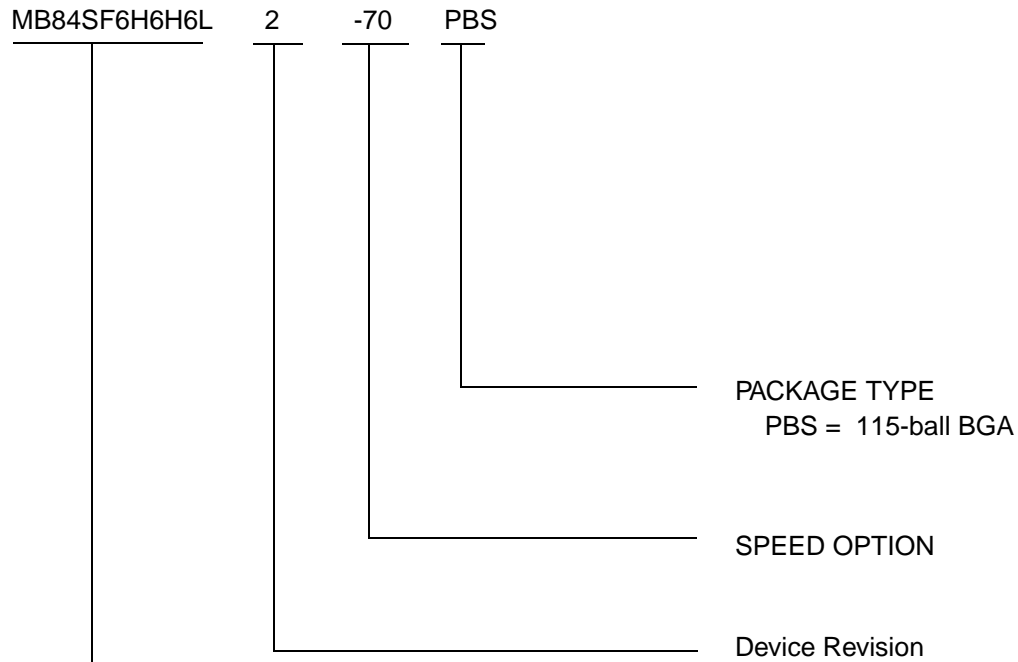
DEVICE NUMBER/DESCRIPTON

128Mega-bit (8M x 16bit) Burst Flash Memory
    1.8V-only Read, Program, and Erase

128Mega-bit (8M x 16bit) Burst Flash Memory
    1.8V-only Read, Program, and Erase

128 Mega-bit (8M x 16bit) FCRAM
    1.8V I/O Supply Voltage
    3.0V Core Supply Voltage

■ PACKAGE DIMENSION

115-ball plastic FBGA
(BGA-115P-M03)
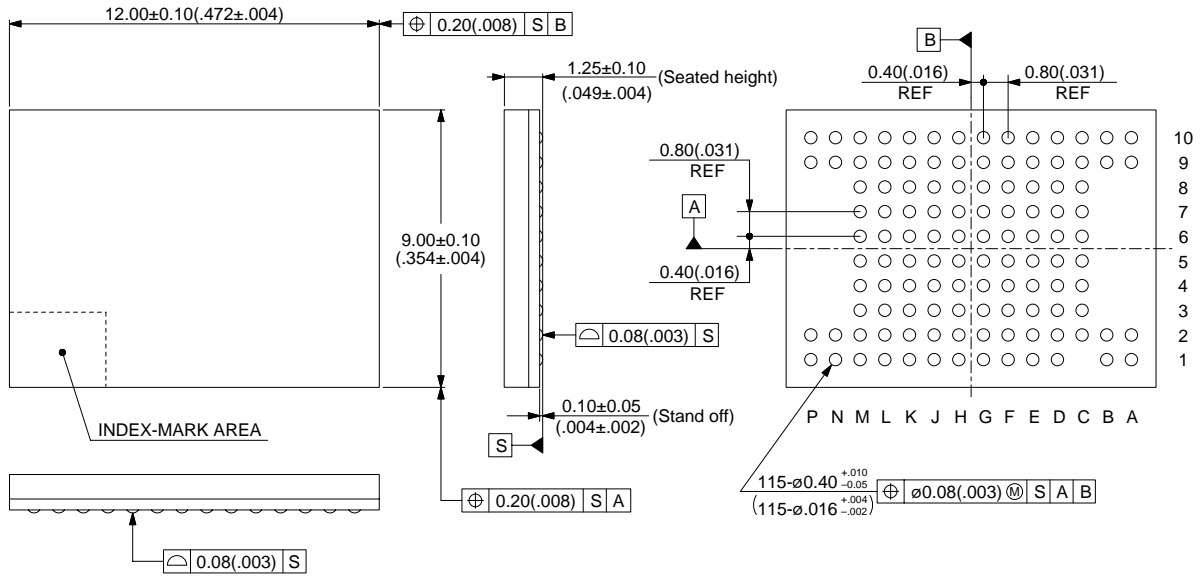
© 2003 FUJITSU LIMITED B115003S-c-1-1

Dimensions in mm (inches)
Note : The values in parentheses are reference values.

FUJITSU LIMITED