Semiconductor

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MCT3A65P100F2, MCT3D65P100F2

65A, 1000V, P-Type MOS-Controlled Thyristor (MCT)

April 1999

Features

- **65A, -1000V**
- **V_{TM} = -1.4V (Max) at I = 65A and 150^{o}C**
- **2000A Surge Current Capability**
- **2000A/μs di/dt Capability**
- **MOS Insulated Gate Control**
- **100A Gate Turn-Off Capability at 150^{o}C**

Part Number Information

PART NUMBER	PACKAGE	BRAND
MCT3A65P100F2	TO-247	M65P100F2
MCT3D65P100F2	MO-093AA	M65P100F2

NOTE: When ordering, use the entire part number.

Description

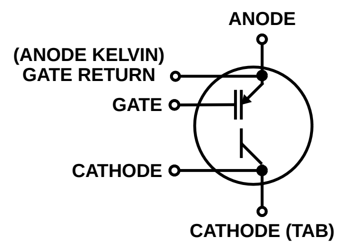
The MCT is an MOS Controlled Thyristor designed for switching currents on and off by negative and positive pulsed control of an insulated MOS gate. It is designed for use in motor controls, inverters, line switches, and other power switching applications.

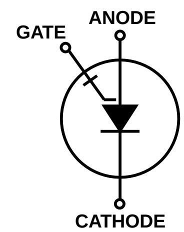
The MCT is especially suited for resonant (zero voltage or zero current switching) applications. The SCR like forward drop greatly reduces conduction power loss.

MCTs allow the control of high power circuits with very small amounts of input energy. They feature the high peak current capability common to SCR type thyristors, and operate at junction temperatures up to 150^{o}C with active switching.

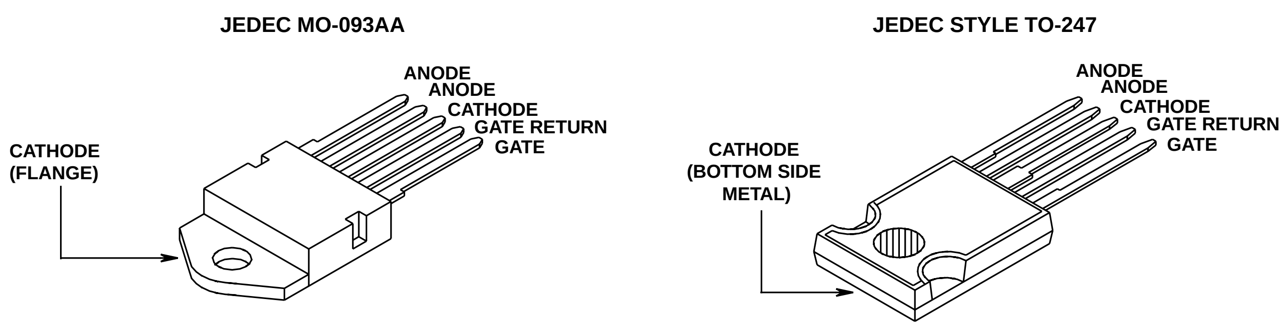
Formerly developmental type TA49226.

Symbols





Packaging



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		MCT3A65P100F2 MCT3D65P100F2	UNITS
Peak Off-State Voltage	V_{DRM}	-1000	V
Peak Reverse Voltage	V_{RRM}	5	V
Continuous Cathode Current			
At $T_C = 25^oC$ (Package Limited)	I_{K25}	85	A
At $T_C = 110^oC$	I_{K110}	65	A
Non-repetitive Peak Cathode Current (Note 1)	I_{KSM}	2000	A
Peak Controllable Current	I_{KC}	100	A
Gate to Anode Voltage (Continuous)	V_{GA}	±15	V
Gate to Anode Voltage (Peak)	V_{GA}	±20	V
Rate of Change of Voltage	dv/dt	Figure 11	
Rate of Change of Current	di/dt	2000	A/µs
Maximum Power Dissipation	P_T	290	W
Power Dissipation Derating $T_C > 25^oC$		2.32	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to 150	^{o}C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^{o}C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum Pulse Width of 200µs (Half Sine). Assume T_J(Initial) = 90^{o}C and T_J(Final) = T_J(Max) = 150^{o}C.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Peak Off-State Blocking Current	I_{DRM}	V_{KA} = -1000V, V_{GA} = 15V	$T_C = 150^oC$	-	-	3	mA
			$T_C = 25^oC$	-	-	100	µA
Peak Reverse Blocking Current	I_{RRM}	V_K = 5V, V_{GA} = 15V	$T_C = 150^oC$	-	-	4	mA
			$T_C = 25^oC$	-	-	100	µA
On-State Voltage	V_{TM}	$I_K = I_{K110}$, V_{GA} = -10V	$T_C = 150^oC$	-	1.25	1.4	V
			$T_C = 25^oC$	-	1.35	1.5	V
Gate to Anode Leakage Current	I_{GAS}	V_{GA} = ±20V		-	-	200	nA
Input Capacitance	C_{ISS}	V_{GA} = 15V, V_{KA} = -20V, f = 1MHz		-	12	-	nF
Current Turn-On Delay Time	$t_{d(ON)I}$	$T_C = 150^oC$, L = 200µH, $I_K = I_{K110}$ = 65A, V_{KA} = -400V, V_{GA} = 15V/-10V, R_G = 2.2Ω, Test Circuit (Figure 13)		-	125	-	ns
Current Rise Time	t_{rI}			-	70	-	ns
Current Turn-Off Delay Time	$t_{d(OFF)I}$			-	770	-	ns
Current Fall Time	t_{fI}			-	1000	1400	ns
Turn-On Energy	E_{ON}			-	2.8	-	mJ
Turn-Off Energy (Note 2)	E_{OFF}			-	15	-	mJ
Thermal Resistance Junction To Case	$R_{\theta JC}$			-	-	0.43	^{o}C/W

NOTE:

2. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the cathode current equals zero (I_K = 0A). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include losses due to diode recovery.

Typical Performance Curves (Unless Otherwise Specified)

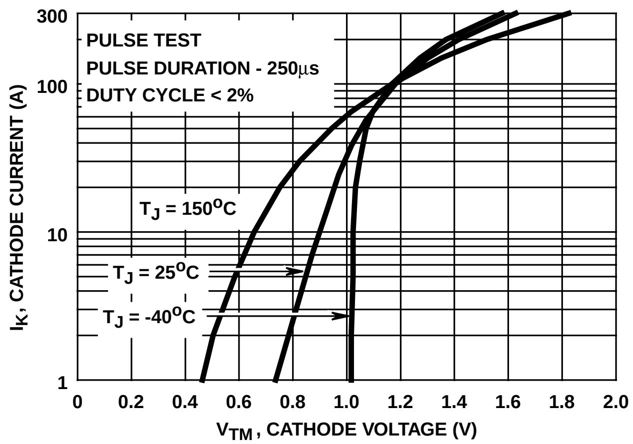


FIGURE 1. CATHODE CURRENT vs SATURATION VOLTAGE

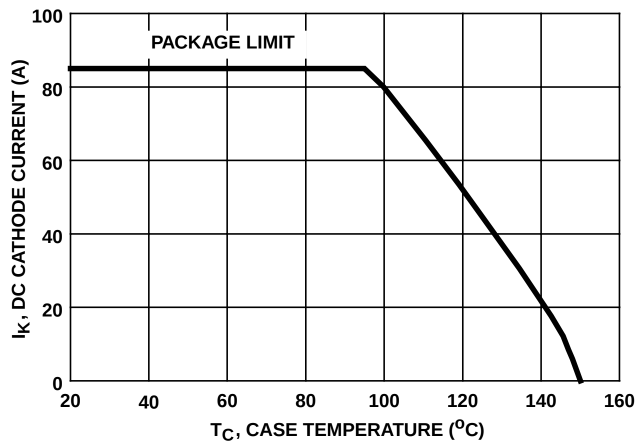


FIGURE 2. DC CATHODE CURRENT vs CASE TEMPERATURE

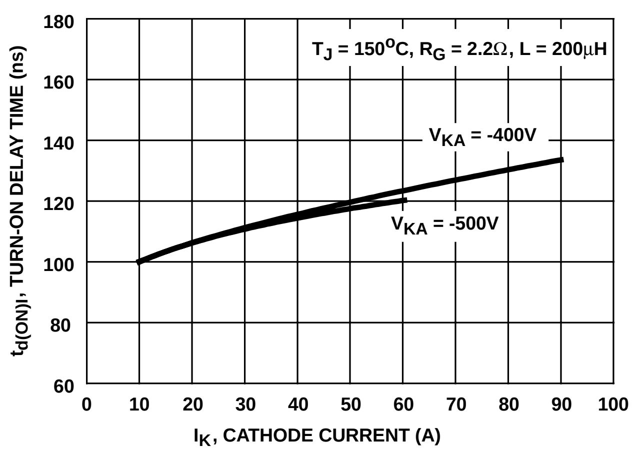


FIGURE 3. TURN-ON DELAY TIME vs CATHODE CURRENT

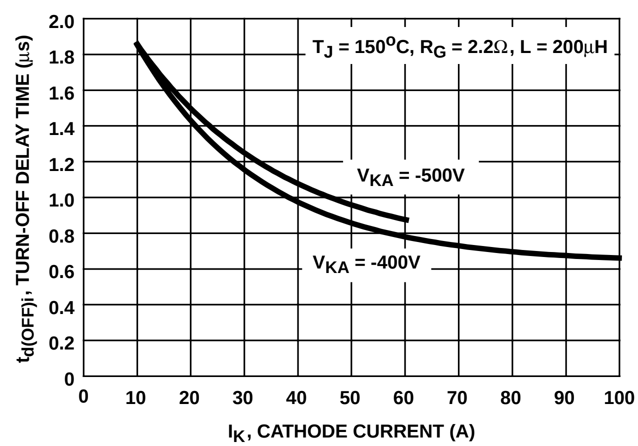


FIGURE 4. TURN-OFF DELAY TIME vs CATHODE CURRENT

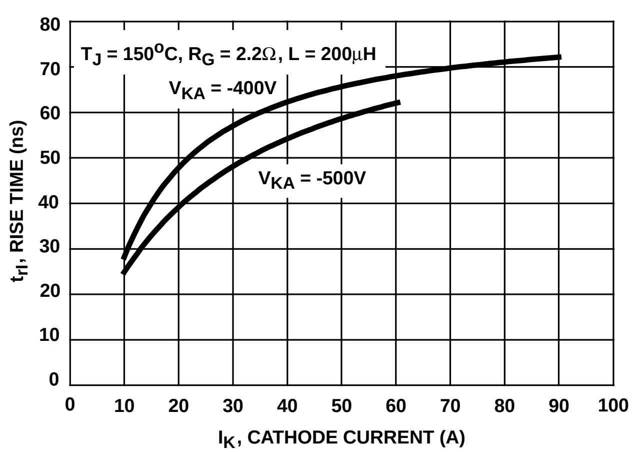


FIGURE 5. TURN-ON RISE TIME vs CATHODE CURRENT

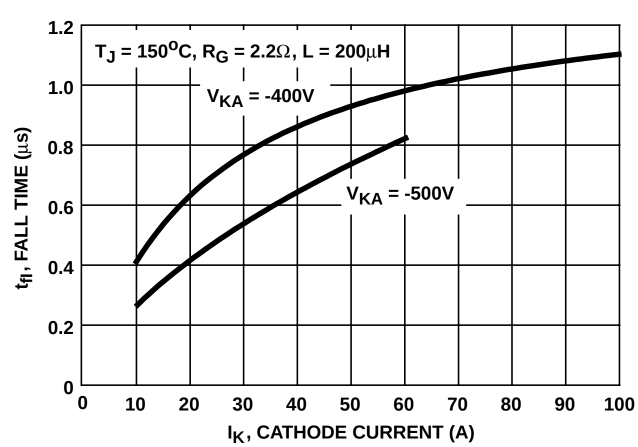


FIGURE 6. TURN-OFF FALL TIME vs CATHODE CURRENT

Typical Performance Curves (Unless Otherwise Specified) **(Continued)**

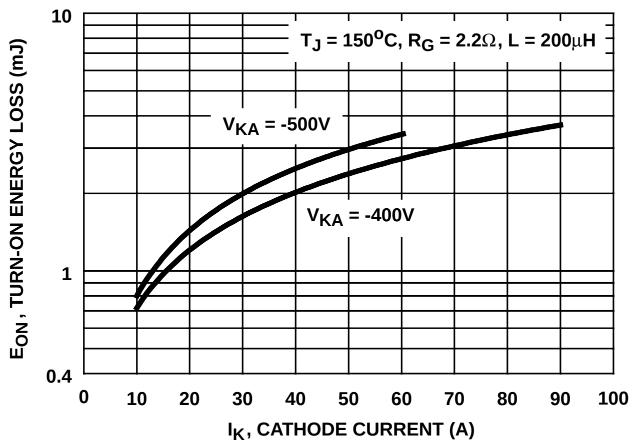


FIGURE 7. TURN-ON ENERGY LOSS vs CATHODE CURRENT

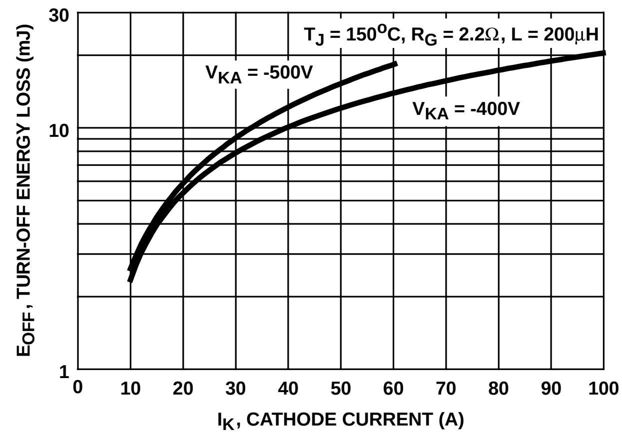


FIGURE 8. TURN-OFF ENERGY LOSS vs CATHODE CURRENT

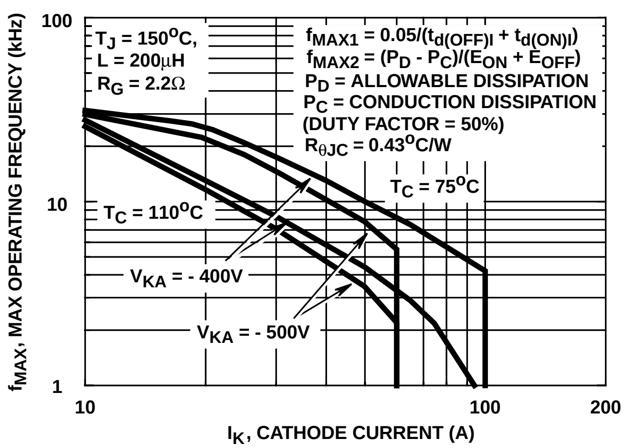


FIGURE 9. OPERATING FREQUENCY vs CATHODE CURRENT

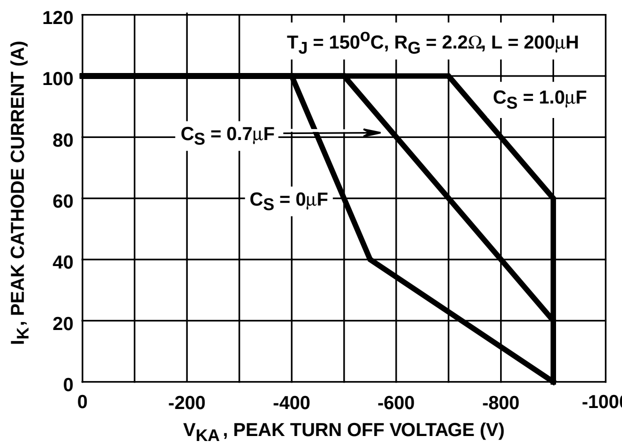


FIGURE 10. TURN-OFF CAPABILITY vs ANODE TO CATHODE VOLTAGE

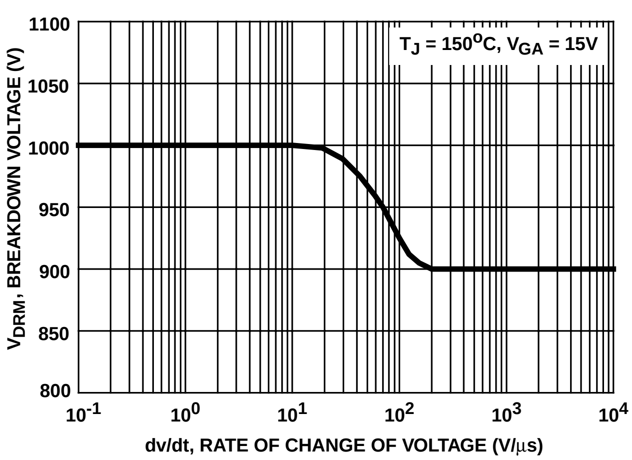


FIGURE 11. BLOCKING VOLTAGE vs RATE OF CHANGE OF VOLTAGE

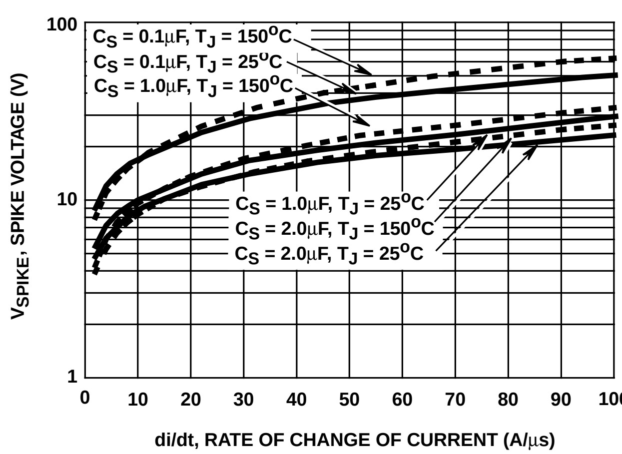


FIGURE 12. SPIKE VOLTAGE vs RATE OF CHANGE OF CURRENT

Test Circuits and Waveforms

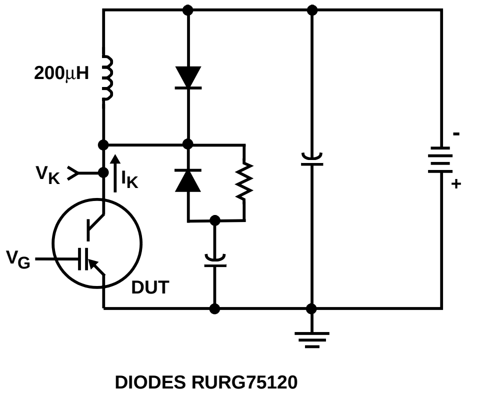


FIGURE 13. INDUCTIVE SWITCHING TEST CIRCUIT

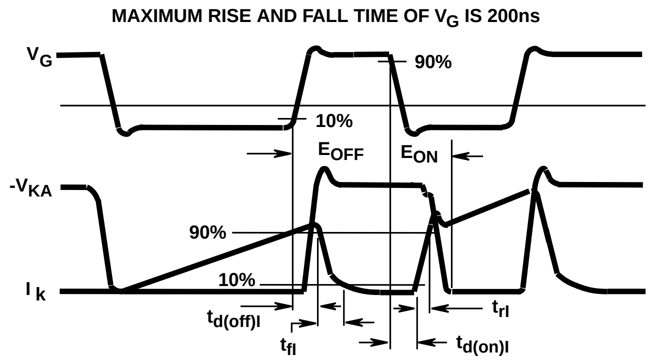


FIGURE 14. SWITCHING TEST WAVEFORMS

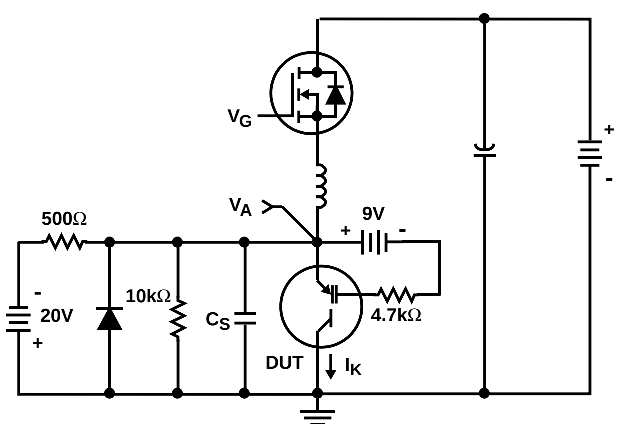


FIGURE 15. V_{SPIKE} TEST CIRCUIT

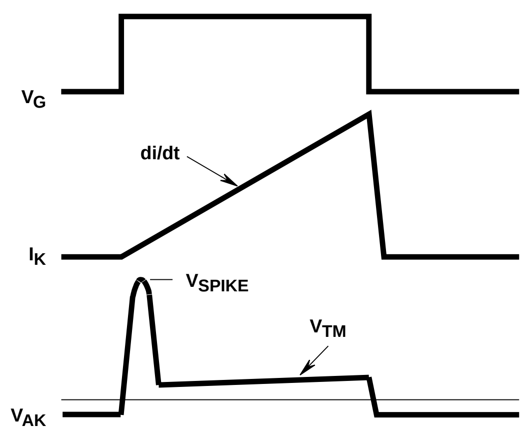


FIGURE 16. V_{SPIKE} TEST WAVEFORMS

Handling Precautions for MCTs

MOS Controlled Thyristors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. MCTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GAM}. Exceeding the rated V_{GA} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to anode. If gate protection is required an external zener is recommended.

Operating Frequency Information

Operating frequency information for a typical device (Figure 9) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs cathode current (I_{AK}) plots are possible using the information shown for a typical unit in Figures 3 to 8. The operating frequency plot (Figure 9) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

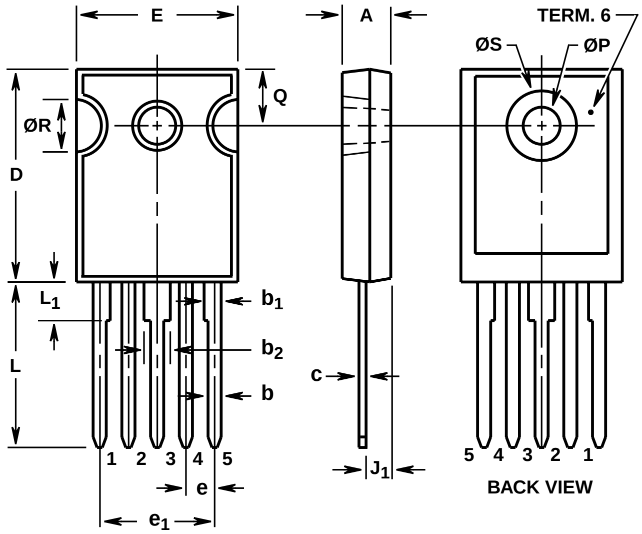
f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I} + t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 14. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{d(OFF)}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 9) and the conduction losses (P_C) are approximated by $P_C = (V_{AK} \times I_{AK})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 14. E_{ON} is the integral of the instantaneous power loss ($I_{AK} \times V_{AK}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{AK} \times V_{AK}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the cathode current equals zero ($I_K = 0$).

TO-247

5 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



LEAD 1	-	**GATE**
LEAD 2	-	**GATE RETURN**
LEAD 3	-	**CATHODE**
LEAD 4	-	**ANODE**
LEAD 5		**ANODE**
TERM. 6		**CATHODE**

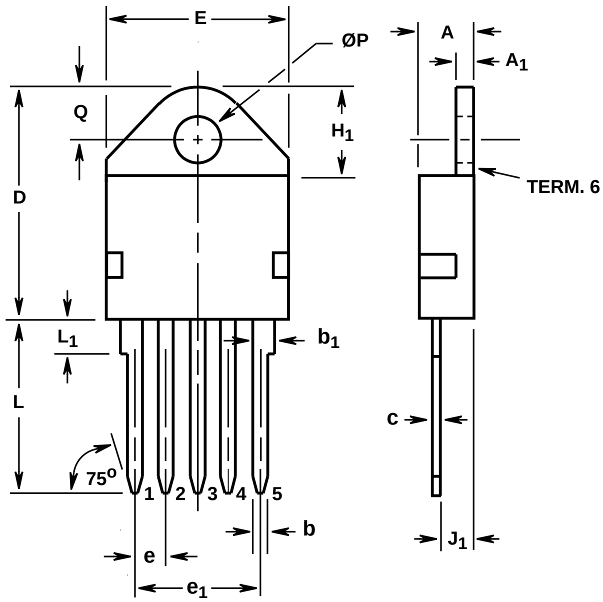
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.110 TYP		2.79 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

MO-093AA

5 LEAD JEDEC MO-093AA PLASTIC PACKAGE



LEAD 1 - GATE
LEAD 2 - GATE RETURN
LEAD 3 - CATHODE
LEAD 4 - ANODE
LEAD 5 ANODE
TERM. 6 CATHODE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.185	0.195	4.70	4.95	-
A_1	0.058	0.062	1.48	1.57	-
b	0.049	0.053	1.25	1.34	3, 4, 5
b_1	0.070	0.080	1.78	2.03	3, 4
c	0.018	0.022	0.46	0.55	3, 4, 5
D	0.800	0.820	20.32	20.82	-
E	0.615	0.625	15.63	15.87	2
e	0.110 TYP		2.80 TYP		7
e_1	0.438 BSC		11.12 BSC		7
H_1	-	0.330	-	8.38	-
J_1	0.115	0.125	2.93	3.17	8
L	0.575	0.600	14.61	15.24	-
L_1	-	0.130	-	3.30	3
ØP	0.159	0.163	4.04	4.14	-
Q	0.176	0.186	4.48	4.72	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC MO-093AA outline dated 2-90.
2. Tab outline optional within boundaries of dimensions E and Q.
3. Lead dimension and finish uncontrolled in L_1.
4. Lead dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder coating.
6. Maximum radius of 0.050 inches (1.27mm) on all body edges and corners.
7. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
8. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
9. Controlling dimension: Inch.
10. Revision 1 dated 1-93.