

# Preliminary Spec.

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MITSUBISHI LSIs

## MH4V36AM-6,-7

FAST PAGE MODE 150994944-BIT ( 4194304-WORD BY 36-BIT ) DYNAMIC RAM

### DESCRIPTION

The MH4V36AM is an 4M word by 36-bit dynamic RAM module and consists of 2 industry standard 4M X 16 dynamic RAMs in TSOP and 1 industry standard 4M X 4(4CAS) dynamic RAMs in TSOP.

The ICs are mounted on both sides of one small ceracom PC board with flash gold plating and form a convenient 68-pin package.

### FEATURES

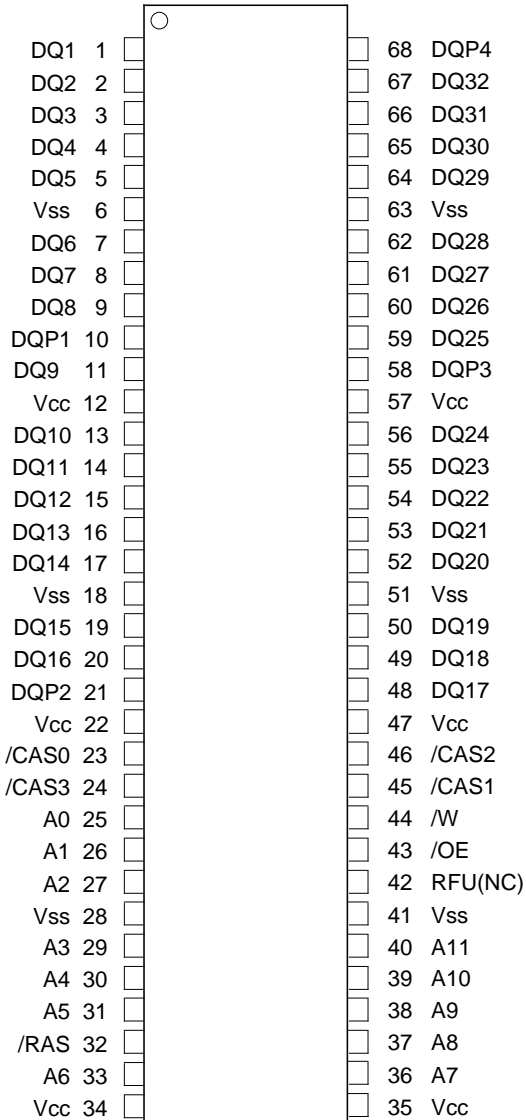
Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)
MH4V36AM-6	60	15	30	15	110
MH4V36AM-7	70	20	35	20	130

- Utilizes industry standard 4M X 16 DRAMs in TSOP package and industry standard 4M X 4(4CAS) DRAM in TSOP package
- Single 3.3V +/- 0.3V supply
- Low stand-by power dissipation  
5.4mW (Max) ..... CMOS Input level
- Low operating power dissipation  
MH4V36AM - 6 ..... 1.155W (Max)  
MH4V36AM - 7 ..... 1.100W (Max)
- All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A<sub>0</sub> ~ A<sub>11</sub>)
- Includes 2pcs 0.22uF decoupling capacitors

### APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

### PIN CONFIGURATION ( TOP VIEW )



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### FUNCTION

The MH4V36AM provide, in addition to normal read, write, and read-modify-write operations, a number of

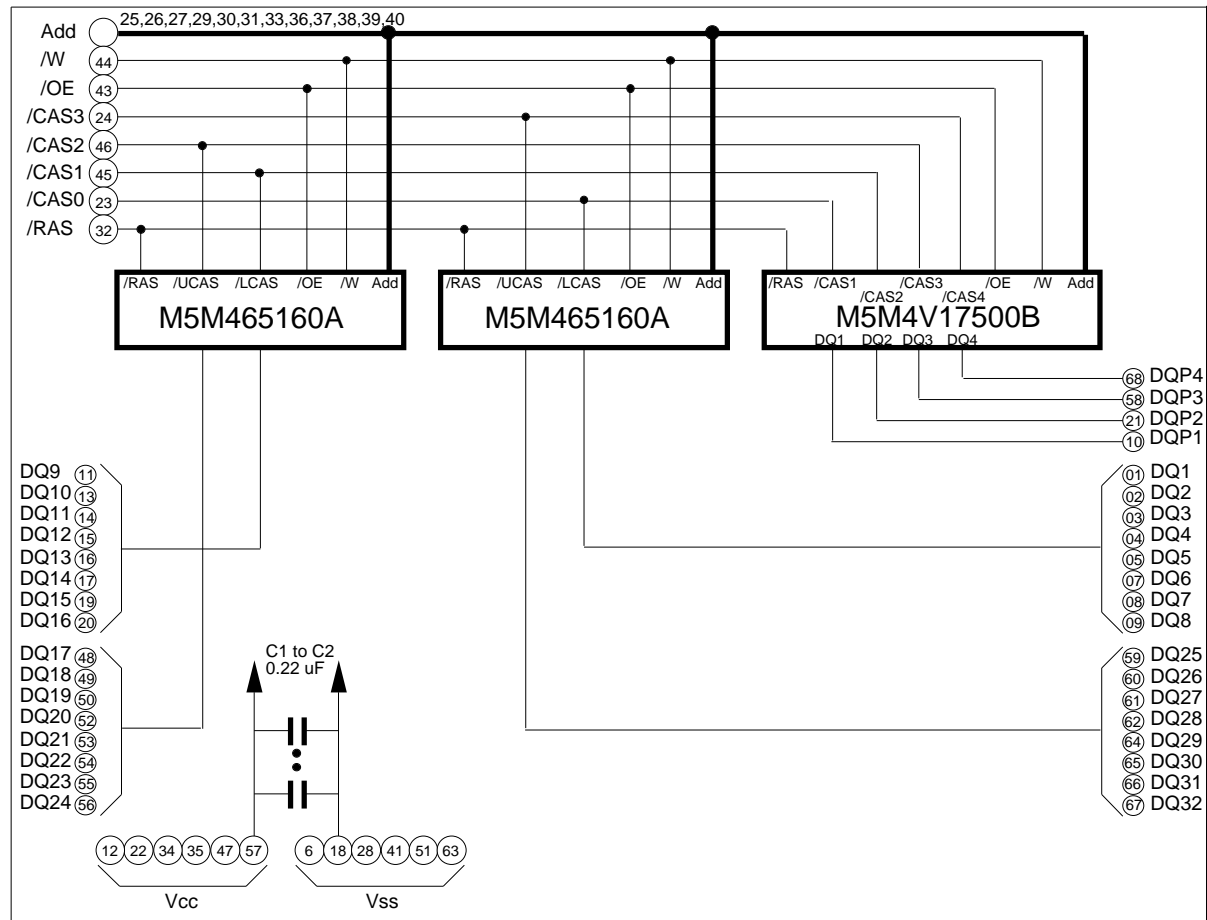
other functions, e.g., fast page mode,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs				Input/Output	
	RAS	CAS	W	OE	Input	Output
Read	ACT	ACT	NAC	ACT	OPN	VLD
Write	ACT	ACT	ACT	NAC	VLD	OPN
Read-modify-write	ACT	ACT	ACT	ACT	VLD	VLD
RAS-only refresh	ACT	NAC	DNC	DNC	DNC	OPN
Hidden refresh	ACT	ACT	DNC	ACT	OPN	VLD
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	NAC	DNC	DNC	OPN
Standby	NAC	DNC	DNC	DNC	DNC	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

### BLOCK DIAGRAM



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### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>cc</sub>	Supply voltage	With respect to V <sub>ss</sub>	-0.5 ~ 4.6	V
V <sub>I</sub>	Input voltage		-0.5 ~ 4.6	V
V <sub>O</sub>	Output voltage		-0.5 ~ 4.6	V
I <sub>O</sub>	Output current		50	mA
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25°C	3	W
T <sub>opr</sub>	Operating temperature		0 ~ 70	°C
T <sub>stg</sub>	Storage temperature		-40 ~ 100	°C

### RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub>=0 ~70 °C , unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V <sub>cc</sub>	Supply voltage	3.0	3.3	3.6	V
V <sub>ss</sub>	Supply voltage	0	0	0	V
V <sub>IH</sub>	High-level input voltage, all inputs	3.0		3.6	V
V <sub>IL</sub>	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to V<sub>ss</sub>

### ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=0 ~70 °C, V<sub>cc</sub>=3.3V±0.3V, V<sub>ss</sub>=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
VOH	High-level output voltage	I <sub>OH</sub> =-2.0mA	2.4		V <sub>cc</sub>	v	
VOL	Low-level output voltage	I <sub>OL</sub> =2.0mA	0		0.4	v	
IOZ	Off-state output current	Q floating 0V V <sub>OUT</sub> 3.6V	-10		10	μA	
I <sub>I</sub>	Input current	0V V <sub>IN</sub> 3.6V, Other inputs pins = 0V	-30		30	μA	
I <sub>CC1</sub> (AV)	Average supply current from V <sub>cc</sub> operating (Note 3,4,5)	-6 -7	R <sub>AS</sub> , C <sub>AS</sub> cycling t <sub>RC</sub> =t <sub>WC</sub> =min. output open			380	mA
						305	
I <sub>CC2</sub>	Supply current from V <sub>cc</sub> , stand-by		R <sub>AS</sub> = C <sub>AS</sub> =V <sub>IH</sub> , output open			4	mA
			R <sub>AS</sub> = C <sub>AS</sub> V <sub>cc</sub> -0.2V, output open			1.4	
I <sub>CC4</sub> (AV)	Average supply current from V <sub>cc</sub> Fast-Page-Mode (Note 3,4,5)	-6 -7	R <sub>AS</sub> =V <sub>IL</sub> , C <sub>AS</sub> cycling t <sub>PC</sub> =min. output open			260	mA
						240	
I <sub>CC6</sub> (AV)	Average supply current from V <sub>cc</sub> C <sub>AS</sub> before R <sub>AS</sub> refresh mode (Note 3,5)	-6 -7	C <sub>AS</sub> before R <sub>AS</sub> refresh cycling t <sub>RC</sub> =min. , W V <sub>cc</sub> - 0.2 output open			380	mA
						365	

Note 2: Current flowing into an IC is positive, out is negative.

3: I<sub>cc1</sub> (AV), I<sub>cc4</sub> (AV) and I<sub>cc6</sub> (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I<sub>cc1</sub> (AV) and I<sub>cc4</sub> (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while R<sub>AS</sub>=V<sub>IL</sub> and C<sub>AS</sub>=V<sub>IH</sub>

### CAPACITANCE (T<sub>a</sub>=0~70°C , V<sub>cc</sub>=3.3V±0.3V, V<sub>ss</sub>=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>I</sub> (A)	Input capacitance, address inputs	V <sub>I</sub> =V <sub>ss</sub> f=1MHZ V <sub>i</sub> =25mVrms			30	pF
C <sub>I</sub> (OE)	Input capacitance, OE input				36	pF
C <sub>I</sub> (W)	Input capacitance, write control input				36	pF
C <sub>I</sub> (RAS)	Input capacitance, RAS input				36	pF
C <sub>I</sub> (CAS)	Input capacitance, CAS input				30	pF
C <sub>I</sub> / O	Input/Output capacitance, data ports				25	pF

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### SWITCHING CHARACTERISTICS (Ta=0~70°C , Vcc=3.3V +/-0.3V, Vss=0V, unless otherwise noted , see notes 6,13,14)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ (Note 7,8)		15		20	ns
tRAC	Access time from $\overline{\text{RAS}}$ (Note 7,9)		60		70	ns
tAA	Column address access time (Note 7,10)		30		35	ns
tCPA	Access time from $\overline{\text{CAS}}$ precharge (Note 7,11)		35		40	ns
tOEA	Access time from $\overline{\text{OE}}$ (Note 7)		15		20	ns
tCLZ	Output low impedance time from $\overline{\text{CAS}}$ low (Note 7)	5		5		ns
tOFF	Output disable time after $\overline{\text{CAS}}$ high (Note 12)	0	15	0	15	ns
tOEZ	Output disable time after $\overline{\text{OE}}$ high (Note 12)	0	15	0	15	ns

Note 6: An initial pause of 500  $\mu\text{s}$  is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-Only refresh or CAS before RAS refresh).

Note the RAS may be cycled during the initial pause . And any 8  $\overline{\text{RAS}}$  or  $\overline{\text{RAS/CAS}}$  cycles are required after prolonged periods (greater than 64 ms) of RAS inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to  $\text{VOH}=2.4\text{V}(\text{IOH}=-2\text{mA})/\text{VOL}=0.4\text{V}(\text{IOL}=2\text{mA})$  load 100pF.

The reference levels for measuring of output signal are 2.0V(VOH) and 0.8V(VOL).

8: Assumes that tRCD tRCD(max) and tASC tASC(max).

9: Assumes that tRCD tRCD(max) and tRAD tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

10: Assumes that tRAD tRAD(max) and tASC tASC(max).

11: Assumes that tCP tCP(max) and tASC tASC(max).

12: tOFF(max) and tOEZ (max) defines the time at which the output achieves the high impedance state (Iout I +/- 10  $\mu\text{A}$ ) and is not reference to VOH(min) or VOL(max).

### TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70 °C, Vcc=3.3V +/- 0.3V, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
tREF	Refresh cycle time		64		64	ms
tRP	RAS high pulse width	40		50		ns
tRCD	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (Note15)	20	45	20	50	ns
tCRP	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	10		10		ns
tRPC	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low	0		0		ns
tCPN	$\overline{\text{CAS}}$ high pulse width	10		10		ns
tRAD	Column address delay time from $\overline{\text{RAS}}$ low (Note16)	15	30	15	35	ns
tASR	Row address setup time before $\overline{\text{RAS}}$ low	0		0		ns
tASC	Column address setup time before $\overline{\text{CAS}}$ low (Note17)	0	10	0	10	ns
tRAH	Row address hold time after $\overline{\text{RAS}}$ low	10		10		ns
tCAH	Column address hold time after $\overline{\text{CAS}}$ low	15		15		ns
tdZC	Delay time, data to $\overline{\text{CAS}}$ low (Note18)	0		0		ns
tdZO	Delay time, data to $\overline{\text{OE}}$ low (Note18)	0		0		ns
tcDD	Delay time, $\overline{\text{CAS}}$ high to data (Note19)	15		15		ns
tODD	Delay time, $\overline{\text{OE}}$ high to data (Note19)	15		15		ns
tr	Transition time (Note20)	1	50	1	50	ns

Note 13: The timing requirements are assumed tr=5ns.

14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) = tRAH(min) + 2tH + tASC(min).

16: tRAD(max) is specified as a reference point only. If tRAD tRAD(max) and tASC tASC(max), access time is controlled exclusively by tAA.

17: tASC(max) is specified as a reference point only. If tRCD tRCD(max) and tASC tASC(max), access time is controlled exclusively by tCAC.

18: Either tdZC or tdZO must be satisfied.

19: Either tcDD or tODD must be satisfied.

20: tr is measured between VIH(min) and VIL(max).

### Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
t <sub>RC</sub>	Read cycle time	110		130		ns
t <sub>RAS</sub>	RAS low pulse width	60	10000	70	10000	ns
t <sub>CAS</sub>	CAS low pulse width	15	10000	20	10000	ns
t <sub>CSH</sub>	CAS hold time after RAS low	60		70		ns
t <sub>RS<math>\bar{H}</math></sub>	RAS hold time after RAS low	15		20		ns
t <sub>RCS</sub>	Read Setup time after CAS high	0		0		ns
t <sub>rch</sub>	Read hold time after CAS low (Note 21)	0		0		ns
t <sub>rrh</sub>	Read hold time after RAS low (Note 21)	10		10		ns
t <sub>RAL</sub>	Column address to RAS hold time	30		35		ns
t <sub>och</sub>	CAS hold time after OE low	15		20		ns
t <sub>orh</sub>	RAS hold time after OE low	15		20		ns

Note 21: Either t<sub>rch</sub> or t<sub>rrh</sub> must be satisfied for a read cycle.

### Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
t <sub>WC</sub>	Write cycle time	110		130		ns
t <sub>RAS</sub>	RAS low pulse width	60	10000	70	10000	ns
t <sub>CAS</sub>	CAS low pulse width	15	10000	20	10000	ns
t <sub>CSH</sub>	CAS hold time after RAS low	60		70		ns
t <sub>RS<math>\bar{H}</math></sub>	RAS hold time after RAS low	15		20		ns
t <sub>WCS</sub>	Write setup time before CAS low (Note 23)	0		0		ns
t <sub>WCH</sub>	Write hold time after CAS low	10		10		ns
t <sub>CWL</sub>	CAS hold time after W low	15		20		ns
t <sub>RWL</sub>	RAS hold time after W low	15		20		ns
t <sub>WP</sub>	Write pulse width	10		10		ns
t <sub>DS</sub>	Data setup time before CAS low or W low	0		0		ns
t <sub>DH</sub>	Data hold time after CAS low or W low	10		15		ns
t <sub>OE<math>\bar{H}</math></sub>	OE hold time after W low	15		20		ns

### Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
trWC	Read write/read modify write cycle time (Note22)	155		180		ns
tRAS	RAS low pulse width	105	10000	120	10000	ns
tCAS	CAS low pulse width	60	10000	70	10000	ns
tCSH	CAS hold time after RAS low	105		120		ns
tRSH	RAS hold time after CAS low	60		70		ns
tRCS	Read setup time before CAS low	0		0		ns
tcWD	Delay time, CAS low to W low (Note23)	40		45		ns
trWD	Delay time, RAS low to W low (Note23)	85		95		ns
tAWD	Delay time, address to W low (Note23)	55		60		ns
tcWL	CAS hold time after W low	15		20		ns
trWL	RAS hold time after W low	15		20		ns
tWP	Write pulse width	10		10		ns
tDS	Data setup time before W low	0		0		ns
tDH	Data hold time after W low	10		15		ns
toEH	OE hold time after W low	15		15		ns

Note 22: trWC is specified as  $trWC_{(min)} = tRAC_{(max)} + tODD_{(min)} + tRWL_{(min)} + tRP_{(min)} + 5t$ .

23: tWCS, tcWD, trWD and tAWD and, tcPWD are specified as reference points only. If tWCS<sub>(min)</sub> the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tcWD tcWD<sub>(min)</sub>, trWD trWD<sub>(min)</sub>, tAWD tAWD<sub>(min)</sub> and tcPWD tcPWD<sub>(min)</sub> (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to V<sub>ih</sub>) is indeterminate.

### Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time	85		95		ns
tRAS	RAS low pulse width for read write cycle (Note25)	100	125000	115	125000	ns
tCP	CAS high pulse width (Note26)	10	15	10	15	ns
tcPRH	RAS hold time after CAS precharge	35		40		ns
tcPWD	Delay time, CAS precharge to W low (Note23)	60		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25: tRAS<sub>(min)</sub> is specified as two cycles of CAS input are performed.

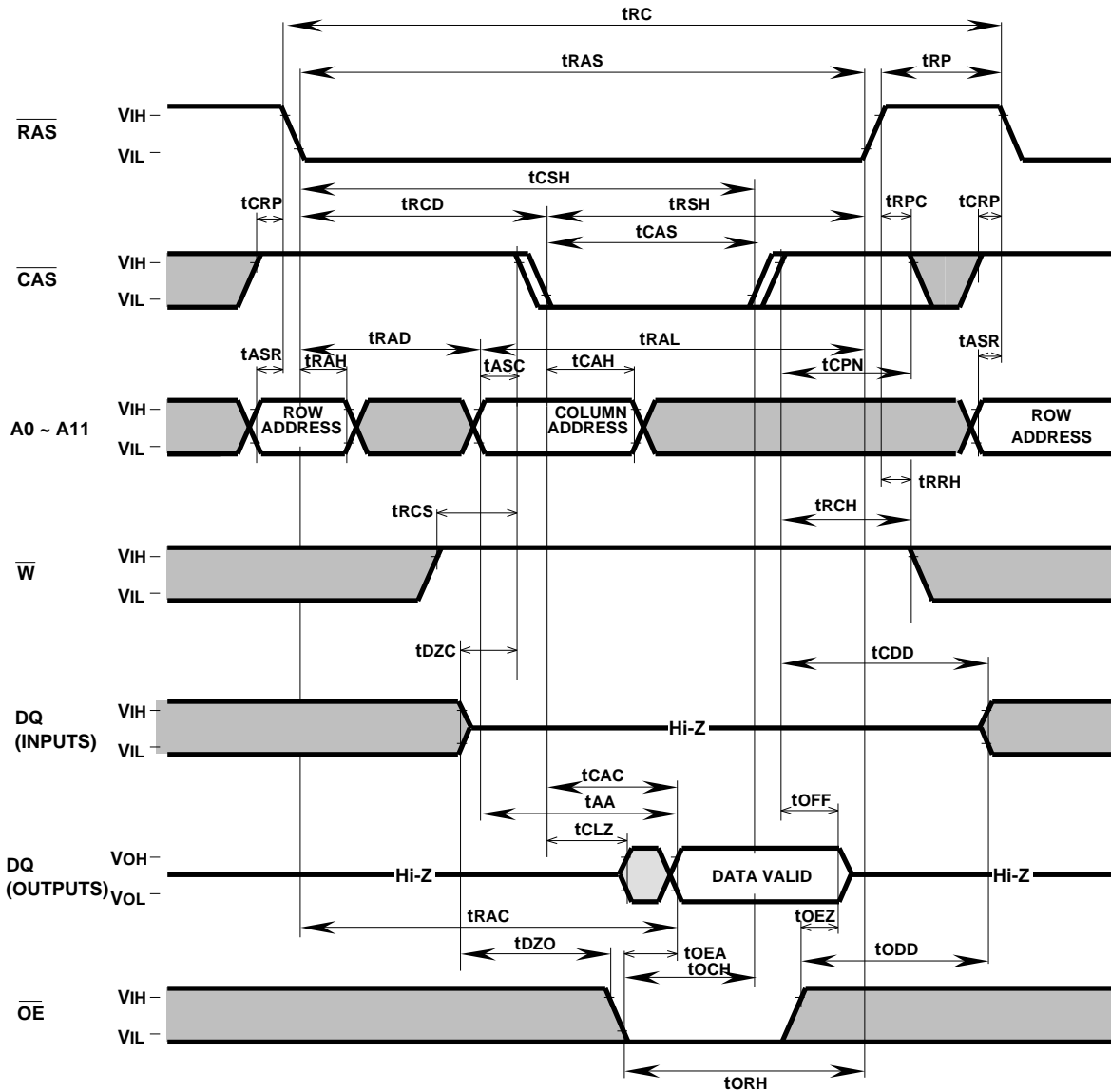
26: tCP<sub>(max)</sub> is specified as a reference point only.

### CAS before RAS Refresh Cycle (Note 27)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
tCSR	CAS setup time before RAS low	10		10		ns
tCHR	CAS hold time after RAS low	10		15		ns
tRSR	Read setup time before RAS low	10		10		ns
trHR	Read hold time after RAS low	10		15		ns

Note 27: Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

Timing Diagrams (Note 28)  
Read Cycle



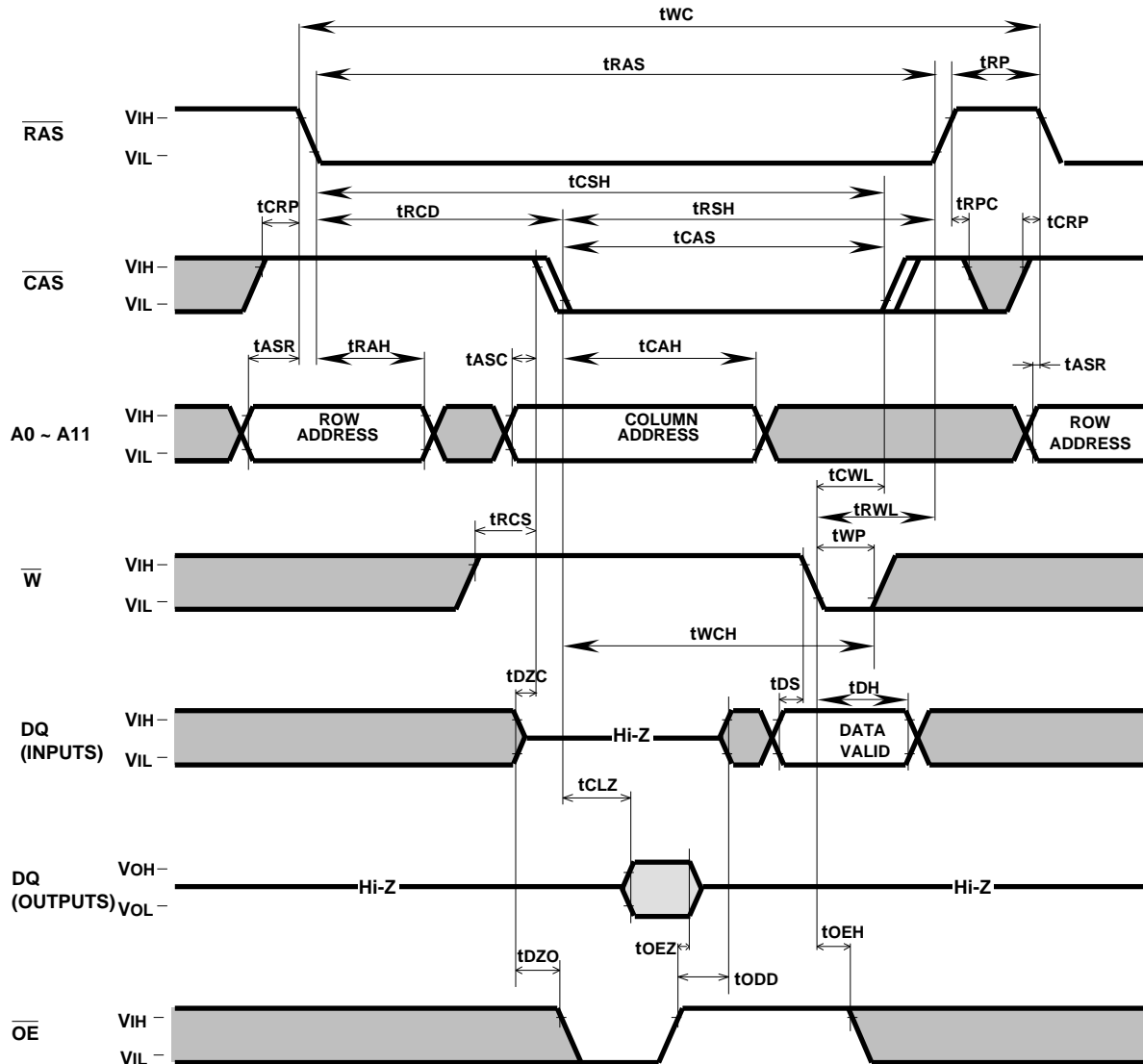
Note 28

- Indicates the don't care input.  
VIH(min) VIN VIH(max) or VIL(min) VIN VIL(max)
- Indicates the invalid output.
- Indicates the skew of the four inputs.

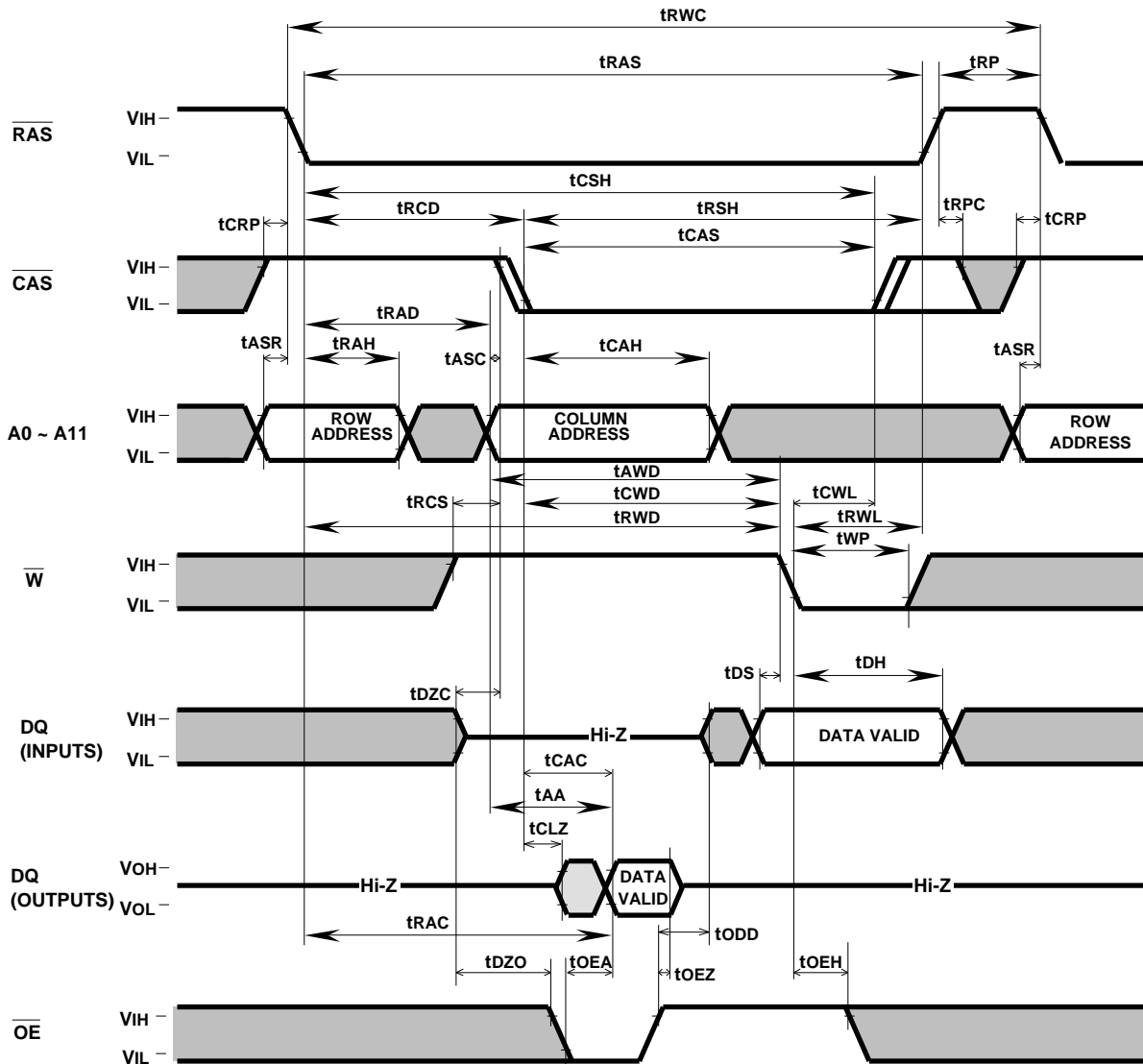




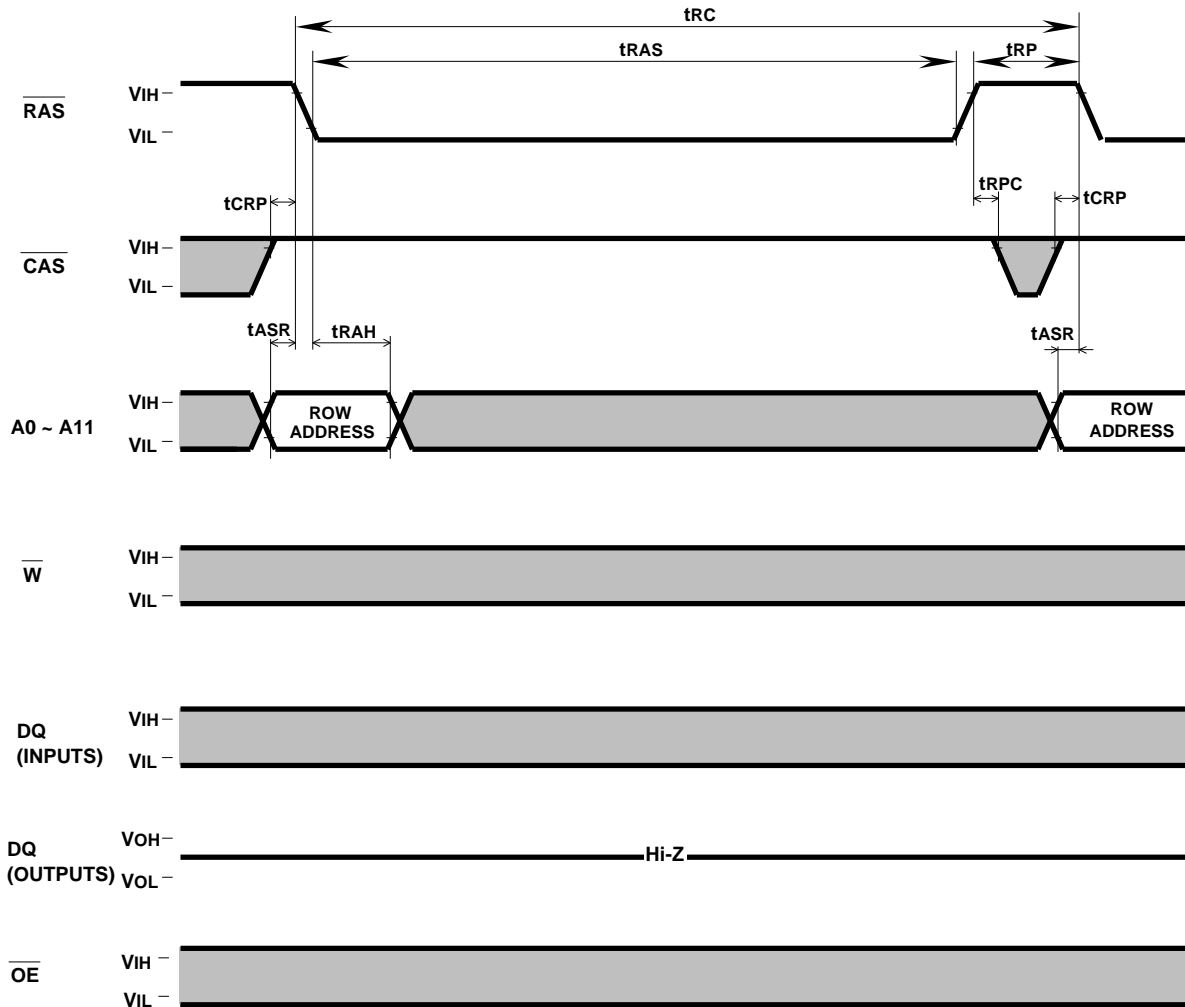
Write Cycle (Delayed write)



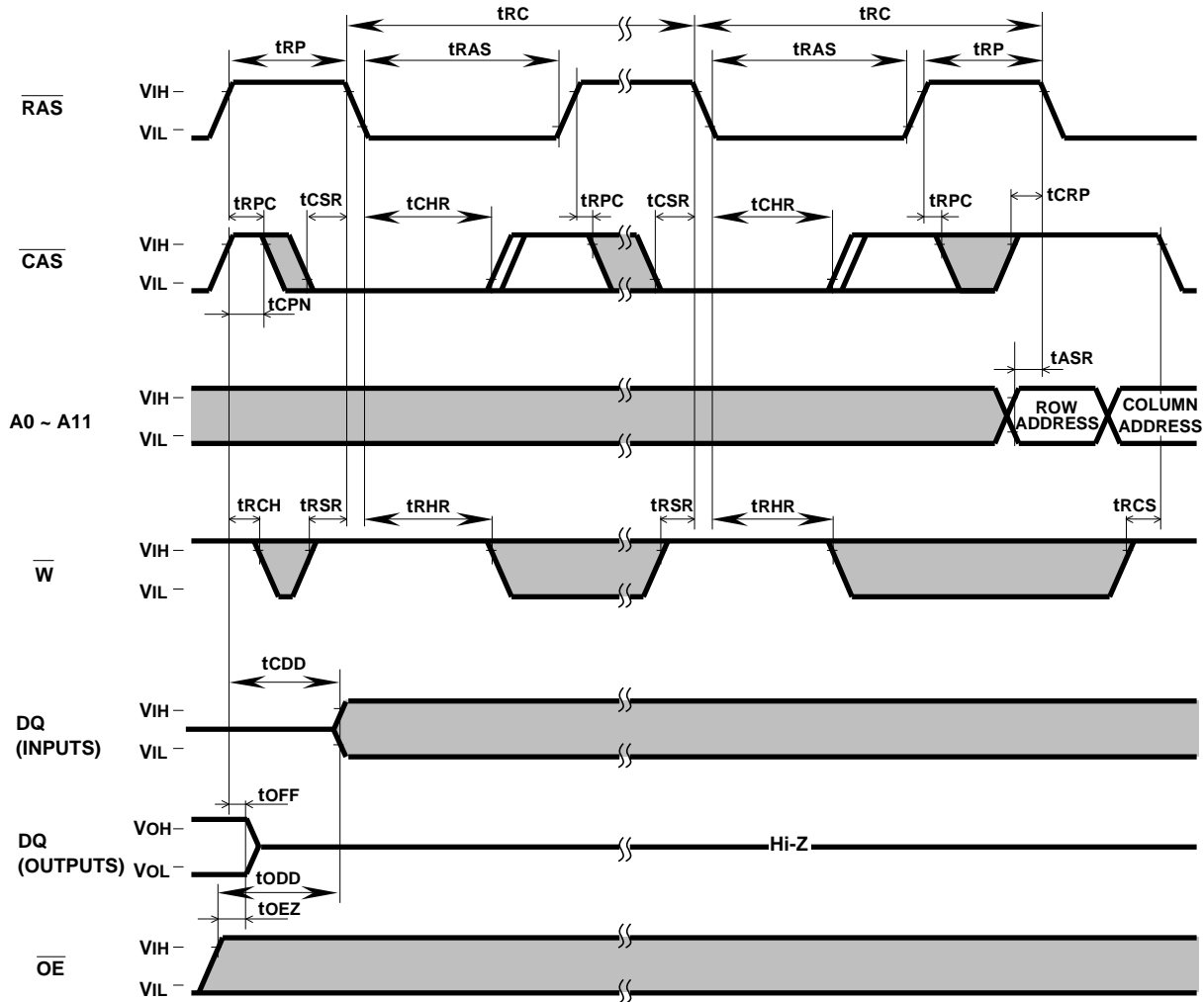
Read-Write, Read-Modify-Write Cycle



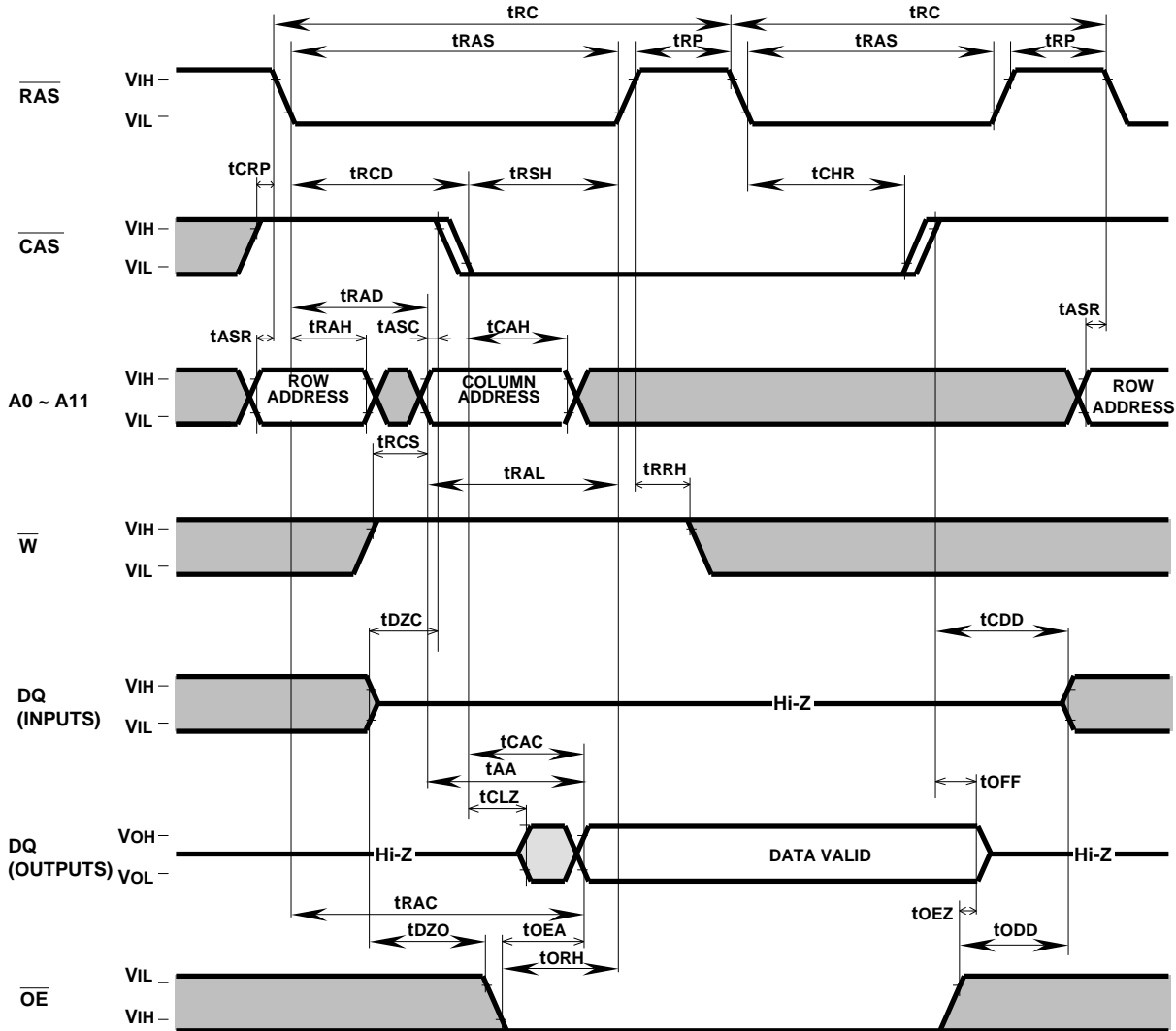
RAS-only Refresh Cycle



CAS before RAS Refresh Cycle



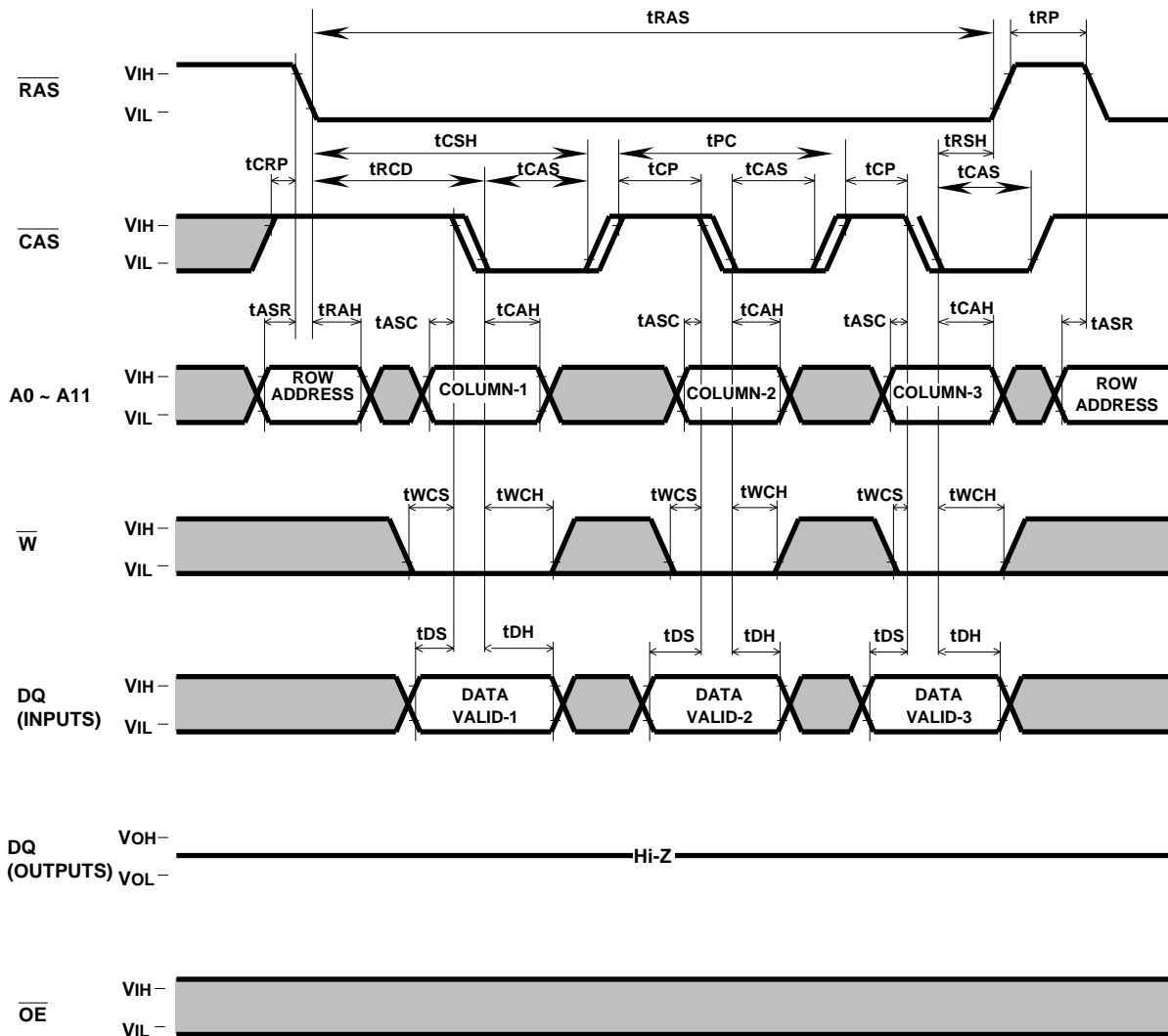
Hidden Refresh Cycle (Read) (Note 29)



Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.



Fast Page Mode Write Cycle (Early Write)









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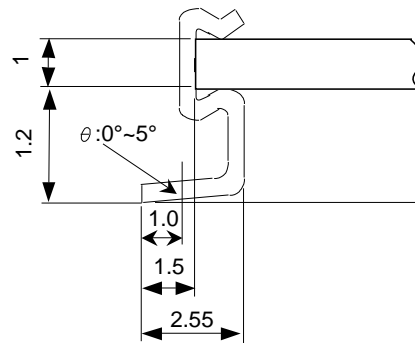
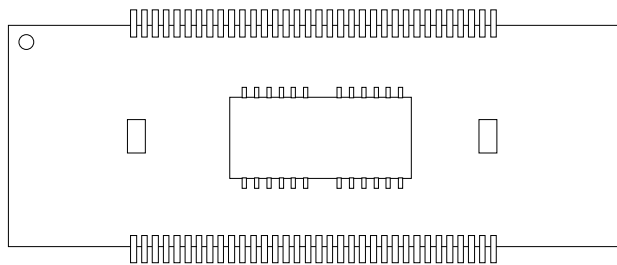
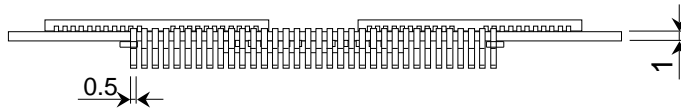
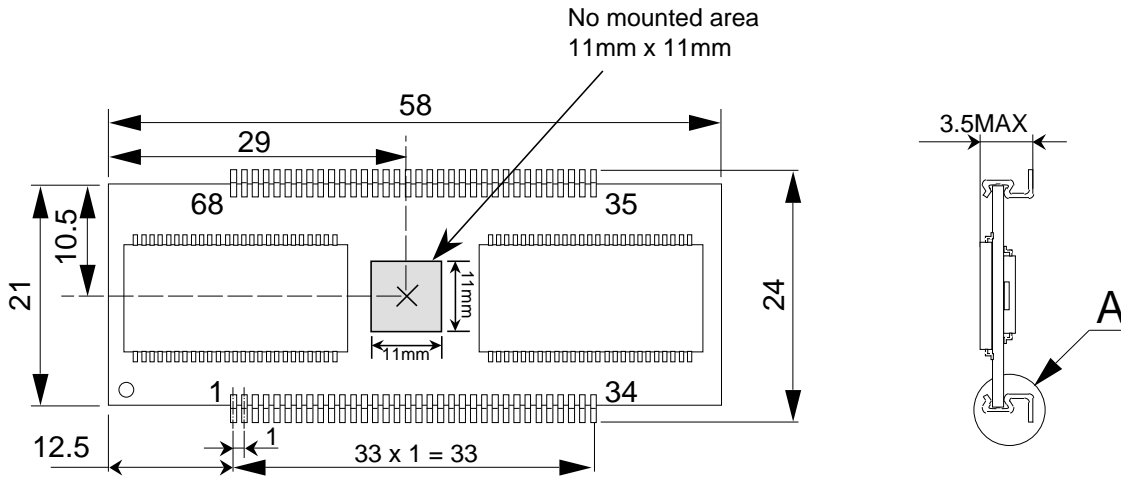
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### MH4V36AM OUTLINE



**Detail A**