Micro Linear

ML2261*

μP Compatible High-Speed 8-Bit A/D Converter with T/H (S/H)

GENERAL DESCRIPTION

The ML2261 is a high-speed, μP compatible 8-bit A/D converter with a conversion time of 670ns over the operating temperature range and supply voltage tolerance. The ML2261 operates from a single 5V supply and has an analog input range from GND to V_{CC}.

The ML2261 has two different pin selectable modes. The T/H mode has an internal track and hold. The S/H mode has a true internal sample and hold and can digitize 0 to 5V sinusoidal signals as high as 500kHz. Timing is compatible with the AD7821.

The ML2261 digital interface has been designed so that the device appears as a memory location or I/O port to a μP.

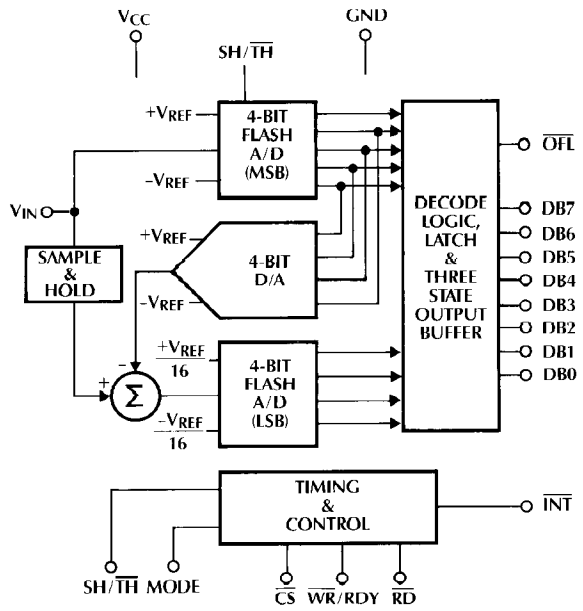
The ML2261 is an enhanced, pin compatible second source for the industry standard ADC0820 and AD7820. The ML2261 enhancements are faster conversion time, parameters guaranteed over the supply tolerance and temperature range, improved digital interface timing, superior power supply rejection, and better latchup immunity on analog inputs.

FEATURES

- Conversion time, WR-RD mode over temperature and supply voltage tolerance
  - Track & Hold Mode ..... 850ns max
  - Sample & Hold Mode ..... 700ns max
- Total unadjusted error ..... ±1/2 LSB or ±1 LSB
- Digitizes a 5V, 250kHz sine wave to 8-bit accuracy
- No missing codes
- 0V to 5V analog input range with single 5V power supply
- No zero or full scale adjust required
- Analog input protection ..... 25mA min
- Operates ratiometrically or with up to 5V voltage reference
- No external clock required
- Easy interface to μP, or operates stand alone
- Power-on reset circuitry
- Low power 75mW
- Standard 20-pin DIP or surface mount PCC
- Superior pin compatible replacement for ADC0820 and AD7820

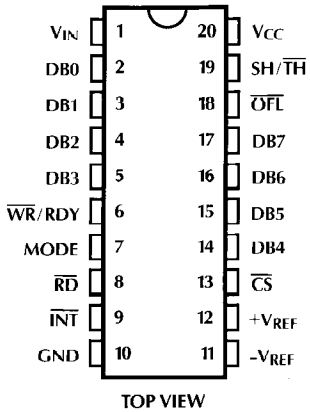
* This Part Is End Of Life As Of August 1, 2000

BLOCK DIAGRAM



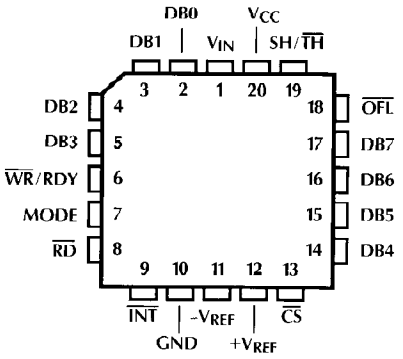
PIN CONNECTIONS

20-Pin DIP



TOP VIEW

20-Pin PCC



TOP VIEW

PIN DESCRIPTION

PIN NO.	NAME	FUNCTION
1	V_{IN}	Analog input.
2	DB0	Data output — bit 0 (LSB).
3	DB1	Data output — bit 1.
4	DB2	Data output — bit 2.
5	DB3	Data output — bit 3.
6	$\overline{WR}$/RDY	Write input or ready output. In WR-RD mode, this pin is WR input. In RD mode, this pin is RDY open drain output. See Digital Interface section.
7	MODE	Mode select input. MODE = GND: RD mode MODE = V_{CC}: WR-RD mode Pin has internal current source pulldown to GND.
8	$\overline{RD}$	Read input. In RD mode, this pin initiates a conversion. In WR-RD mode, this pin latches data into output latches. See Digital Interface section.
9	$\overline{INT}$	Interrupt output. This output signals the end of a conversion and indicates that data is valid on the data outputs. See Digital Interface section.
10	GND	Ground.
11	$-V_{REF}$	Negative reference voltage for A/D converter.
12	$+V_{REF}$	Positive reference voltage for A/D converter.
13	$\overline{CS}$	Chip select input. This pin must be held low for the device to perform a conversion.
14	DB4	Data output — bit 4.
15	DB5	Data output — bit 5.
16	DB6	Data output — bit 6.
17	DB7	Data output — bit 7 (MSB).
18	$\overline{OFL}$	Overflow output. This output goes low at end of conversion if V_{IN} is greater than $+V_{REF}$ – ½LSB.
19	SH/$\overline{TH}$	S/H, T/H mode select. When SH/$\overline{TH}$ = V_{CC}, the device is in sample and hold mode. When SH/$\overline{TH}$ = GND, the device is in track and hold mode. Pin has internal pulldown current source to GND.
20	V_{CC}	Positive supply. +5 volts ± 5%.

ABSOLUTE MAXIMUM RATINGS
(Note 1)

Supply Voltage, V_{CC} 6.5V
Voltage
- Logic Inputs ..... –0.3V to V_{CC} + 0.3V
- Analog Inputs ..... –0.3V to V_{CC} + 0.3V

Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation
- at T_A = 25°C (Board Mount) 875mW

Lead Temperature (Soldering 10 sec.)
- Dual-In-Line Package (Plastic) ..... 260°C
- Dual-In-Line Package (Ceramic) ..... 300°C
- Molded Chip Carrier Package
  - Vapor Phase (60 sec.) ..... 215°C
  - Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... $4.5V_{DC}$ to $6.0V_{DC}$
Temperature Range (Note 3) ..... $T_{MIN} \leq T_A \leq T_{MAX}$
- ML2261BCQ, ML2261CCQ
- ML2261BCP, ML2261CCP ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, and $-V_{REF} = GND$

PARAMETER	NOTES	CONDITIONS	ML2261XCX MIN	ML2261XCX TYP (Note 4)	ML2261XCX MAX	ML2261XIX MIN	ML2261XIX TYP (Note 4)	ML2261XIX MAX	UNITS
Converter									
Total Unadjusted Error ML2261BXX ML2261CXX	5, 7	$V_{REF} = V_{CC}$			 ±1/2 ±1			 ±1/2 ±1	 LSB LSB
$+V_{REF}$ Voltage Range	6		$-V_{REF}$		$V_{CC}+0.1$	$-V_{REF}$		$V_{CC}+0.1$	V
$-V_{REF}$ Voltage Range	6		GND–0.1		$+V_{REF}$	GND–0.1		$+V_{REF}$	V
Reference Input Resistance	5		1	2	3	1	2	3	kΩ
Analog Input Range	5, 8		GND–0.1		$V_{CC}+0.1$	GND–0.1		$V_{CC}+0.1$	V
Power Supply Sensitivity	5	DC V_{CC} = 5V ± 5%, V_{REF} = 4.75V		±1/32	±1/4		±1/32	±1/4	LSB
		100mVp-p 100kHz sine on V_{CC}, V_{IN} = 0		±1/16			±1/16		LSB
Analog Input Leakage Current	5, 9	Converter Idle	–1		+1	–1		+1	µA
Analog Input Capacitance		During Acquisition Period		45			45		pF
Digital and DC									
$V_{IN(1)}$, Logical "1" Input Voltage	5	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$	2.0			2.0			V
		MODE, SH/$\overline{TH}$	V_{CC}–0.5			V_{CC}–0.5			V
$V_{IN(0)}$, Logical "0" Input Voltage	5	$\overline{WR}$, $\overline{RD}$, $\overline{CS}$			0.8			0.8	V
		MODE, SH/$\overline{TH}$			0.5			0.5	V
$I_{IN(1)}$, Logical "1" Input Current	5	$V_{IH} = V_{CC}$; $\overline{WR}$, $\overline{RD}$, $\overline{CS}$			1			1	µA
		$V_{IH} = V_{CC}$; MODE, SH/$\overline{TH}$	15	50	150	15	50	150	µA
$I_{IN(0)}$, Logical "0" Input Current	5	V_{IL} = GND; $\overline{WR}$, $\overline{RD}$, $\overline{CS}$	–1			–1			µA
		V_{IL} = GND; MODE, SH/$\overline{TH}$	–20			–20			µA
$V_{OUT(1)}$, Logical "1" Output Voltage	5	I_{OUT} = –2mA	4.0			4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	5	I_{OUT} = 2mA			0.4			0.4	V
I_{OUT}, Three-State Output Current	5	V_{OUT} = 0V	–1			–1			µA
		$V_{OUT} = V_{CC}$			1			1	µA
C_{OUT}, Logic Output Capacitance				5			5		pF
C_{IN}, Logic Input Capacitance				5			5		pF
I_{CC}, Supply Current	5	$\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = "1" No Output Load		8	14		8	15.5	mA

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, $-V_{REF} = GND$, and timing measured at 1.4V, $C_L = 100pF$.

PARAMETER	NOTES	CONDITIONS	ML2261XCX MIN	ML2261XCX TYP (Note 4)	ML2261XCX MAX	ML2261XIX MIN	ML2261XIX TYP (Note 4)	ML2261XIX MAX	UNITS
AC and Dynamic Performance (Note 9)									
t_{CRD}, Conversion Time, Read Mode	5	$\overline{RD}$ to $\overline{INT}$, MODE = 0V			1060			1100	ns
t_{CWR-RD}, Conversion Time, Write-Read Mode	5, 9	$\overline{WR}$ Falling Edge to $\overline{INT}$, $t_{RD} < t_{INT}$, MODE = V_{CC}; SH/$\overline{TH}$=V_{CC}		650	700		690	740	ns
		SH/$\overline{TH}$=GND			850			920	ns
SNR, Signal to Noise Ratio		V_{IN} = 5V, 250kHz Noise is sum of all nonfundamental components from 0–500kHz. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1 MHz		48			48		dB
HD, Harmonic Distortion		V_{IN} = 5V, 250kHz THD is sum of 2–5th harmonics relative to fundamental. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1 MHz		–63			–63		dB
IMD, Intermodulation Distortion		fa = 2.5V, 250kHz fb = 2.5V, 248kHz IMB is (fa + fb), (fa – fb), (2fa + fb), (2fa – fb), (fa + 2fb), or (fa – 2fb) relative to fundamental. SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1 MHz		–60			–60		dB
FR, Frequency Response		V_{IN} = 5V, 0–250kHz Relative to 1kHz SH/$\overline{TH}$ = V_{CC}, MODE = V_{CC} $f_{SAMPLING}$ = 1 MHz		±0.1			±0.1		dB
SR, Slew Rate Tracking	6	SH/$\overline{TH}$ = V_{CC}			4.0			4.0	V/μs
		SH/$\overline{TH}$ = GND			.25			.25	V/μs
AC Performance Read Mode (Pin 7 = 0V), Figure 2									
t_{RDY}, $\overline{CS}$ to RDY Delay	5		0		65	0		70	ns
t_{RDD}, $\overline{RD}$ Low to RDY Delay	5, 10	Figure 1			1060			1100	ns
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	5		0			0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	5		0			0			ns
t_{CRD}, Conversion Time — $\overline{RD}$ Low to $\overline{INT}$ Low	5, 10				1060			1100	ns

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = +V_{REF} = 5V \pm 5\%$, $-V_{REF}$ = GND, and timing measured at 1.4V, C_L = 100pF

PARAMETER	NOTES	CONDITIONS	ML2261XCX MIN	ML2261XCX TYP (Note 4)	ML2261XCX MAX	ML2261XIX MIN	ML2261XIX TYP (Note 4)	ML2261XIX MAX	UNITS
AC Performance Read Mode (Pin 7 = 0V), Figure 2 (Continued)									
t_{ACC0}, Data Access Time $\overline{RD}$ to Data Valid	5		t_{CRD}		t_{CRD}+30	t_{CRD}		t_{CRD}+30	ns
t_{RDPW}, $\overline{RD}$ Pulse Width	5		t_{CRD}+30			t_{CRD}+30			ns
t_{INTH}, $\overline{RD}$ to $\overline{INT}$ Delay	5, 10		0		65	0		70	ns
t_{DH}, Data Hold Time — $\overline{RD}$ Rising Edge to Data High Impedance State	6, 10	Figure 1	0		50	0		60	ns
t_P, Delay Time Between Conversions — $\overline{INT}$ Low to $\overline{RD}$ Low	5, 10	Sample & Hold Mode, SH/$\overline{TH}$ = V_{CC}	300			325			ns
		Track & Hold Mode, SH/$\overline{TH}$ = GND	240			260			ns
AC Performance Write-Read Mode (Pin 7 = 5V), Figures 3 and 4									
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	5		0			0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	5		0			0			ns
t_{WR}, $\overline{WR}$ Pulse Width	5	SH/$\overline{TH}$ = V_{CC}	170		50K	180		50K	ns
	6	SH/$\overline{TH}$ = GND	320		50K	360		50K	ns
t_{RD}, Read Time — $\overline{WR}$ High to $\overline{RD}$ Low Delay	5	$t_{RD} < t_{INTL}$	275			290			ns
t_{RI}, $\overline{RD}$ to $\overline{INT}$ Delay	5, 10	$t_{RD} < t_{INTL}$	0		255	0		270	ns
t_{ACC1}, Data Access Time — $\overline{RD}$ Low to Data Valid	5	$t_{RD} < t_{INTL}$	0		260	0		280	ns
t_{CWR-RD}, Conversion Time — $\overline{WR}$ Falling Edge to $\overline{INT}$ Low	5,9,10	$t_{RD} < t_{INTL}$, SH/$\overline{TH}$ = V_{CC}		650	700		690	740	ns
	6,9,10	$t_{RD} < t_{INTL}$, SH/$\overline{TH}$ = GND			850			920	ns
t_{INTL}, Internal Comparison Time — $\overline{WR}$ Rising Edge to $\overline{INT}$ Low	5, 10	$t_{RD} > t_{INTL}$			650			670	ns
t_{ACC2}, Data Access Time — $\overline{RD}$ to Data Valid	5	$t_{RD} > t_{INTL}$	0		50	0		60	ns
t_{DH}, Data Hold Time — $\overline{RD}$ Rising Edge to Data High Impedance State	6, 10	Figure 1	0		50	0		60	ns
t_{INTH}, $\overline{RD}$↑ to $\overline{INT}$↑ Delay	5, 10		0		65	0		70	ns
t_P, Delay Time Between Conversions — $\overline{INT}$ Low to $\overline{WR}$ Low	5, 10	Sample & Hold Mode, SH/$\overline{TH}$ = V_{CC}	300			325			ns
		Track & Hold Mode, SH/$\overline{TH}$ = GND	240			260			ns
t_{IHWR}, $\overline{WR}$↑ to $\overline{INT}$↑ Delay	5, 10	Standalone Mode	0		100	0		110	ns
t_{ID}, $\overline{INT}$↓ to Data Valid Delay	5, 10	Standalone Mode	0		20	0		30	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: When the voltage at any pin exceeds the power supply rails (V_{IN} < GND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: 0°C to 70°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full scale, linearity, and sample and hold errors. Total unadjusted error is tested at the minimum specified times for $\overline{WR}$, $\overline{RD}$, t_{RI}, and t_P. For example, for the ML2261XCX in the sample and hold mode, $\overline{WR}/\overline{RD}$ mode: t_{WR} = 170ns, t_{RD} = 275ns with a frequency of 1.000MHz (cycle time of 1000ns).

Note 8: For $-V_{REF} \geq V_{IN}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to the analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct – especially at elevated temperatures, and cause errors for analog inputs near full scale. This spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input range will therefore require a minimum supply voltage of $4.900V_{DC}$ over temperature variations, initial tolerance and loading.

Note 9: Conversion time, write-read mode = $t_{WR} + t_{RD} + t_{RI}$.

Note 10: Defined from the time an input crosses 0.8V or 2.4V.

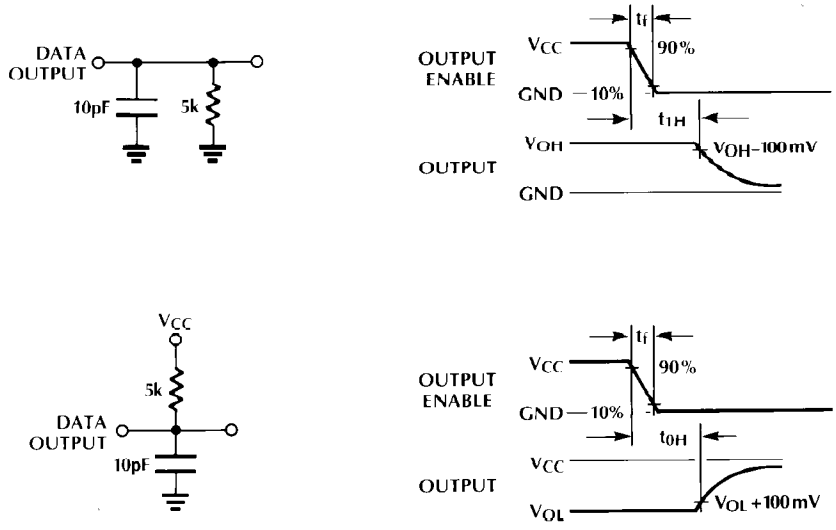


Figure 1. High Impedance Test Circuits and Waveforms

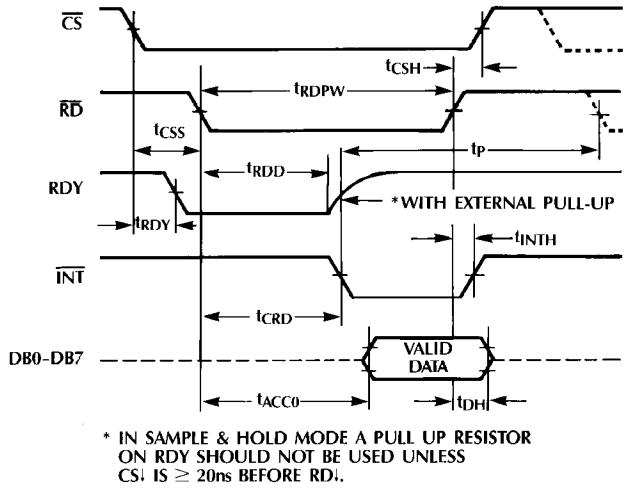


Figure 2. RD Mode Timing

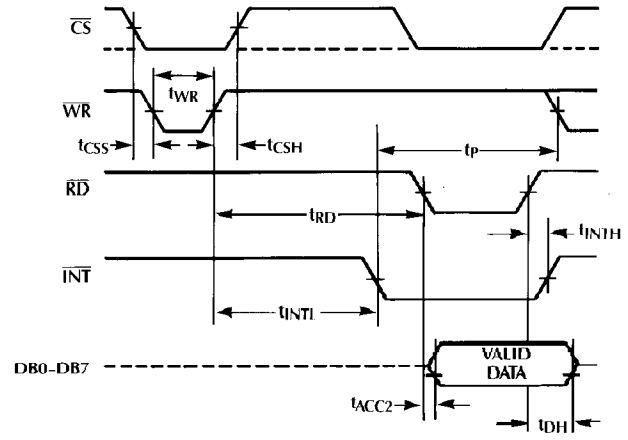


Figure 3. WR-RD Mode Timing ($t_{RD} > t_{INTL}$)

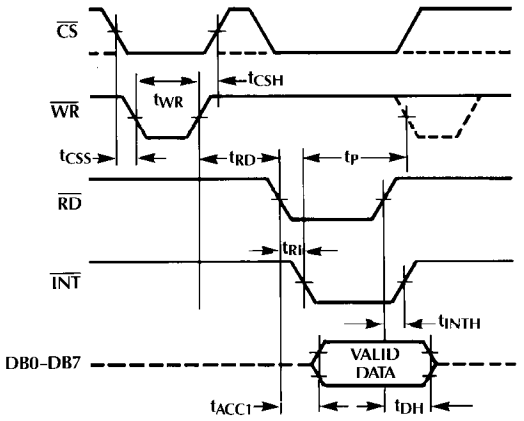


Figure 4. WR-RD Mode Timing ($t_{RD} < t_{INTL}$)

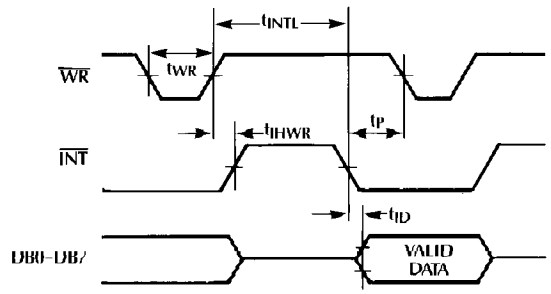


Figure 5. WR-RD Mode Stand-Alone Timing $\overline{CS}$ = $\overline{RD}$ = 0

1.0 FUNCTIONAL DESCRIPTION

The ML2261 uses a two stage flash technique for A/D conversion. This technique first performs a 4 bit flash conversion on V_{IN} to determine the 4 MSB's. These 4 MSB's are then cycled through an internal DAC to recreate the analog input. This reconstructed analog input signal from the DAC is then subtracted from the input, and the difference voltage is converted by a second 4 bit flash conversion, providing the 4 LSB's of the output data word. An additional overrange function detects if V_{IN} is greater than $+V_{REF}$ – ½LSB.

1.1 ANALOG INPUT

The analog input on the ML2261 behaves differently from inputs on conventional converters. The analog input current requirements change while the conversion is in progress, and the amount of input current depends on what cycle the converter is in.

The equivalent input circuit for the converter is shown in Figure 6. When the conversion starts in the T/H mode (WR↓ in the WR-RD mode or RD↓ in the RD mode) S1, S4 and S6 close and S3 opens. This period is known as the acquisition period where the MSB flash converter tracks the input signal and the LSB flash converter samples it. During this period, V_{IN} is connected to the 16 MSB and 15 LSB comparators. Thus 38 pF of input capacitance must be charged up through the combined R_{ON} resistance of the internal analog switches plus any external source resistance, R_S. In addition, there is a stray capacitance of approximately 11 pF that needs to be charged through the external source resistance R_S. This period ends in the WR-RD mode when WR↑ or by an internal timer in the RD mode. At this point S1 and S4 open and the analog input at V_{IN} is no longer being sampled; thus during this time the analog voltage on V_{IN} does not affect converter performance.

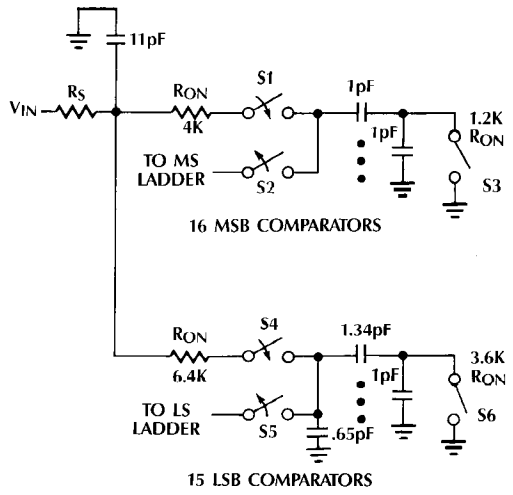


Figure 6. Converter Equivalent Input Circuit

As shown above, the critical period for charging up the analog input occurs when the MSB and LSB comparators are sampling the input, known as the acquisition period. The source of the external signal on V_{IN} must adequately charge up the analog voltage during the acquisition period. To do this, the input must settle within the required analog accuracy tolerance at least 50ns before the end of the acquisition period so that the MSB comparators have adequate time to make the correct decision. If more time is needed due to finite charging or settling time of the external source, the WR low period can be extended in WR-RD mode. In RD mode, since the acquisition time is fixed by internal delays, the burden is on the external source to charge up and settle the input adequately.

When the ML2261 operates in the S/H mode (pin 19 = V_{CC}) both the MSB and the LSB flash converter perform a true sample and hold operation during the acquisition or sampling period. This period starts after the falling edge of INT and ends with the falling edge of WR in the WR-RD mode or the falling edge of RD in the RD mode. The duration of this period is user controlled and must satisfy a minimum of t_P.

During this period S1, S3, S4 and S6 close, therefore 46 pF of input capacitance must be charged up in addition to the 11 pF of stray capacitance.

1.2 TRACK AND HOLD vs. SAMPLE AND HOLD

The MSB Flash Converter of the ML2261 in T/H mode has a track and hold mechanism for sampling the input. The input is attached to the MSB comparators directly in the MSB compare cycle, or acquisition period. When the MSB compare cycle ends, the state of the MSB comparators is latched. The LSB Flash Converter always performs a S/H operation. Thus, the analog input signal can be changing during the MSB compare cycle, or acquisition period, and the MSB comparators will be tracking it as long as the slew rate of the analog input is slow enough so that the MSB comparators can respond. The ML2261 can track and hold signals with slew rates as high as .25V/μs (16kHz @ 5 volts) without sacrificing conversion accuracy.

The ML2261 in S/H mode does not have the slew rate limitation of the T/H mode since an internal sample and hold acquires the analog signal, holds it internally, and then performs a conversion. Since this is a true sample and hold function, the S/H mode can theoretically digitize signals of frequencies much higher than the T/H mode. The ML2261 in S/H mode can digitize signals of frequencies as high as 250kHz @ 5V (slew rates as high as 4V/μs) without sacrificing conversion accuracy. In most applications, the S/H mode is more desirable than T/H mode because of the better dynamic performance.

1.2.1 CONVERTER — T/H MODE

The operating sequence for the WR-RD mode is illustrated in Figure 7a. Initially, the internal comparators are auto-zeroed while WR is high. A conversion is initiated by the falling edge of WR. While WR is low, the MSB comparators are tracking the analog input and comparing this voltage against voltages from the internal resistor ladder. At the same time, the input is being acquired or sampled by LSB comparators. On the rising edge of WR, the MSB comparator results are latched, and the LSB acquisition time is ended by closing the sampling switch to the LSB comparators. While WR is high, the LSB comparators then compare the residual input voltage against internal voltages from the resistor ladder to determine the 4 LSB's. When the LSB comparison or conversion is complete, INT goes low and latches the conversion result into the output latches. Then, the comparators are auto-zeroed while WR is high before another conversion can start.

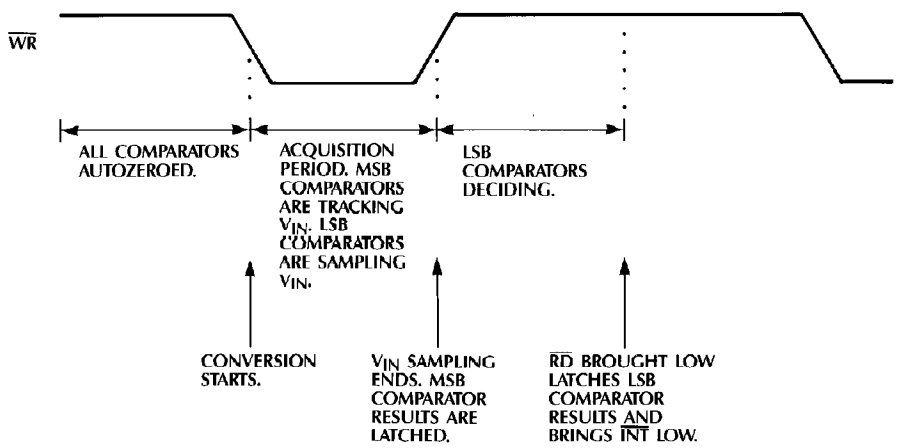
The operating sequence for RD mode, is similar to that described above for the WR-RD mode, except the conversion is initiated by the falling edge of RD, and the MSB and LSB conversions are generated by internal clock edges that are generated while RD is low.

1.2.2 CONVERTER — S/H MODE

The operating sequence for S/H mode is illustrated in Figure 7b. Notice that it is similar to T/H mode described above except this mode has a true sample and hold function. The falling edge of INT closes the sampling switch and starts the acquisition period where the analog input is sampled at the same time all comparators are auto-zeroed. The falling edge of WR opens the internal sampling switch, ends the acquisition period, and starts the conversion on the internally sample and held signal. The MSB comparators make their decisions while WR is low. On the rising edge of WR, the MSB comparator results are latched. The LSB comparators make their decision when WR is high. When the LSB comparison or conversion is complete, INT goes low and latches the conversion result into the output buffers. Then, the acquisition period begins again and the converter is ready for the next conversion.

The operating sequence for the RD mode is the same as the WR-RD mode, except the conversion is initiated by the falling edge of RD, and the MSB and LSB conversions are generated by internal clock edges that are generated while RD is low.

a). T/H Mode



b). S/H Mode

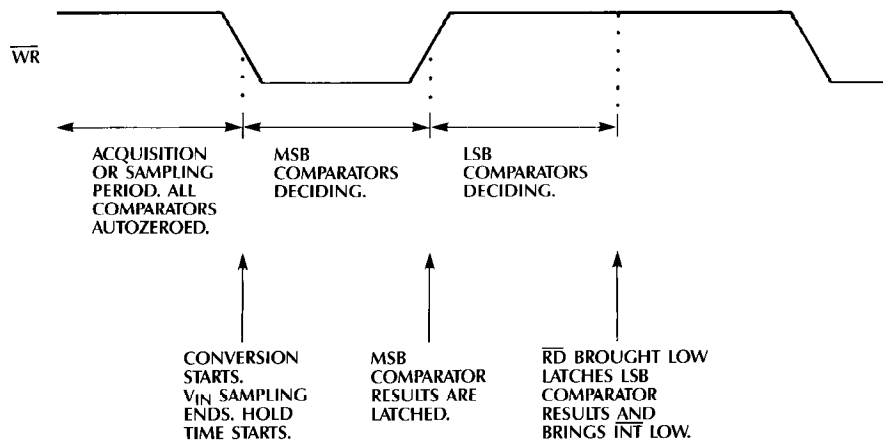


Figure 7. Operating Sequence (WR-RD Mode)

1.3 REFERENCE

The $+V_{REF}$ and $-V_{REF}$ inputs are the reference voltages that determine the full scale and zero input voltages, respectively, for the A/D converter. Thus, $+V_{REF}$ defines the analog input which produces a full scale output and $-V_{REF}$ defines the analog input which produces an output code of all zeroes. The transfer function for the A/D converter is shown in Figure 8.

$+V_{REF}$ and $-V_{REF}$ can be set to any voltage between GND and V_{CC}. This means that the reference voltages can be offset from GND and the difference between $+V_{REF}+$ and $-V_{REF}-$ can be made small to increase the resolution of the conversion. Note that the total unadjusted error increases when $[+V_{REF} - (-V_{REF})]$ decreases.

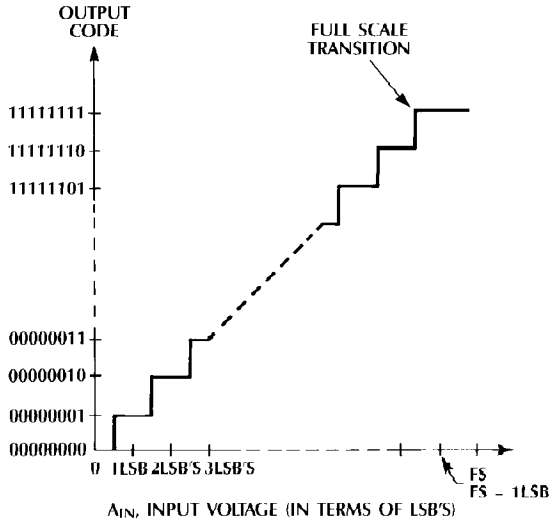


Figure 8. A/D Transfer Characteristic

1.4 POWER SUPPLY AND REFERENCE DECOUPLING

A 0.1μF ceramic disc capacitor is recommended to bypass V_{CC} to GND, using as short a lead length as possible.

If REF+ and REF– inputs are driven by long lines, they should be bypassed by 0.1μF ceramic disc capacitors at the reference input pins.

1.5 DYNAMIC PERFORMANCE

1.5.1 SINUSOIDAL INPUTS

Since the ML2261 has an internal sample and hold, the device can digitize high frequency sinusoids with little or no signal degradations. Using the Nyquist criteria, the highest frequency input to the converter could theoretically be 1/2 the sampling rate (f_S). Any frequency components above $f_S/2$ will be aliased below $f_S/2$. In most applications, these aliased components cause unacceptable distortion and must be filtered out of the input. If the input frequency is too close to $f_S/2$, then the requirements on the anti-alias filter become difficult to impossible to realize with standard component and tolerances. In most practical applications, the highest input frequency has to be limited to 1/3 to 1/4 of f_{max} in order to relax the filtering requirements enough to make a realizable anti-alias filter.

The maximum sampling rate (f_{max}) for the ML2261 in the WR-RD mode, ($t_{RD} < t_{INTL}$) can be calculated as follows:

$$f_{max} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_P}$$

$$f_{max} = \frac{1}{170ns + 275ns + 255ns + 300ns}$$

f_{max} = 1.00 MHz

t_{WR} = Write Pulse Width

t_{RD} = Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses

t_{RI} = $\overline{RD}$ to $\overline{INT}$ Delay

t_P = Delay Time between Conversions

This permits a maximum sampling rate of 1MHz for the ML2261. The dynamic performance specifications (SNR, HD, IMD, and FR) for the ML2261 are all specified at 250kHz, which is approximately 1/4 of the sampling rate, f_S.

In applications where aliased frequency components are acceptable and filtering of the input signal is not needed or where a filter with a steep amplitude response is available, the user can apply an input sinusoid higher than 250kHz to the device. Note, however, that as the input frequency increases above 500kHz, dynamic performance degradation will occur due to the finite bandwidth of the internal sample and hold.

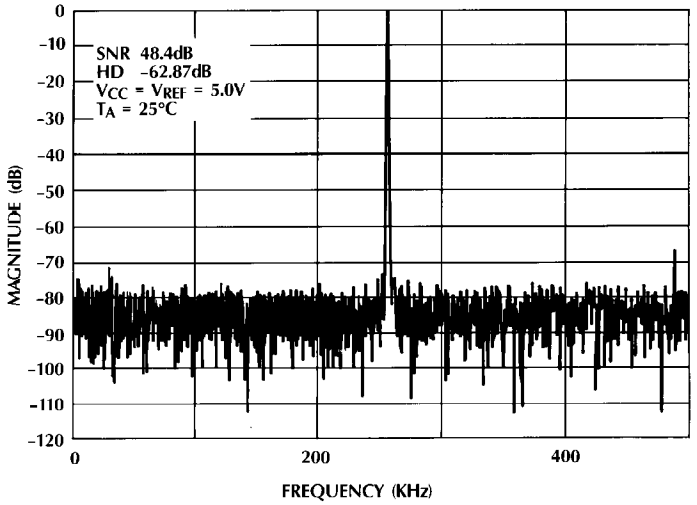
The Figure 9 plots are 4096 point FFT's of the ML2261 converting a 257kHz and a 491kHz, 0 to 4.5V, low distortion sine wave input. The ML2261 samples and digitizes at its specified accuracy, dynamic input signals with frequency components up to the Nyquist frequency (one-half the sampling rate). The output spectra yields precise measurements of the input signal level, harmonic components, and signal to noise ratio up to the 8-bit level. The near ideal signal to noise ratio is maintained independent of increasing analog input frequencies to 500kHz.

1.5.2 SIGNAL-TO-NOISE RATIO

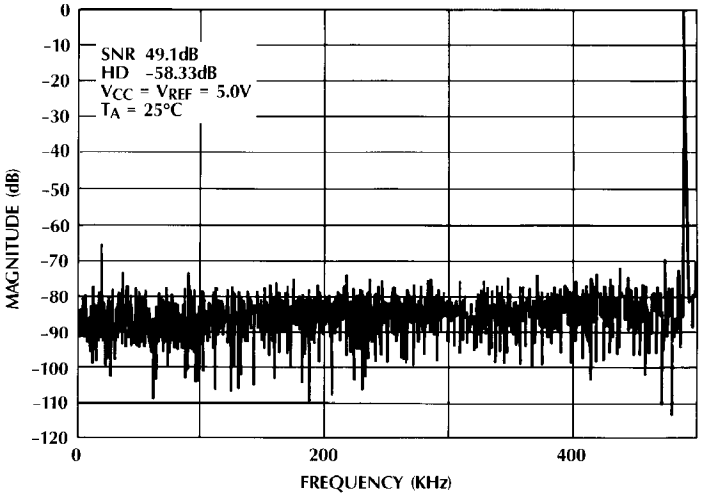
Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more the levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for ideal 8-bit converter, SNR = 49.92 dB.



a) Ouput Spectrum with f_{IN} = 257kHz, f_S = 1MHz



b) Output Spectrum with f_{IN} = 491kHz, f_S = 1MHz

Figure 9. Dynamic Performance, Sample and Hold Mode

1.5.3 HARMONIC DISTORTION

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2261 is defined as

$$20 \log \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

1.5.4 INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms $(f_A + f_B)$ and $(f_A - f_B)$ and the third order terms $(2f_A + f_B)$, $(2f_A - f_B)$, $(f_A + 2f_B)$, and $(f_A - 2f_B)$ only.

1.6 DIGITAL INTERFACE

The ML2261 has two basic interface modes, RD and WR-RD, which are selected by the MODE input pin.

1.6.1 RD MODE

In the RD mode, the $\overline{WR}$/RDY pin is configured as the RDY output. The read mode performs a conversion with a single $\overline{RD}$ pulse. This allows the μP to start a conversion, wait, and then read data with a single read instruction.

The timing for the RD mode is shown in Figure 2. To do a conversion, $\overline{CS}$ must be low to select the device. After $\overline{CS}$ goes low, the RDY output goes low indicating that the device is ready to do a conversion. The conversion starts on the falling edge of $\overline{RD}$. While $\overline{RD}$ is low, the MSB and LSB decisions are made with internally generated clock edges. When the conversion is complete, RDY goes high and $\overline{INT}$ goes low signaling the end of the conversion. After $\overline{INT}$ goes low, the data outputs go from high impedance to active state with valid output data. Data stays valid until either $\overline{RD}$ or $\overline{CS}$ goes high. When either signal goes high, the output data lines return to the high impedance state and $\overline{INT}$ returns high. A pull up resistor on RDY in the sample and hold mode will cause clock injection, degrading the total unadjusted error, unless $\overline{CS}\downarrow$ is $\geq$ 20ns before $\overline{RD}\downarrow$.

1.6.2 WR-RD MODE

In the WR-RD mode, the $\overline{WR}$/RDY pin is configured as the $\overline{WR}$ input. In this mode, $\overline{WR}$ initiates the conversion and $\overline{RD}$ controls reading the output data. This can be done in several ways, described below.

1.6.3 WR-RD MODE — USING INTERNAL DELAY ($t_{RD} > t_{INTL}$)

The timing is shown in Figure 3. To do a conversion, $\overline{CS}$ must be low to select the device. Then, $\overline{WR}$ falling edge triggers the conversion. While $\overline{WR}$ is low, the MSB comparison is made. When $\overline{WR}$ returns high the LSB decision is made. After some internal delay, $\overline{INT}$ goes low indicating end of conversion. Valid data will appear on DB0–7 when $\overline{RD}$ is pulled low. $\overline{INT}$ is then reset by the rising edge of either $\overline{CS}$ or $\overline{RD}$.

1.6.4 WR-RD MODE — READING BEFORE DELAY ($t_{RD} < t_{INTL}$)

The internally generated delay for the LSB decision when $t_{RD} > t_{INTL}$ is longer than necessary due to circuit design tolerances of t_{INTL} delay. If desired, a faster conversion will result without loss of accuracy by bringing $\overline{RD}$ low within the minimum time specified for t_{RD}. The timing diagram for this mode is shown in Figure 4. $\overline{WR}$ is the same as when $t_{RD} > t_{INTL}$. But in this case, $\overline{RD}$ is brought low t_{RD} ns after $\overline{WR}$ rising edge and before INT. INT goes low indicating an end of conversion after the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. When $\overline{RD}$ is brought low before INT goes low the data bus always remains in the high-impedance state until INT↓.

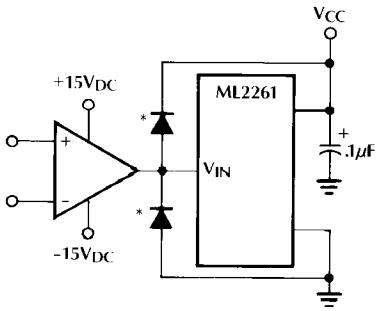
1.6.5 WR-RD MODE — STAND ALONE OPERATION

Stand alone operation can be implemented by tying $\overline{CS}$ and $\overline{RD}$ low as shown in Figure 5. $\overline{WR}$ initiates a conversion as before. When $\overline{WR}$ is low, the MSB comparison is made. When, $\overline{WR}$ goes high, the LSB comparison is made. Since $\overline{RD}$ is already low, the output data will appear automatically at end of conversion. Since $\overline{RD}$ is always low, INT is reset on rising edge of $\overline{WR}$ and goes low at end of conversion.

1.6.6 POWER-ON RESET

When power is first applied, an internal power-on reset and timer circuit inhibits the $\overline{CS}$ input and resets the internal circuitry to prevent the ML2261 from starting in an unknown state. During this period of approximately 3μs, INT remains high and the data bus is in the high-impedance state.

2.0 TYPICAL APPLICATIONS



* NO PROTECTION IS REQUIRED IF INPUT CURRENT < 25mA

Figure 10. Protecting the Input

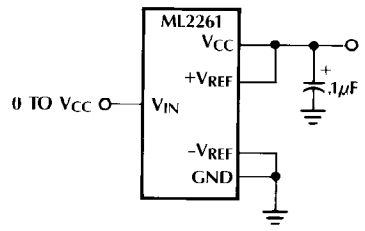


Figure 11. Using V_{CC} as Reference for Ratiometric Operation

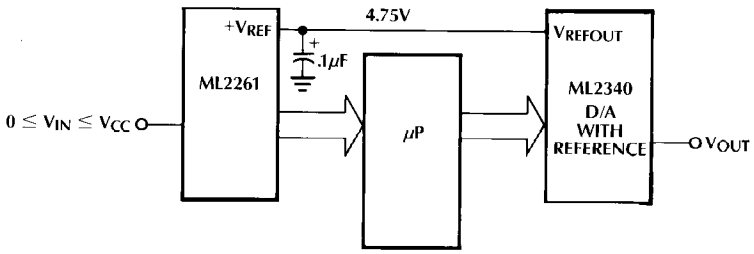


Figure 12. Using External Reference of D/A

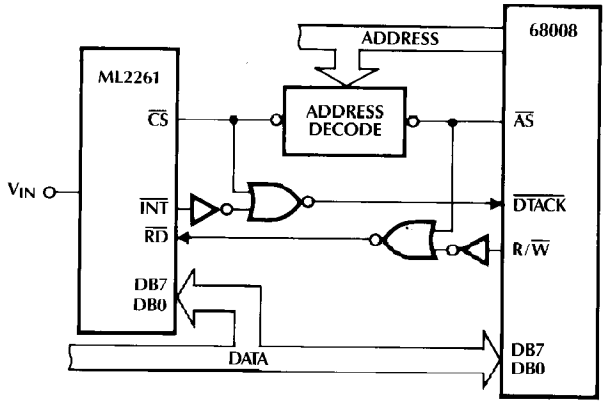


Figure 13. 68000 Type Interface to ML2261

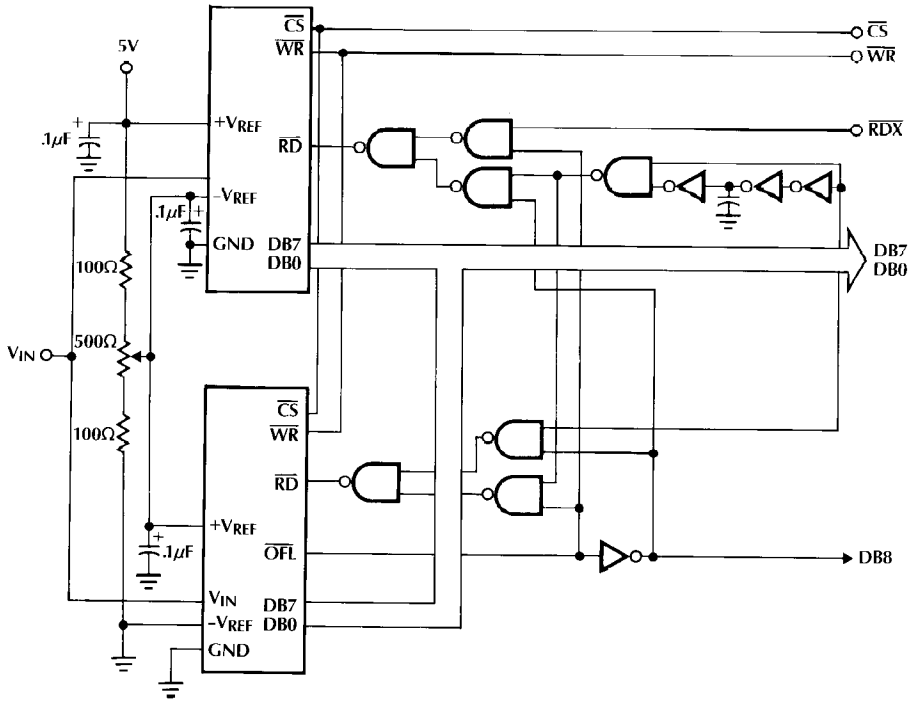


Figure 14. 9-Bit Resolution

2.0 TYPICAL APPLICATIONS (Continued)

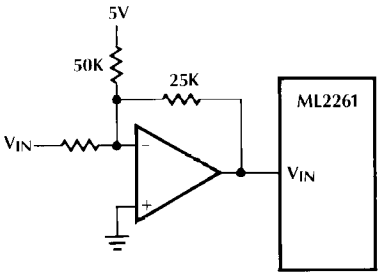


Figure 15. ±2.5V Analog Input Range

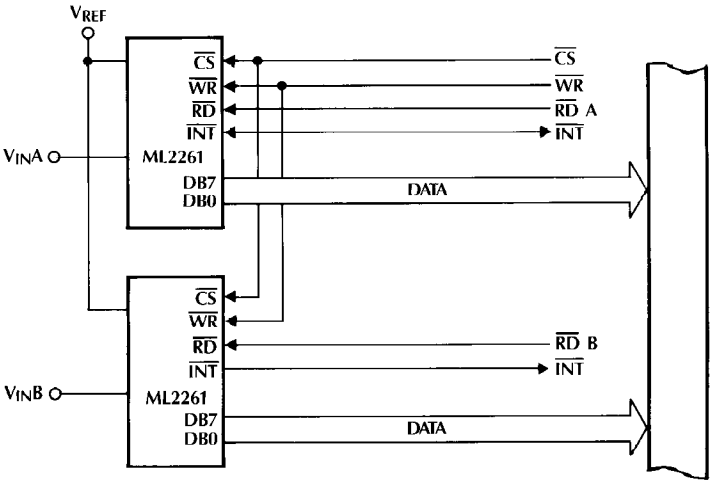


Figure 16. Simultaneous Sampling of Two Variables

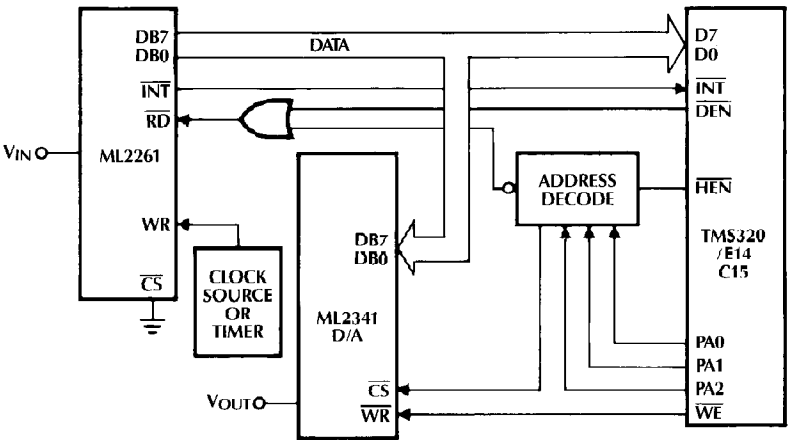


Figure 17. TMS320 Interface with D/A Output

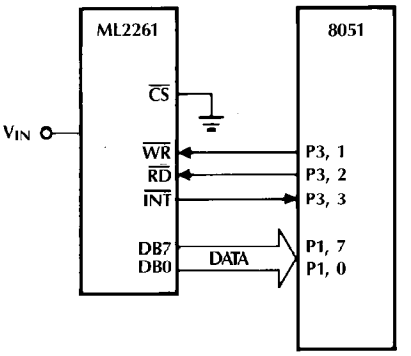


Figure 18. 8051 Interface to ML2261

TYPICAL APPLICATIONS (Continued)

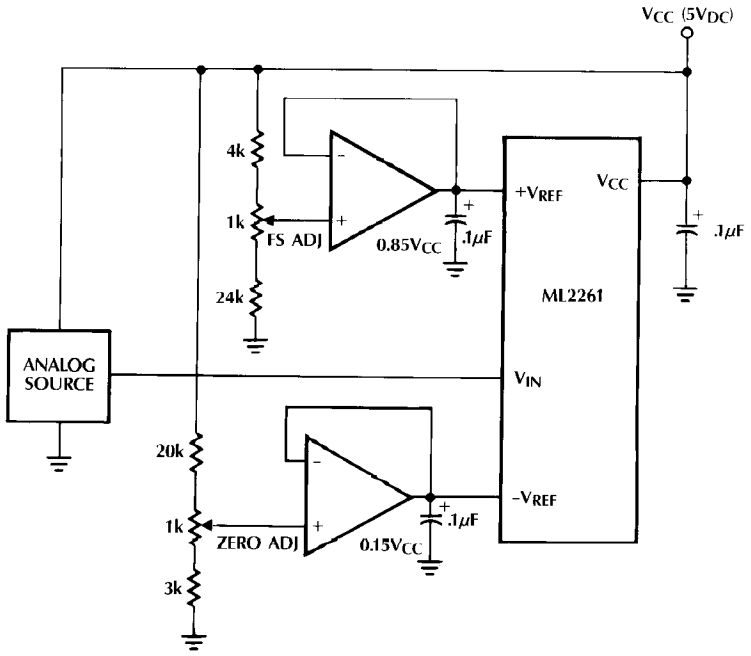


Figure 19. Operating with a Ratiometric Analog Signal of 15% of V_{CC} to 85% of V_{CC}

ORDERING INFORMATION

PART NUMBER	TOTAL UNADJUSTED ERROR	TEMPERATURE RANGE	PACKAGE
ML2261BCP	±1/2 LSB	0°C to 70°C	Molded DIP (P20) (Obsolete)
ML2261BCQ		0°C to 70°C	Molded PCC (Q20) (Obsolete)
ML2261CCP	±1 LSB	0°C to 70°C	Molded DIP (P20) (Obsolete)
ML2261CCQ		0°C to 70°C	Molded PCC (Q20) (End Of Life)