OKI Semiconductor   This version: Oct. 2001

ML9213

56-Bit Duplex/Triplex (1/2 duty/1/3 duty) VFD Controller/Driver with Anode Digital Dimming

GENERAL DESCRIPTION

The ML9213 is a full CMOS controller/driver for Duplex or Triplex (1/2 duty or 1/3 duty) vacuum fluorescent display tube. It consists of a 56-segment driver multiplexed to drive up to 168 segments, and 10-bit digital dimming circuit.

ML9213 features a selection of a master mode and a slave mode, and therefore it can be used to expand segments for the VFD driver with keyscan and A/D converter function.
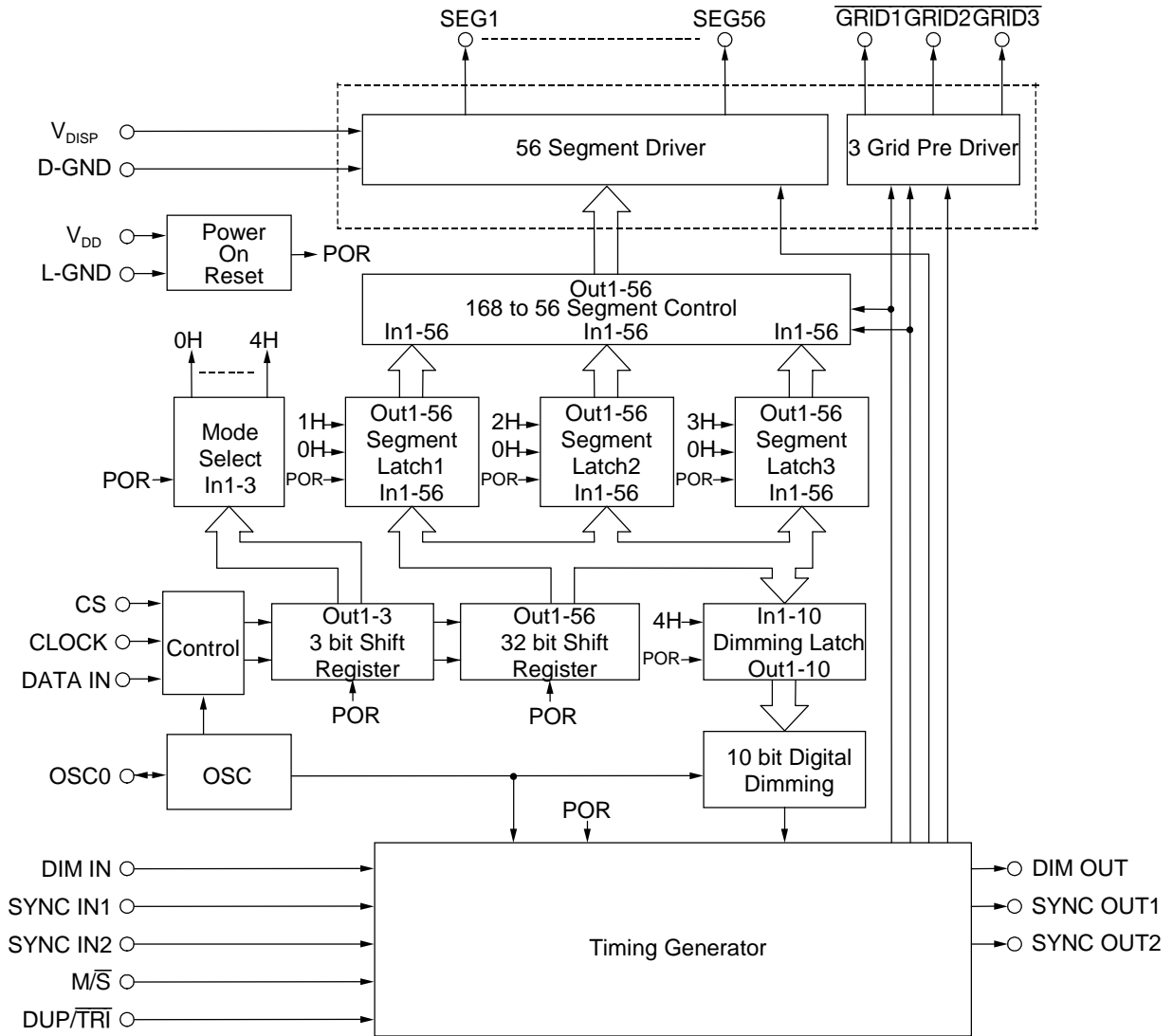
ML9213 provides an interface with a microcontroller only by three signal lines: DATA IN, CLOCK and CS.
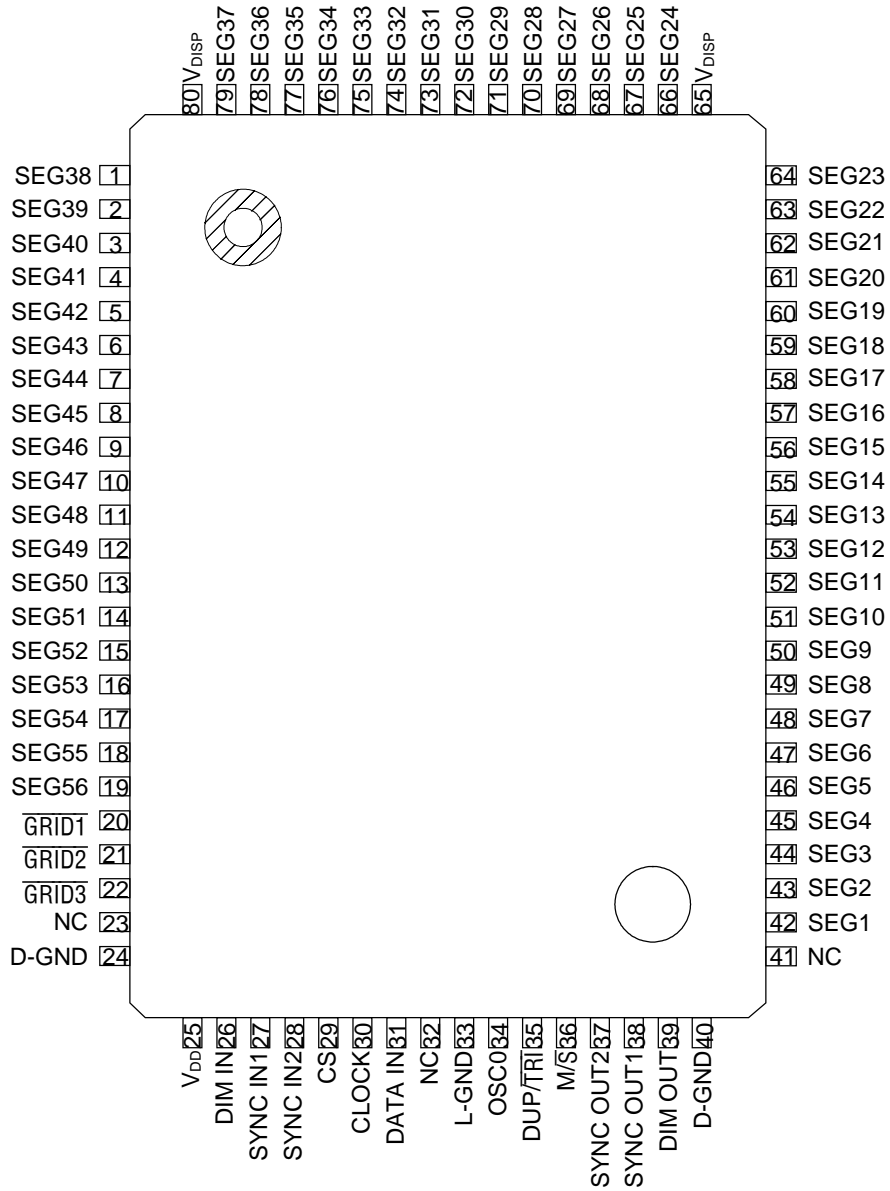
FEATURES

- Logic supply voltage (V_{DD})   : 5.0 V ±10%
- Driver supply voltage (V_{DISP})   : 8.0 to 18.0 V
- Duplex/Triplex (1/2 duty / 1/3 duty) selectable
  DUP/$\overline{TRI}$ = 1/2 duty selectable at "H" level
  DUP/$\overline{TRI}$ = 1/3 duty selectable at "L" level
- Number of display segments
  112 segments max. (during 1/2 duty mode)
  168 segments max. (during 1/3 duty mode)
- Master/Slave selectable
  M/$\overline{S}$ = "H" level   : Master mode
  M/$\overline{S}$ = "L" level   : Slave mode
- Interface with a microcontroller
  Three lines: CS, CLOCK, and DATA IN
- 56-segment driver outputs   : I_{OH} = –5.0 mA at V_{OH} = V_{DISP}–0.8 V (SEG1 to 37)
  (can be directly connected to VFD tube   : I_{OH} = –10.0 mA at V_{OH} = V_{DISP}–0.8 V (SEG38 to 56)
  and requires no external resistors)   : I_{OL} = 500 μA at V_{OL} = 2.0 V (SEG1 to 56)
- 3-grid pre-driver outputs   : I_{OH} = –5.0 mA at V_{OH} = V_{DISP}–0.8 V
  (requires external drivers) I_{OL} = 10.0 mA at V_{OL} = 2.0 V
- Logic outputs   : I_{OH} = –200 μA at V_{OH} = V_{DD}–0.8 V
          I_{OL} = 200 μA at V_{OL} = 0.8 V
- Built-in anode digital dimming circuit (10-bit resolution)
- Built-in oscillation circuit (external resistor and capacitor)
- Built-in Power-On-Reset circuit
- Package options:
  80-pin plastic QFP (QFP80-P-1420-0.80-BK)   Product name: ML9213GA
  80-pin plastic QFP (QFP80-P-1414-0.65-K)   Product name: ML9213GP

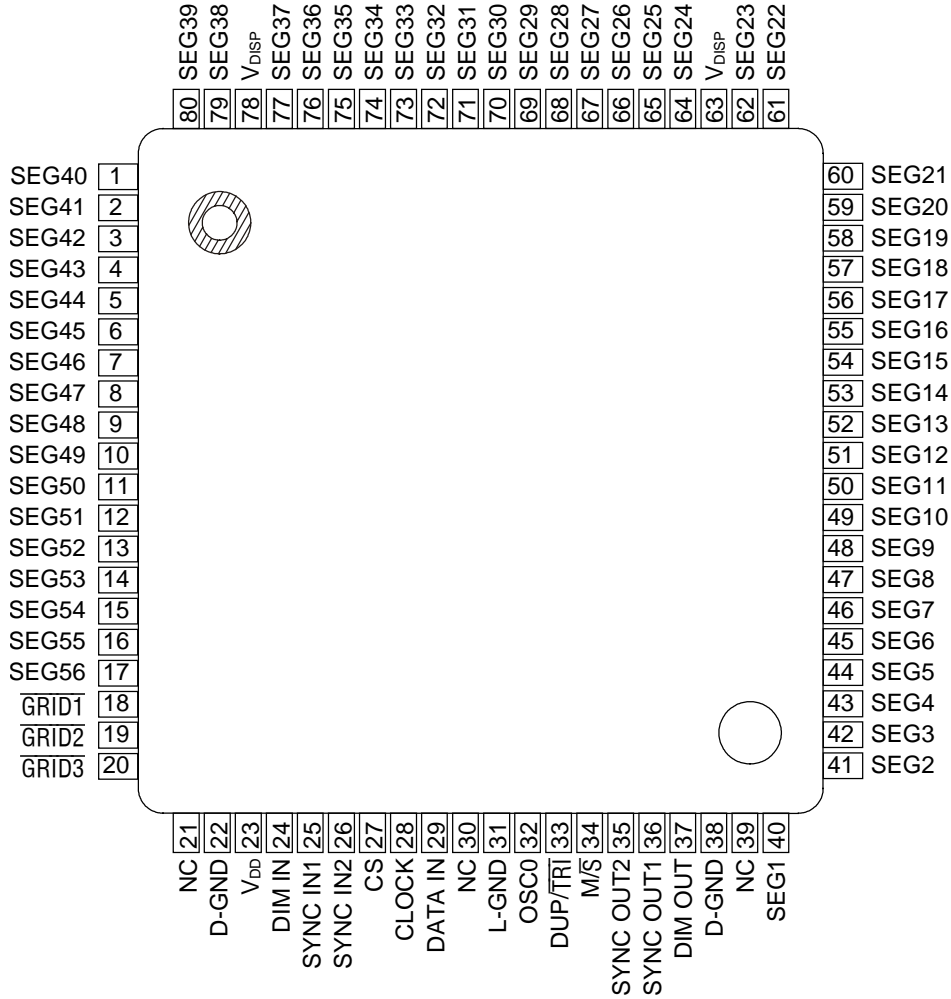**OKI** Semiconductor   **ML9213**

BLOCK DIAGRAM

OKI Semiconductor   **ML9213**

PIN CONFIGURATION (TOP VIEW)

Top pins (left to right, pins 80–65):
80 V_{DISP}, 79 SEG37, 78 SEG36, 77 SEG35, 76 SEG34, 75 SEG33, 74 SEG32, 73 SEG31, 72 SEG30, 71 SEG29, 70 SEG28, 69 SEG27, 68 SEG26, 67 SEG25, 66 SEG24, 65 V_{DISP}

Left pins (top to bottom, pins 1–24):
SEG38 1
SEG39 2
SEG40 3
SEG41 4
SEG42 5
SEG43 6
SEG44 7
SEG45 8
SEG46 9
SEG47 10
SEG48 11
SEG49 12
SEG50 13
SEG51 14
SEG52 15
SEG53 16
SEG54 17
SEG55 18
SEG56 19
$\overline{GRID1}$ 20
$\overline{GRID2}$ 21
$\overline{GRID3}$ 22
NC 23
D-GND 24

Right pins (top to bottom, pins 64–41):
64 SEG23
63 SEG22
62 SEG21
61 SEG20
60 SEG19
59 SEG18
58 SEG17
57 SEG16
56 SEG15
55 SEG14
54 SEG13
53 SEG12
52 SEG11
51 SEG10
50 SEG9
49 SEG8
48 SEG7
47 SEG6
46 SEG5
45 SEG4
44 SEG3
43 SEG2
42 SEG1
41 NC

Bottom pins (left to right, pins 25–40):
25 V_{DD}, 26 DIM IN, 27 SYNC IN1, 28 SYNC IN2, 29 CS, 30 CLOCK, 31 DATA IN, 32 NC, 33 L-GND, 34 OSC0, 35 DUP/$\overline{TRI}$, 36 M/$\overline{S}$, 37 SYNC OUT2, 38 SYNC OUT1, 39 DIM OUT, 40 D-GND

NC: No connection

ML9213GA
80-Pin Plastic QFP
(QFP80-P-1420-0.80-BK)

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Top pins (left to right, pins 80–61): SEG39, SEG38, V$_{DISP}$, SEG37, SEG36, SEG35, SEG34, SEG33, SEG32, SEG31, SEG30, SEG29, SEG28, SEG27, SEG26, SEG25, SEG24, V$_{DISP}$, SEG23, SEG22

Left pins (top to bottom, pins 1–20):

Pin	Name
1	SEG40
2	SEG41
3	SEG42
4	SEG43
5	SEG44
6	SEG45
7	SEG46
8	SEG47
9	SEG48
10	SEG49
11	SEG50
12	SEG51
13	SEG52
14	SEG53
15	SEG54
16	SEG55
17	SEG56
18	$\overline{GRID1}$
19	$\overline{GRID2}$
20	$\overline{GRID3}$

Right pins (top to bottom, pins 60–41):

Pin	Name
60	SEG21
59	SEG20
58	SEG19
57	SEG18
56	SEG17
55	SEG16
54	SEG15
53	SEG14
52	SEG13
51	SEG12
50	SEG11
49	SEG10
48	SEG9
47	SEG8
46	SEG7
45	SEG6
44	SEG5
43	SEG4
42	SEG3
41	SEG2

Bottom pins (left to right, pins 21–40): NC, D-GND, V$_{DD}$, DIM IN, SYNC IN1, SYNC IN2, CS, CLOCK, DATA IN, NC, L-GND, OSC0, DUP/$\overline{TRI}$, M/$\overline{S}$, SYNC OUT2, SYNC OUT1, DIM OUT, D-GND, NC, SEG1

NC: No connection

ML9213GP
80-Pin Plastic QFP
(QFP80-P-1414-0.65-K)

PIN DESCRIPTIONS

Symbol	Pin		Type	Description
	ML9213GA	ML9213GP		
V_{DISP}	65, 80	63, 78	—	Power supply pins for VFD driver circuit. These should be connected externally.
V_{DD}	25	23	—	Power supply pin for logic drive.
D-GND	24, 40	22, 38	—	D-GND is ground pin for the VFD driver circuit. L-GND is ground
L-GND	33	31	—	pin for the logic circuit. These should be connected externally.
SEG1 to 37	42 to 64, 66 to 79	40 to 62, 64 to 77	O	Segment (anode) signal output pins for a VFD tube. These pins can be directly connected to the VFD tube. External circuit is not required. $I_{OH} \leq -5$ mA
SEG38 to 56	1 to 19	79, 80, 1 to 17	O	Segment (anode) signal output pins for a VFD tube. These pins can be directly connected to the VFD tube. External circuit is not required. $I_{OH} \leq -10$ mA
$\overline{GRID1}$	20	18		Inverted Grid signal output pins. Since these pins are connected
$\overline{GRID2}$	21	19	O	to the pre-driver, an external circuit is required. $I_{OL} \leq 10$ mA
$\overline{GRID3}$	22	20		
CS	29	27	I	Chip select input pin. Data is not transferred when CS is set to a Low level.
CLOCK	30	28	I	Shift clock input pin. Serial data shifts at the rising edge of the CLOCK.
DATA IN	31	29	I	Serial data input pin (positive logic). Data is input to the shift register at the rising edge of the CLOCK signal.
DUP/$\overline{TRI}$	35	33	I	Duplex/Triplex operation select input pin. Duplex (1/2 duty) operation is selected when this pin is set to V_{DD}. Triplex (1/3 duty) operation is selected when this pin is set to L-GND.
M/$\overline{S}$	36	34	I	Master/Slave mode select input pin. Master mode is selected when this pin is set to V_{DD}. Slave mode is selected when this pin is set to L-GND.
DIM IN	26	24	I	Dimming pulse input. When the slave mode is selected, connect this pin to the master side DIM OUT pin. The pulse width of all the segment outputs is controlled by an input pulse width of DIM IN. When the master mode is selected, input to this pin is ignored; therefore, connect this pin to V_{DD} or L-GND. The pulse width of all the segment outputs is controlled by the built-in digital dimming circuit, and the pulse width of all the grid outputs is controlled by the internal timing generator.
SYNC IN1	27	25		Synchronous signal input. When the slave mode is selected, connect these pins to the master side SYN COUT1 and 2 pins.
SYNC IN2	28	26	I	When the master mode is selected, input to these pins is ignored; therefore, connect these pins to V_{DD} or L-GND.
DIM OUT	39	37	O	Dimming pulse output. Connect this pin to the slave side DIM IN pin.

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Symbol	Pin		Type	Description
	ML9213GA	ML9213GP		
SYNC OUT1	38	36	O	Synchronous signal output.
SYNC OUT2	37	35		Connect these pins to the slave side SYNC IN1 and 2 pins.
OSC0	34	32	I/O	RC oscillator connecting pins. Oscillation frequency depends on display tubes to be used. For details, refer to ELECTRICAL CHARACTERISTICS.
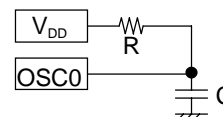
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rating	Unit
Driver Supply Voltage	V_{DISP}	—		−0.3 to +20	V
Logic Supply Voltage	V_{DD}	—		−0.3 to +6.5	V
Input Voltage	V_{IN}	—		−0.3 to V_{DD}+0.3	V
Power Dissipation	P_D	Ta≥25°C	QFP80-P-1420-0.80-BK	342	mW
			QFP80-P-1414-0.65-K	343	
Storage Temperature	T_{STG}	—		−55 to +150	°C
Output Current	I_{O1}	SEG1 to 37		−10.0 to +2.0	mA
	I_{O2}	SEG38 to 56		−20.0 to +2.0	mA
	I_{O3}	$\overline{GRID1}$ to $\overline{3}$		−10.0 to +20.0	mA
	I_{O4}	DIM OUT, SYNC OUT1, SYNC OUT2		−2.0 to +2.0	mA

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Driver Supply Voltage	V_{DISP}	—		8.0	13.0	18.0	V
Logic Supply Voltage	V_{DD}	—		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}	All inputs except OSC0		$0.8V_{DD}$	—	—	V
Low Level Input Voltage	V_{IL}	All inputs except OSC0		—	—	$0.2V_{DD}$	V
Clock Frequency	f_C	—		—	—	2.0	MHz
Oscillation Frequency	f_{OSC}	R = 10 kΩ ± 5%, C = 27 pF ± 5%		2.2	3.3	4.4	MHz
Frame Frequency	f_{FR}	R = 10 kΩ ± 5%, C = 27 pF ± 5%	1/3 Duty	179	269	358	Hz
			1/2 Duty	268	403	538	Hz
Operating Temperature	T_{OP}	—		−40	—	+105	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

Ta = −40 to +105°C, V_{DISP} = 8.0 to 18.0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	*1)	—		$0.8V_{DD}$	—	V
Low Level Input Voltage	V_{IL}	*1)	—		—	$0.2V_{DD}$	V
High Level Input Current	I_{IH}	*1)	$V_{IH} = V_{DD}$		−1.0	+1.0	μA
Low Level Input Current	I_{IL}	*1)	V_{IL} = GND		−1.0	+1.0	μA
High Level Output Voltage	V_{OH1}	SEG1-37	V_{DISP} = 9.5 V	I_{OH1} = −5 mA	V_{DISP}−0.8	—	V
	V_{OH2}	SEG38-56		I_{OH2} = −10 mA	V_{DISP}−0.8	—	V
	V_{OH3}	$\overline{GRID1\text{-}3}$		I_{OH3} = −5 mA	V_{DISP}−0.8	—	V
	V_{OH4}	*2)	V_{DD} = 4.5V	I_{OH4} = −200 μA	V_{DD}−0.8	—	V
Low Level Output Voltage	V_{OL1}	SEG1-37	V_{DISP} = 9.5 V	I_{OL1} = 500 μA	—	2.0	V
	V_{OL2}	SEG38-56		I_{OL2} = 500 μA	—	2.0	V
	V_{OL3}	$\overline{GRID1\text{-}3}$		I_{OL3} = 10 mA	—	2.0	V
	V_{OL4}	*2)	V_{DD} = 4.5 V	I_{OL4} = 200 μA	—	0.8	V
Supply Current	I_{DISP}	V_{DISP}	R=10 kΩ ±5%,C=27 pF ±5%,		—	100	μA
	I_{DD}	V_{DD}	no load		—	5.0	mA

*1) CS, CLOCK, DATA IN, DIM IN, SYNC IN1, SYNC IN2, M/$\overline{S}$, DUP/$\overline{TRI}$

*2) DIM OUT, SYNC OUT1, SYNC OUT2

AC Characteristics

Ta = −40 to +105°C, V_{DISP} = 8.0 to 18.0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Condition		Min.	Max.	Unit
Clock Frequency	f_C	—		—	2.0	MHz
Clock Pulse Width	t_{CW}	—		200	—	ns
Data Setup Time	t_{DS}	—		200	—	ns
Data Hold Time	t_{DH}	—		200	—	ns
CS Off Time	t_{CSL}	—		20	—	μs
CS Setup Time (CS–Clock)	t_{CSS}	—		200	—	ns
CS Hold Time (Clock–CS)	t_{CSH}	—		200	—	ns
CS Wait Time	t_{RSOFF}	—		400	—	μs
Output Slew Rate Time	t_R	C_L = 100 pF	t_R = 20% to 80%	—	2.0	μs
	t_F		t_F = 80% to 20%	—	2.0	μs
V_{DD} Rise Time	t_{PRZ}	Mounted in a unit		—	100	μs
V_{DD} Off Time	t_{POF}	Mounted in a unit, V_{DD} = 0.0 V		5.0	—	ms

TIIMING DIAGRAM

● **Data Input Timing**
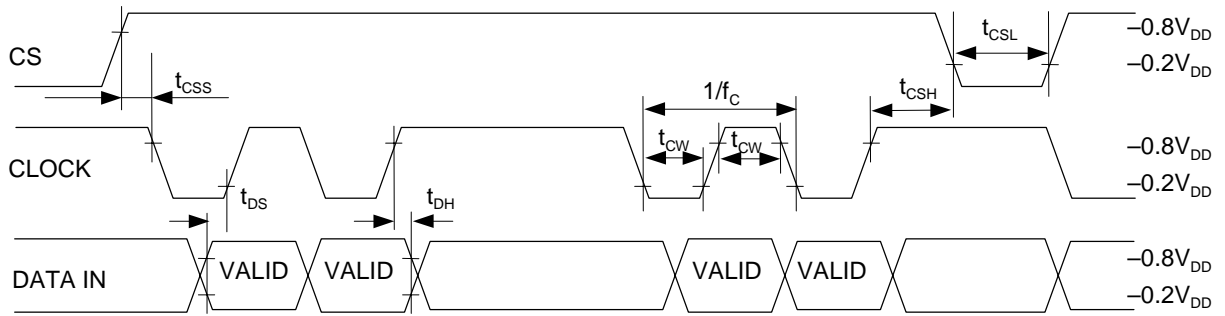
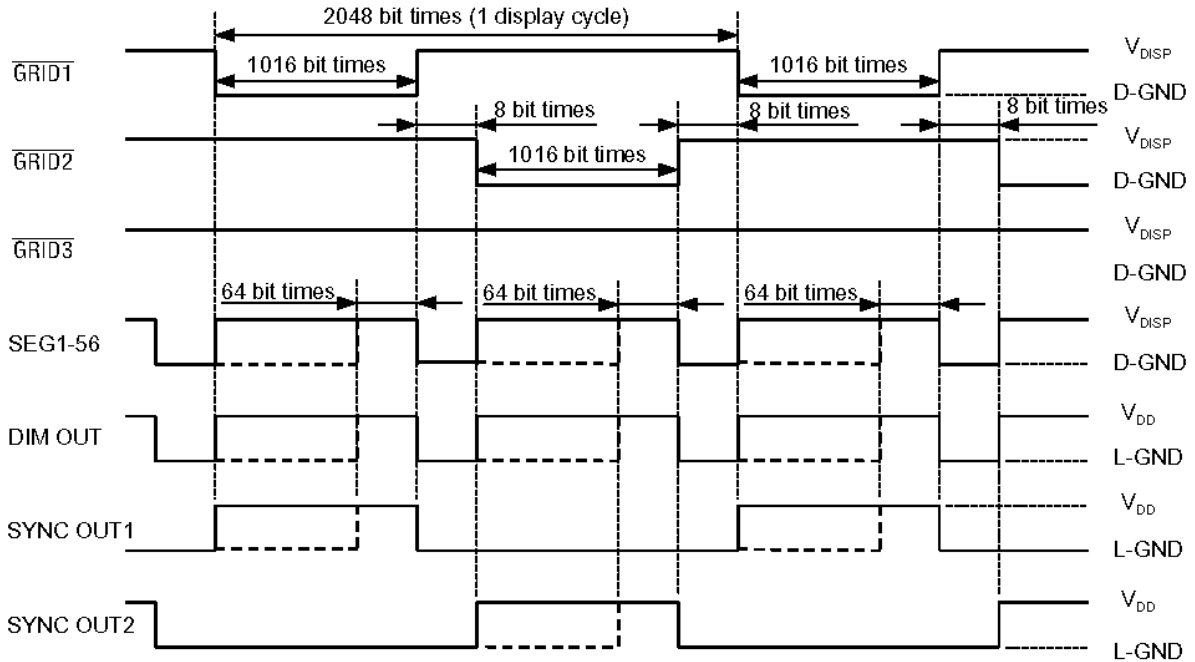● **Reset Timing**
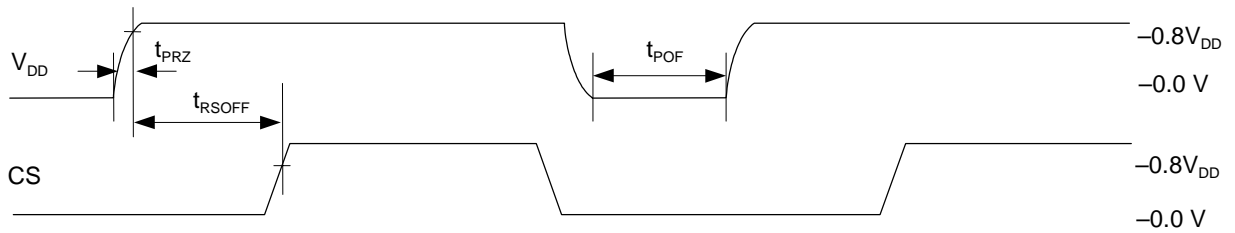
● **Driver Output Timing**

● **Output Timing (Duplex Operation)**   *1 bit time = 4/f_{OSC}
   Solid line: Indicates that the anode dimming data is 1016/1024 in the master mode.
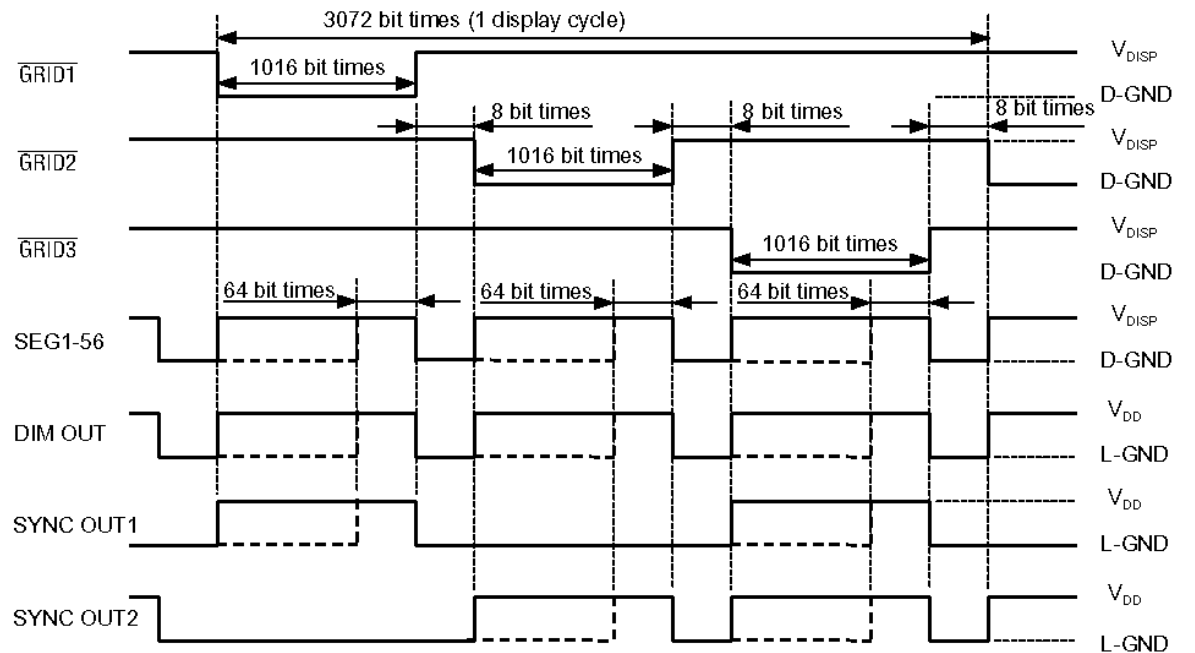   Chain line: Indicates that the anode dimming data is 64/1024 in the master mode.

● **Output Timing (Triplex Operation)**   *1 bit time = 4/f_{OSC}
   Solid line: Indicates that the anode dimming data is 1016/1024 in the master mode.
   Chain line: Indicates that the anode dimming data is 64/1024 in the master mode.

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FUNCTIONAL DESCRIPTION

Power-on Reset
When power is turned on, the ML9213 is initialized by the internal power-on reset circuit.
The status of the internal circuit after initialization is as follows:
- The contents of the shift registers and latches are set to "0".
- The anode dimming duty cycle is set to "0".
- All segment outputs (SEG1 to 56) are set to Low level.
- The $\overline{GRID1}$ output is set to Low level.
- The $\overline{GRID2}$ and $\overline{GRID3}$ outputs are set to High level.

Data Transfer Method
Data can be transferred between the rising edge and the next falling edge of chip select input.
The mode data, segment data and anode dimming data are written by a serial transfer method. The serial data is input to the shift register at the rising edge of a shift clock pulse.
The mode data (M0 to M2) must be transferred after the segment data and anode dimming data succeedingly.
When the chip select input falls, an internal LOAD signal is automatically generated and data is loaded to the latches.
Set the shift clock to a High level except during data transfer.
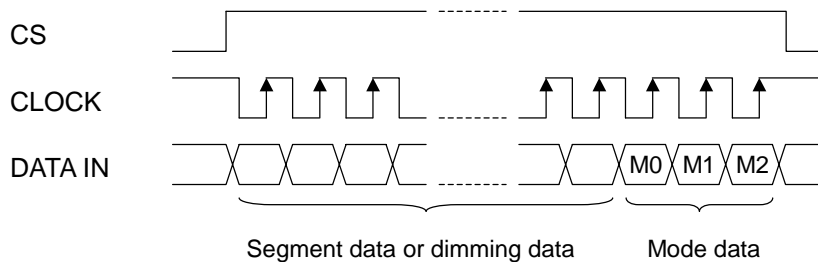
Function Mode
Function mode is selected by the mode data (M0 to M2). The relation between function mode and mode data is as follows:

FUNCTION MODE	OPERATING MODE	MODE DATA		
		M0	M1	M2
0	Segment Data for $\overline{GRID1\text{-}3}$ Input	0	0	0
1	Segment Data for $\overline{GRID1}$ Input	1	0	0
2	Segment Data for $\overline{GRID2}$ Input	0	1	0
3	Segment Data for $\overline{GRID3}$ Input	1	1	0
4	Digital Dimming Data Input	0	0	1

OKI Semiconductor **ML9213**

Segment Data Input [Function Mode: 0 to 3]

- ML9213 receives the segment data when function mode 0 to 3 are selected.
- The same segment data is transferred to the 3 segment data latches corresponding to $\overline{GRID1}$ to $\overline{3}$ at the same time when the function mode 0 is selected.
- The segment data is transferred to only one segment data latch corresponding to the specified GRID when the function mode is 1, 2 or 3 is selected.
- Segment output (SEG1 to 56) becomes High level (lighting) when the segment data (S1 to S56) is set to "1".

[Data Format]
    Input Data   : 59 bits
    Segment Data: 56 bits
    Mode Data   :   3 bits

Bit	1	2	3	4	……….	53	54	55	56	57	58	59
Input Data	S1	S2	S3	S4	……….	S53	S54	S55	S56	M0	M1	M2

← ——————————— Segment Data (56 bits) ——————————— → ← Mode Data → (3 bits)

[Bit correspondence between segment output and segment data]

Segment output	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Segment data	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
Segment output	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Segment data	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31	S32
Segment output	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
Segment data	S33	S34	S35	S36	S37	S38	S39	S40	S41	S42	S43	S44	S45	S46	S47	S48
Segment output	49	50	51	52	53	54	55	56	---	---	---	---	---	---	---	---
Segment data	S49	S50	S51	S52	S53	S54	S55	S56	---	---	---	---	---	---	---	---

Anode Dimming Data Input [Function Mode: 4]

- ML9213 receives the anode dimming data when function mode 4 is selected.
- The output duty changes in the range of 0/1024 (0%) to 1016/1024 (99.2%) for each grid.
- The 10-bit anode dimming data is input from LSB.

[Data Format]

Input Data	:	13 bits
Anode Dimming Data	:	10 bits
Mode Data	:	3 bits

Bit	1	2	3	4	5	6	7	8	9	10	11	12	13
Input Data	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	M0	M1	M2

LSB ← Digital Dimming Data (10bits) → MSB   ← Mode Data (3bits) →

(LSB)				Dimming Data					(MSB)	Duty Cycle
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	
0	0	0	0	0	0	0	0	0	0	0/1024
1	0	0	0	0	0	0	0	0	0	1/1024
1	1	1	0	1	1	1	1	1	1	1015/1024
0	0	0	1	1	1	1	1	1	1	1016/1024
1	0	0	1	1	1	1	1	1	1	1016/1024
1	1	1	1	1	1	1	1	1	1	1016/1024

Master Mode

Master Mode is selected when M/$\overline{\text{S}}$ pin is set at High level. The master mode operation is as follows:

- Input to DIM IN, SYNC IN1 and SYNC IN2 is ignored, and these pins should be connected to L-GND or V_{DD}.
- The pulse width of SEG1 to SEG56 is controlled by the internal digital dimming circuit.
- The segment data corresponding to $\overline{\text{GRID1}}$ to $\overline{3}$ is selected by the internal timing generator.

Slave Mode

Slave Mode is selected when M/$\overline{S}$ pin is set at Low level. The slave mode operation is as follows:

- Output from internal anode dimming circuit is ignored. Connect the DIM IN, SYNC IN1 and SYNC IN2 pins to the master side DIM OUT, SYNC OUT1 and SYNC OUT2 pins respectively.
- The pulse width of SEG1 to 56 is controlled by the pulse width of DIM IN signal.
- The segment data corresponding to $\overline{GRID1}$ to $\overline{3}$ is selected by combinations of the SYNC IN1 and SYNC IN2 signals.
- The output levels of $\overline{GRID1}$ to $\overline{3}$ are set at High level. The output levels of DIM OUT, SYNC OUT1 and SYNC OUT2 are set at Low level.

[Correspondence between SYNC IN1, 2 and $\overline{GRID1}$ to $\overline{3}$]   [Correspondence between DIM IN and SEG1 to 56]

SYNC IN 1	SYNC IN 2	Segment Latch	GRID
0	0	No	No
1	0	Latch1	$\overline{GRID1}$
0	1	Latch2	$\overline{GRID2}$
1	1	Latch3	$\overline{GRID3}$

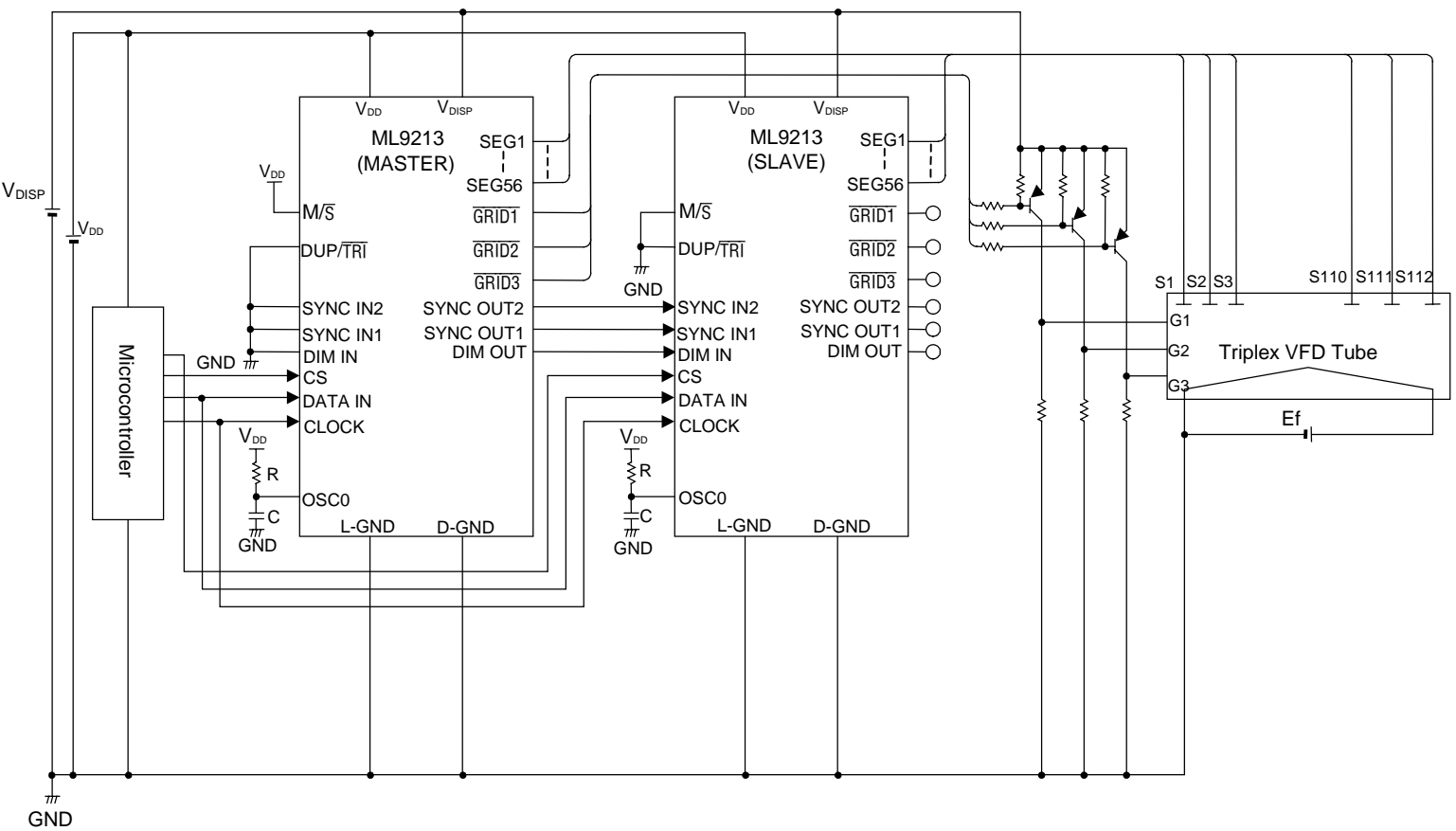| DIM IN	SEG1 to 56
0	Low
1	High

Note: Low: Lights OFF

High: Lights ON

APPLICATION CIRCUITS

1. Circuit for the duplex VFD tube (2-Grid × 112-Anode)
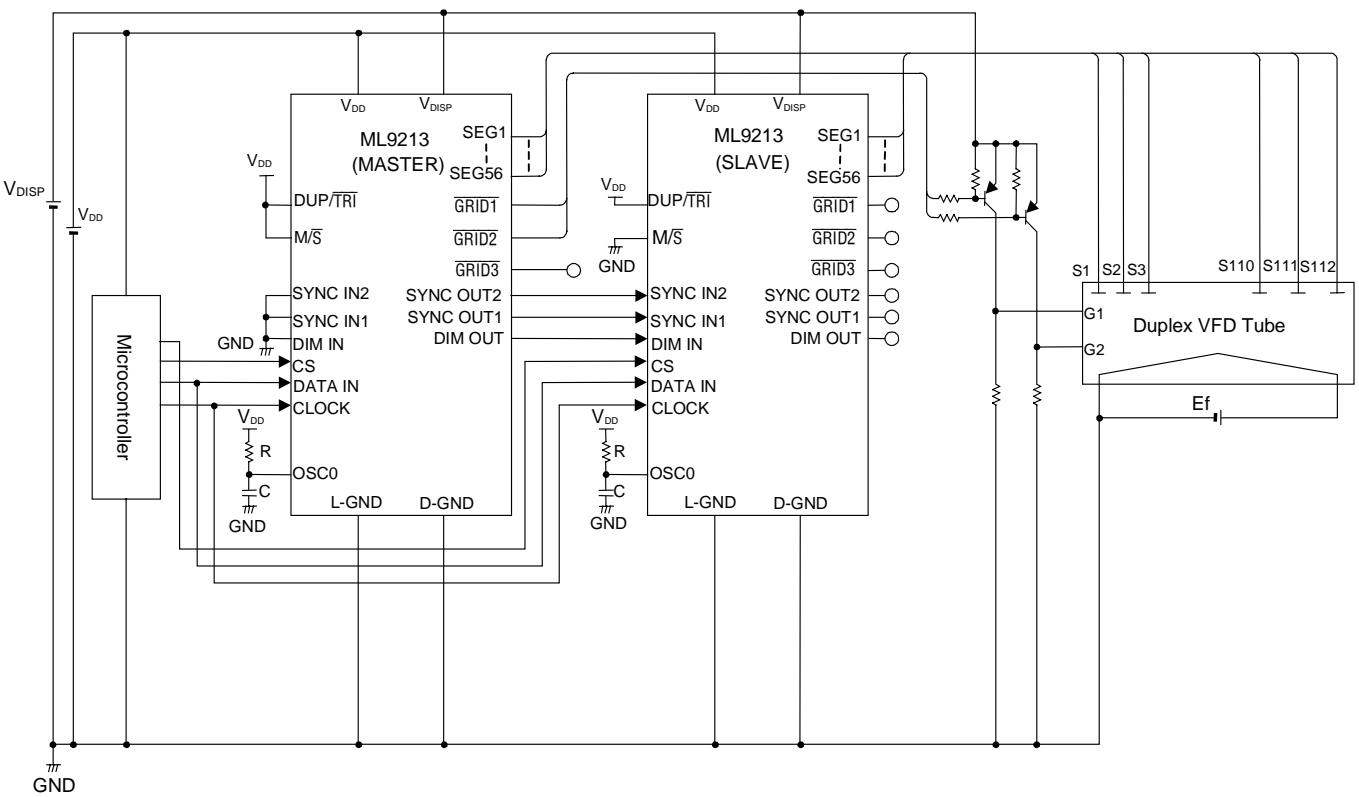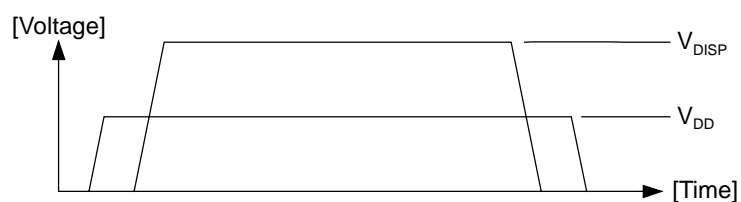
2. Circuit for the triplex VFD tube (3-Grid × 112-Anode)

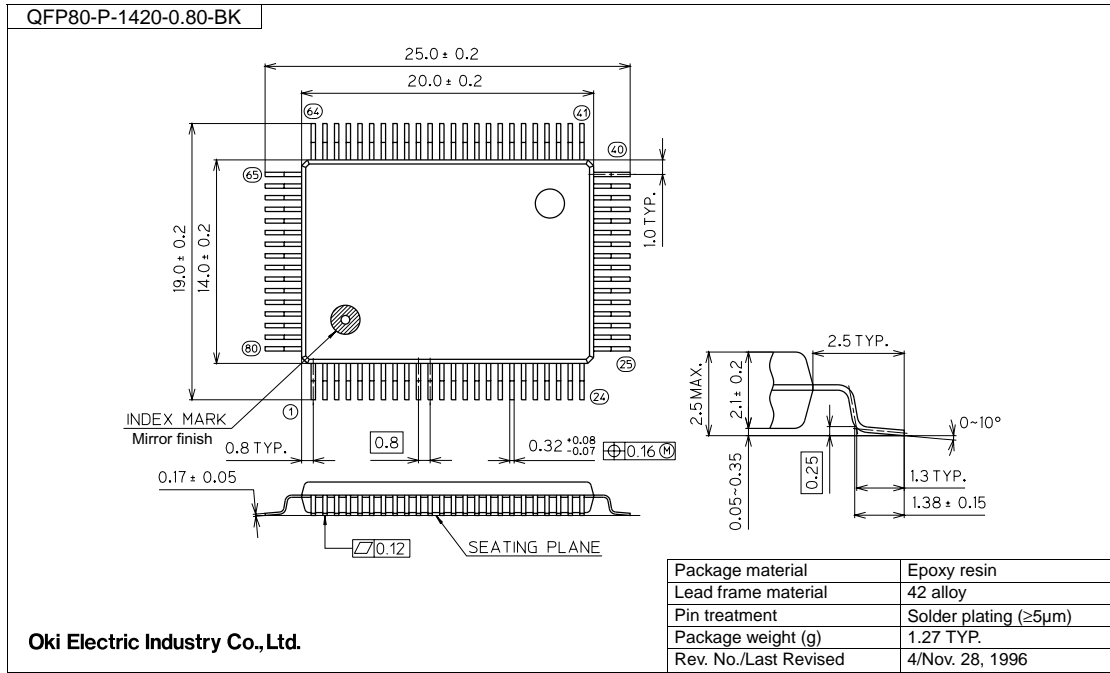**NOTES ON TURNING POWER ON/OFF**

- Connect L-GND and D-GND externally to be an equal potential voltage.
- To avoid wrong operations, turn on the driver power supply after turning on the logic power supply. Conversely, turn off the logic power supply after turning off the driver power supply.
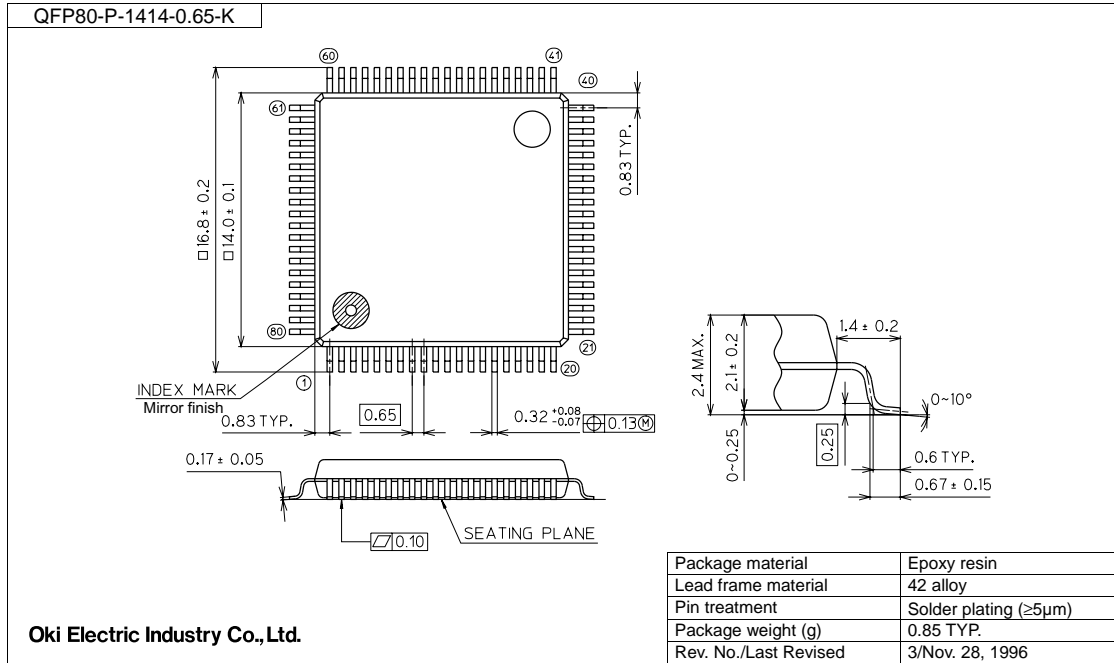
PACKAGE DIMENSIONS

(Unit: mm)

QFP80-P-1420-0.80-BK

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	1.27 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co.,Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)

Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.85 TYP.
Rev. No./Last Revised	3/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

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NOTICE
1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

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