MN12861

CMOS 1-chip Peripheral LSI for 16-bit MPU

■ Outline

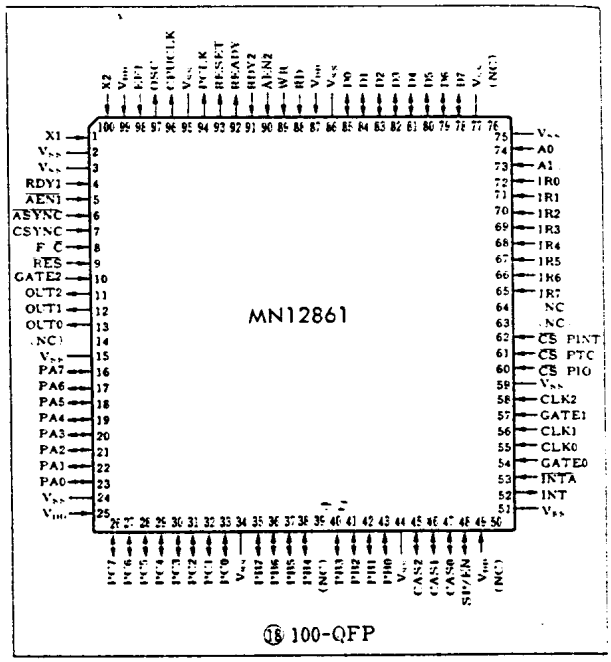
The MN12861 is a multifunctional peripheral LSI which can interface with Intel 16-and 8-bit microprocessors(MPUs).It is a CMOS 1-chip LSI which integrates functions such as clock generation,timer/counter,general purpose I/O,interrupt control,etc.on a single chip.

A combination of the MN12861 and MPU enables the most compact and advanced microcomputer system configuration.

■ Features

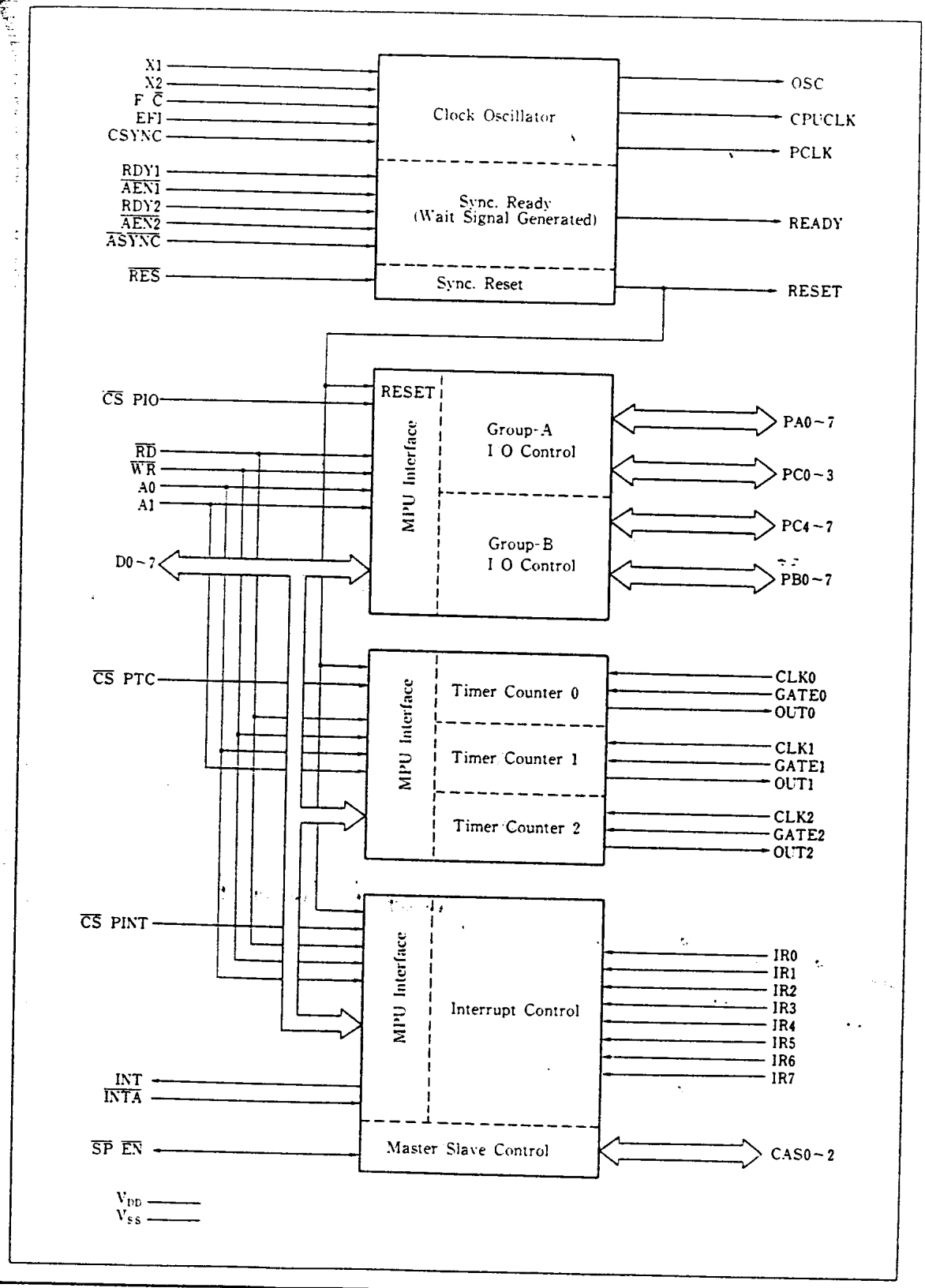
- 4 functions integrated on 1 chip
  1)Clock generator
  2)Programmable timer/counter
  3)Programmable I/O
  4)Programmable interrupt control
  Each function is compatible with Intel 8-bit/16-bit peripheral device. Terminals of each function block are all separately provided for wide general purpose properties.
  (Bus line and control line from the MPU are common)
- 5 V single power,TTL compatible I/O
- Low power consumption due to CMOS process
- 100-pin flat package
- Target MPUs
  - Intel 8086/88,8085A or their equivalents
  - Zailog Z-80 or its equivalents
  - The 8086/88 can be interfaced up to an 8 MHz version.

■ Pin Configuration



⑱ 100-QFP

■ Block Diagram



■ Pin Descriptions

Pin No.	Name	I/O	Description
85 84 83 82 81 80 79 78	D0 D1 D2 D3 D4 D5 D6 D7	I/O I/O I/O I/O I/O I/O I/O I/O	Interface pin related to CPU data. Used for reading and writing register, counter, etc. in each function block. It also serves as a vector address interrupt read pin from the CPU. It becomes an output pin at read time and as an input pin at write time.
74 73	A0 A1	I I	Specifies the addresses of the register, counter, latch and port in each function block which is read/written form the CPU.
89	$\overline{WR}$	I	Low-level Active control signal which writes data from the CPU to the MN12861. Data is written at a pulse rise edge. When a write/read control signal($\overline{RD}$, $\overline{INTA}$) is set to the High level together with this signal, D0-D7 are fixed at high impedance.
88	$\overline{RD}$	I	Low-level Active control signal which reads data from the MN12861 to the CPU. When a read control signal($\overline{WR}$, $\overline{INTA}$) is set to the High level together with this signal, D0-D7 are fixed at high impedance.
61	$\overline{CSPTC}$	I	When this pin is set to the Low level, either read signal($\overline{RD}$) or write signal($\overline{WR}$) becomes valid and it is enabled to read/write data from the CPU to the timer/counter of the MN12861.
60	$\overline{CSPIO}$	I	When this pin is set to the Low level, either read signal($\overline{RD}$) or write signal($\overline{WR}$) become valid and it is enabled to read/write data from the CPU to the I/O of the MN12861.
62	$\overline{CSPINT}$	I	When this pin is set to the Low level, either($\overline{RD}$) or write($\overline{WR}$) signal becomes valid, and it is enabled to read/write data from the CPU to the interrupt controller of the MN12861.
1 100	X1 X2	I I	Connects to a self-oscillating crystal oscillator and generates oscilations at a frequency 3 times higher than the CPUCLK signal. Used with the F/C pin set to the Low level.
4 91	RDY1 RDY2	I I	Informs the CPU that the device on the system bus completed reception or is ready to send. Valid when $\overline{AEN1}$=0 with RDY1=1, or $\overline{AEN2}$=0 with RDY2=1, and outputs "1" to the READY pin.
5 90	$\overline{AEN1}$ $\overline{AEN2}$	I I	$\overline{AEN1}$ validates RDY1, and $\overline{AEN2}$ RDY2, respectively; both Low-level Active signals.
6	$\overline{ASYNC}$	I	Selects a RDY signal synchronizing method when either RDY1 or RDY2 is made valid. At the Low level, the READY signal is outputted after 2-time synchronization. When set to the High level or opened, the READY signal is outputted after 1-time synchronization.

■ Pin Descriptions(Continued)

Pin No.	Name	I/O	Description
7	CSYNC	I	Synchronizing signal to output in-phase clocks as other clock generators of the MN12861 or the Intel 8284A. An internal counter is reset at the High level. When set to the Low level, the internal counter starts counting. CSYNC is externally synchronized with EFI input. Fix at GND when using internal self-oscillation.
8	F/C	I	Selects a CPUCLK, PCLK clock source. A crystal oscillation clock is selected as a source when set to the Low level, and EFI input clock when set to the High level. At the High level, self-oscillation stops.
9	RES	I	Input pin for RESET signal generation. It combines with an in-chip I/O reset signal. It is a Schmidt trigger level input pin. Once the reset signal is inputted from the RES pin, the CAS0-CAS2 pins remain at high impedance until a mode is set for the interrupt controller.
98	EFI	I	When the F/C input pin is set to the High level, EFI input becomes a clock source for CPUCLK and PCLK.
97	OSC	O	Self-oscillation output with the same frequency as an oscillation one. This pin is not affected if CSYNC is set to the High level.
96	CPUCLK	O	System clock supplied to the CPU or its local bus device. Outputs a high-level clock(duty 1/3) of 1/3-divided crystal oscillation frequency or EFI input clock frequency.
94	PCLK	O	Clock signal for a peripheral device. Outputs a 1/2 duty clock of 1/2-divided CPUCLK clock frequncy.
93	PESET	O	CPU reset signal which also serves as a in-chip I/O reset signal. If $\overline{\text{RES}}$ input is set to the Low level, the RESET signal is synchronized with the High level to be outputted. If reset is made valid from the I/O, all the I/O pins of PA, PB and PC are fixed at the Mode 0 input state. The control register in the I/O section is also cleared.
92	READY	O	RDY1/RDY2 synchronized signal and Hign-level Active. This pin is set to the High level if either one of input signals RDY1 and RDY2 becomes active.
55 56 58	CLK0 CLK1 CLK2	I I I	Clock input signals to relevant timers/counters. Down-counting starts at a fall of CLK input if a count number is set.
13 12 11	OUT0 OUT1 OUT2	O O O	Outputs from relevant timers/counters. Output waveforms of specified modes are outputted synchronously with respective CLK signals. Also available as interrupt signals to the CPU.

■ Pin Descriptions(Continued)

<table>
<tr><th>Pin No.</th><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>54
57
10</td><td>GATE0
GATE1
GATE2</td><td>I
I
I</td><td>Starts,stops and resets counting in accordance with a relevant timer counter set mode.</td></tr>
<tr><td>23
22
21
20
19
18
17
16</td><td>PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7</td><td>I/O
I/O
I/O
I/O
I/O
I/O
I/O
I/O</td><td>Serves as an input port, output port or bidirectional port depending on mode setting. Input or output is controlled by Port C relevant bits in the Mode 1 or 2.
<table>
<tr><th></th><th>Input</th><th>Output</th></tr>
<tr><td>Mode 0</td><td>Buffer input</td><td>Latch output</td></tr>
<tr><td>Mode 1</td><td>Latch inut</td><td>Latch output</td></tr>
<tr><td>Mode 2</td><td colspan="2">Latch I/O</td></tr>
</table></td></tr>
<tr><td>43
42
41
40
38
37
36
35</td><td>PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7</td><td>I/O
I/O
I/O
I/O
I/O
I/O
I/O
I/O</td><td>Serves as an input port or output port depending on mode setting. Input or output is cotrolled by Port C relevant bits in the Mode 1. The port B does not have the Mode 2.
<table>
<tr><th></th><th>Input</th><th>Output</th></tr>
<tr><td>Mode 0</td><td>Buffer input</td><td>Latch output</td></tr>
<tr><td>Mode 1</td><td>Latch input</td><td>Latch output</td></tr>
</table></td></tr>
<tr><td>33
32
31
30</td><td>PC0
PC1
PC2
PC3</td><td>I/O
I/O
I/O
I/O</td><td>Lower 4 bits of the port C. Serves as a 4-bit input or output port depending on mode setting of Gorup B including the Port B. In the Mode 1, PC0-PC2 are I/O control bits of the Port B, and remaining PC3 depends on Mode setting of Group A including the Port A. When Group A is in the Mode 1 or 2, PC3 becomes an interrupt output signal concerned with the Port A.
<table>
<tr><th>Mode
Port</th><th colspan="3">Group B</th></tr>
<tr><td></td><td colspan="2">Mode 0</td><td>Mode 1</td></tr>
<tr><td>PC0</td><td colspan="2">I/O</td><td>INTRB/INTRB</td></tr>
<tr><td>PC1</td><td colspan="2">I/O</td><td>IBFB/$\overline{\text{OBFB}}$</td></tr>
<tr><td>PC2</td><td colspan="2">I/O</td><td>$\overline{\text{STBB}}$/$\overline{\text{ACKB}}$</td></tr>
<tr><td>PC3</td><td>I/O</td><td>INTRA</td><td>I/O</td></tr>
<tr><td></td><td>Mode 0</td><td>Mode 1/2</td><td>Mode 0</td></tr>
<tr><td></td><td colspan="3">Group A</td></tr>
</table></td></tr>
<tr><td>29
28
27
26</td><td>PC4
PC5
PC6
PC7</td><td>I/O
I/O
I/O
I/O</td><td>Upper 4 bits of the Port C. Serves as a 4-bit input or output port depending on mode setting of Group A including the Port A. In case of Mode-1 input, PC3-PC5 serve as Port A input pins. In Mode-1 output, PC3, PC6 and PC7 serve as Port A output control pins.
<table>
<tr><th>Mode
Port</th><th colspan="3">Group A</th></tr>
<tr><td></td><td>Mode 0</td><td>Mode 1</td><td>Mode 2</td></tr>
<tr><td>PC4</td><td>I/O</td><td>$\overline{\text{STBA}}$/I/O</td><td>$\overline{\text{STBA}}$</td></tr>
<tr><td>PC5</td><td>I/O</td><td>IBFA/I/O</td><td>IBFA</td></tr>
<tr><td>PC6</td><td>I/O</td><td>I/O/$\overline{\text{ACKA}}$</td><td>$\overline{\text{ACKA}}$</td></tr>
<tr><td>PC7</td><td>I/O</td><td>I/O/$\overline{\text{OBFA}}$</td><td>$\overline{\text{OBFA}}$</td></tr>
</table></td></tr>
</table>

■ Pin Descriptions(Continued)

Pin No.	Name	I/O	Description
72 71 70 69 68 67 66 65	IR0 IR1 IR2 IR3 IR4 IR5 IR6 IR7	I I I I I I I I	Async. interrupt request signal to the interrupt controller. It is received differently depending on mode setting. The interrupt controller requests the CPU for an interrupt when IR input is changed from L to H(_┌) in the edge trigger mode, and when IR input is at the High level in the level trigger mode. At that time, IR input must keep the High level at least until a fall of an initial $\overline{\text{INTA}}$ pulse, in order to ensure complete interrupt operation.
53	INTA	I	Read signal outputted in a CPU interrupt processing sequence in order to read an interrupt vector.
52	INT	O	Interrupt request signal outputted to the CPU when IR input to the interrupt controller is received. High level. Active.
48	$\overline{\text{SP}}/\overline{\text{EN}}$	I/O	Low-level Active pin which serves as input or output depending on mode setting. Serves as an output pin in the buffer mode. A control pulse is outputted in order to enable the buffer transceiver. Serves as an input pin in the non-buffer mode and allows setting High level=Master/Low level=Slave. Interrupt input can be extended by externally attaching the Intel 8259A to the MN12861.
47 46 45	CAS0 CAS1 CAS2	I/O I/O I/O	Used in the master, slave mode which is used with 1 to 8 Intel 8259As externally attached. 3-bit signal lines to specify individual device addresses and serve as both input and output. When the MN12861 is in the master mode, they become output to the external 8259A, and when in the slave mode, they become input. When the system requires only one MN12861 interrupt controller regardless of the master/slave mode, they become high impedance by mode setting. If the reset signal is inputted from the $\overline{\text{RES}}$ pin, they are always at high impedance until the mode is set.

■ Outline of Functions

(1)Clock generator
- Source clock generation(max.24MHz)
- CPU clock generation for the 8086/88(max. 8 MHz: duty 1/3)
- Peripheral clock generation for 8086/88(max. 4 MHz)
- CPU Ready(wait end) signal output
- Clock synchronization
- Reset signal output(MN12861 system reset combined)

(2)Programmable Timer/Counter
- 16-bit timer/counter×3(independent)
- Binary/BCD count system
- Count frequency DC 5 MHz
- 6 operation modes:
  - 0: Interrupt at count end
  - 1: Programmable one shot
  - 2: Rate generator
  - 3: Square wave rate generator
  - 4: Software trigger strobe(strobe pulse generation at count end)
  - 5: Hardware trigger strobe(starts the operation above by trigger input)

(3)Programmable I/O
- 3-port(Ports A, B and C, 24 bits) I/O
- Bit setting/resetting allowed for the Port C
- 3-mode I/O operation
  - 0: I/O per byte(I/O by 4 bits allowed for the Port C only)
  - 1: Applied to the Ports A and B. Port C specific bits provide other port's I/O control and buffer status output(interrupt output included).
  - 2: Applied to the Port A only. Port C specific 5 bits provide I/O control and buffer status output(interrupt output included), and provide handshaking through the Port A. The Port A serves as a bidirectional I/O pin.
- Initialization of other function blocks by the system reset pin.

(4)Programmable Interrupt Control
- Target MPU: 8086/88, 8085A, 80286 and Z-80
- Interrupt input: 8, up to 64 by selecting the master/slave(eight 8259As externally attached)
- Interrupt vector address outputted in accordance with an interrupt level
- Interrupt mask and interrupt priority level programmable

■ Absolute Maximum Ratings(V_{SS}=0V, Ta=25°C)

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	−0.3~7.0	V
Input pin voltage	V_{IN}	−0.3~V_{DD}+0.3	V
Output pin voltage	V_{OUT}	−0.3~V_{DD}+0.3	V
Power dissipation	P_T	500	mW
Operating temperature	T_{opr}	−20~+75	°C
Storage temperature	T_{stg}	−65~+150	°C

■ Operating Conditions

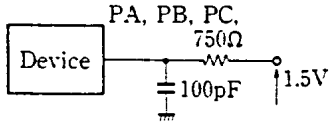
Item	Symbol	Condition	min.	typ.	max.	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Operating temperature	T_{opr}		−20		75	°C

■ Electrical Characteristics

● DC Characteristics(V_{DD} = +5V±10%, Ta = −20 to +75°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Input voltage low level	V_{IL}		−0.3		0.8	V
Input voltage high level	$V_{IH(1)}$	$\overline{RES}$	2.6		V_{IN}−0.3	V
	$V_{IH(2)}$	Other than $\overline{RES}$	2.2		V_{IN}−0.3	V
Output voltage low level	$V_{OL(1)}$	CPUCLK, PCLK I_{OL}=5mA OSC,READY,RESET			0.45	V
	$V_{OL(2)}$	DB0~7 I_{OL}=2.5mA PA0~7 PB0~7 PC0~7			0.45	V
	$V_{OL(3)}$	Output pins other than the above I_{OH}=2.2mA			0.45	V
Output voltage high level	$V_{OH(1)}$	CPUCLK I_{OH}=−1mA	4.0			V
	$V_{OH(2)}$	PCLK, OSC I_{OH}=−1mA READY, RESET	2.8			V
	$V_{OH(3)}$	INT I_{OH}=−100μA	3.5			V
	$V_{OH(4)}$	Output pins other than the above I_{OH}=−400μA	2.4			V
Input hysteresis voltage	V_{INHR} -V_{INLR}	$\overline{RES}$ pin only	0.25			V
Darlington drive current	I_{DAR}	PA0~7 PB0~7 8pins out of them(Note) PC0~7	−1			mA
Input leakage current	$I_{LI(1)}$	IR0~7 V_{IN}=0~V_{DD}	−300		10	μA
	$I_{LI(2)}$	$\overline{ASYNC}$ V_{IN}=0~V_{DD}	−200		10	μA
	$I_{LI(3)}$	Input pins other than the above V_{IN}=0~V_{DD}	−10		10	μA
Output leakage current	I_{LO}	V_{OUT}=0~V_{DD}	−10		10	μA
Standby current	I_{DDST}	At initialize time, output pins opened and input pin level fixed(pull-up pins: High level)			0.5	mA
Supply current	I_{DD}	Output pin no-load, f_{CLK0-2}=5 MHz, foce=24MHz.8086-2(8MHz)assumed to be used			80	mA

Note) Measure with the following circuit.



● Capacitance(V_{DD}=GND=0V, Ta=25°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Input capacitance	C_{IN}	Other than f_C=1MHz measured pins. Fixed at 0 V Note)			10	pF
Output capacitance(at high impedance)	C_{OUT}	Other than f_C=1MHz measured pins. Fixed at 0V Note)			20	pF

Note) The X1, X2, OSC, CPUCLK, PCLK, READY and RESET pins are excluded.

● AC Characteristics (1) MPU Interface(V_{DD}=5V±10%, Ta=−20 to +75°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
[Read Cycle]						
Address($\overline{CS}$, A0, A1) stable time Note)	$t_{AR(1)}$	Timer/counter	30			ns
	$t_{AR(2)}$	I/O, interrupt controller	0			ns
Address($\overline{CS}$, A0, A1) holding time Note)	t_{RA}		0			ns
RD pulse width	t_{RR}		150			ns
Read data delay time	t_{RD}	CL=150pF			120	ns
Read data floating time	t_{RF}	CL=20 pF, RL=2KΩ	10		85	ns
[Write Cycle]						
Address(CS, A0, A1) stable time Note)	t_{AW}		0			ns
Address(CS, A0, A1) holding time Note)	t_{WA}		0			ns
$\overline{WR}$ pulse width	$t_{WW(1)}$	Timer/counter	160			ns
	$t_{WW(2)}$	I/O,interrupt controller	120			ns
Write data setting time	$t_{DW(1)}$	Timer/counter, interrupt controller	120			ns
	$t_{DW(2)}$	I/O	100			ns
Write data holding time	t_{WD}		0			ns
[Read, Write Bus Recovery Time]						
Read recovery time	$t_{RV(1)}$	Timer/counter, I/O	200			ns
	$t_{RV(2)}$	Interrupt controller	160			ns
Write recovery time	$t_{WV(1)}$	Timer/counter, I/O	200			ns
	$t_{WV(2)}$	Interrupt controller	190			ns
Read/write recovery time	$t_{RWV(1)}$	Timer/counter, I/O, interrupt controller	200			ns
	$t_{RWV(2)}$	Interrupt controller, $\overline{INTA}$−$\overline{RD}$/$\overline{WR}$	250			ns

Note) $\overline{CS}$ means $\overline{CS_{PTC}}$, $\overline{CS_{PIO}}$, $\overline{CS_{PINT}}$.

● AC Characteristics 2) Clock Generator(V_{DD}=5V±10%, Ta=−20 to +75°C)

Item		Symbol	Condition	min.	typ.	max.	Unit
EFI	High-level width	t_{EHEL}	90%−90% V_{IN}	13			ns
	Low-level width	t_{ELEH}	10%−10% V_{IN}	13			ns
	Cycle	t_{ELEL}	Note 1)	41.6			ns
Quartz frequency		f_{OSC}		8		24	MHz
RDY1	Active setting time	t_{RIVCL}	$\overline{ASYNC}$=HIGH	35			ns
RDY2	(to CPUCLK)	t_{RIVCH}	$\overline{ASYNC}$=LOW	35			ns
	Inactive setting time (to CPUCLK)	t_{RIVCL}		35			ns
	Holding time (to CPUCLK)	t_{CLRIX}		0			ns
$\overline{ASYNC}$	Setting time(to CPUCLK)	t_{AYVCL}		50			ns
	Holding time(to CPUCLK)	t_{CLAYX}		0			ns
$\overline{AEN1}$ $\overline{AEN2}$	Setting time(to RDY1, RDY2)	t_{AIVRIV}		15			ns
	Holding time (to CPUCLK)	t_{CLAIX}		0			ns
CSYNC	Setting time (to CPUCLK)	t_{YHEH}		20			ns
	Holding time (to CPUCLK)	t_{EHYL}		10			ns
	Pulse width	t_{YHYL}		2-t_{ELEL}			ns
$\overline{RES}$	Setting time (to CPUCLK)	t_{IIHCL}	Note 1)	65			ns
	Holding time (to CPUCLK)	t_{CLIIH}	Note 1)	20			ns
Input rise time		t_{ILIH}	0.8~2.0V			20	ns
Input fall time		t_{IHIL}	2.0~0.8V			12	ns
CPUCLK	Cycle	t_{CKLCKL}		125			ns
	High-level width	t_{CKHCKL}	See Measuring Circuit Diagrams 3 and 4.	(1/3 t_{CKLCKL}) −2			ns
	Low-level width	t_{CKLCKH}	See Measuring Circuit Diagrams 3 and 4.	(2/3 t_{CKLCKL}) −15			ns
	Rise time	t_{CHICH2}	1.0V~3.5V			10	ns
	Fall time	t_{CL2CL1}	3.5V~1.0V			10	ns
PCLK	High-level width	t_{PHPL}		t_{CLCL}−20			ns
	Low-level width	t_{PLPH}		t_{CLCL}−20			ns
READY	Inactive time (to CPUCLK) Note 2)	t_{RYLCL}	See Measuring Circuit Diagrams 5 and 6.	−8			ns
	Active time (to CPUCLK) Note 3)	t_{RYHCH}	See Measuring Circuit Diagrams 5 and 6.	(2/3t_{CLCL}) −15			ns

Note 1) Required only when assuring an acceptance by the next clock.
Note 2) Applied to the T2 state.(For meaning of the T2 state, see Intel MPU8086/88)
Note 3) Applied to the T3 and TW states only.(For meanings of the T3 and TW states, see Intel MPU8086/88)

● AC Characteristics (2) (Continued)

Item	Symbol	Condition	min.	typ.	max.	Unit
CLK→RESER delay time	t_{CLIL}				40	ns
CLK→POLK ↑ delay time	t_{CLPH}				22	ns
CLK→PCLK ↓ delay time	t_{CLPL}				22	ns
OSC→CLK ↑ delay time	t_{OLCH}		−5		22	ns
OSC→CLK ↓ delay time	t_{OLCL}		2		35	ns
Output rise time	t_{OLOH}	0.8 to 2.0 V for other than CPUCLK			20	ns
Output fall time	t_{OHOL}	2.0 to 0.8 V for other than CPUCLK			12	ns

● AC Characteristics (3) Timer/Counter (V_{DD}=5V±10%, Ta=−20 to +75°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Clock cycle	t_{CLK}		200		DC	ns
Clock pulse width(H period)	t_{PWH}		80			ns
Clock pulse width(L period)	t_{PWL}		80			ns
Gate pulse width(H period)	t_{GW}		50			ns
Gate setting time(to CLK ↑)	t_{GS}		50			ns
Gate holding time(to CLK ↑)	t_{GH}		50			ns
Gate pulse width(L period)	t_{GL}		50			ns
Output delay time(to CLK ↓)	t_{OD}	C_L=150pF			150	ns
Output delay time(to GATE ↓)	t_{ODG}	C_L=150pF			120	ns

● AC Characteristics (4) I/O Section (V_{DD}=5V±10%, Ta=−20 to +75°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
WR=1 Output delay time	t_{WB}	C_L=150pF			350	ns
Peripheral data setting time (to $\overline{RD}$)	t_{IR}		0			ns
Peripheral data holding time(to $\overline{RD}$)	t_{HRL}		0			ns
ACK pulse width	t_{AK}		300			ns
STB pulse width	t_{ST}		350			ns
Peripheral data setting time(to STB)	t_{PS}		0			ns
Peripheral data holding time(to STB)	t_{PH}		150			ns
$\overline{ACK}$→Output delay time	t_{AD}	CL=150pF			300	ns
$\overline{ACK}$→Output float delay time	t_{KD}		20		250	ns
$\overline{WR}$=1→$\overline{OBF}$=0	t_{WOB}				300	ns
$\overline{ACK}$=0→OBF=1	t_{AOB}				350	ns
$\overline{STB}$=0→IBF=1	t_{SIB}				300	ns
$\overline{RD}$=1→IBF=0	t_{RIB}				300	ns
$\overline{RD}$=0→INTR=0	t_{RIT}				400	ns
$\overline{SBT}$=1→INTR=1	t_{SIT}				300	ns
$\overline{ACK}$=1→INTR=1	t_{AIT}				350	ns
$\overline{WR}$=0→INTR=0	t_{WIT}				450	ns

Remark) At least, a reset pulse width of 50 μs is required during or immediately after power-on. Thereafter, 500 ns min.is sufficient.

● AC Characteristics(5) Interrupt Controller(V_{DD}=5V±10%, Ta=−20 to +75°C)

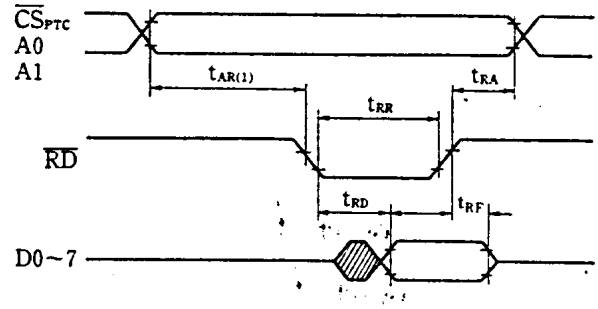
Item	Symbol	Condition	min.	typ.	max.	Unit
IR input pulse width	t_{JLJH}	Note)	100			ns
INT output delay time	t_{JHIH}				300	ns
$\overline{INTA}$ 1st-CAS delay time	t_{IALCV}	Master only			360	ns
$\overline{INTA}$ 2nd 3rd-CAS setting time	t_{CVIAL}	Slave only	40			ns
$\overline{INTA}$ pulse width	t_{RLRH}	Same as t_{RR} for $\overline{RD}$ read	120			ns
$\overline{INTA}$ read address setting time	t_{AHRL}	Same as $t_{AR(2)}$ for $\overline{RD}$ read	0			ns
$\overline{INTA}$ read address holding time	t_{RHAX}	Same as t_{RA} for $\overline{RD}$ read	0			ns
$\overline{INTA}$ read data delay time	t_{RLDV}				120	ns
Address($\overline{CS}$, PINT, A0)read data delay time	t_{AHDV}	Applied to both $\overline{RD}$ and $\overline{INTA}$ read			200	ns
$\overline{INTA}$ read data holdeing time	t_{RHDZ}		10		85	ns
CAS read data delay time	t_{CVDV}				200	ns
$\overline{INTA}$ recovery time	t_{RHRL}	At an identical sequence	160			ns
	t_{CHCL}	At other $\overline{INTA}$ sequence	250		ns	
EN pulse delay time	t_{RLEL}	$\overline{RD}$↓/$\overline{INTA}$↓−$\overline{EN}$↓			100	ns
$\overline{EN}$ pulse holding time	t_{RHEH}	$\overline{RD}$↑/$\overline{INTA}$↑−$\overline{EN}$↑			150	ns

Note) Time required to clear the input latch in the edge trigger mode

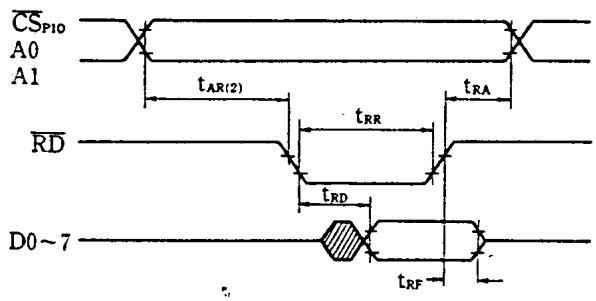
■ AC Timing Diagrams

(1)Read Cycles

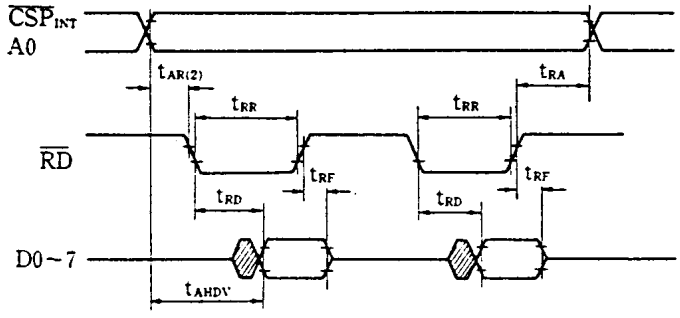
1.Timer/counter read cycle



2.I/O section read cycle(same as Mode-0 Input)

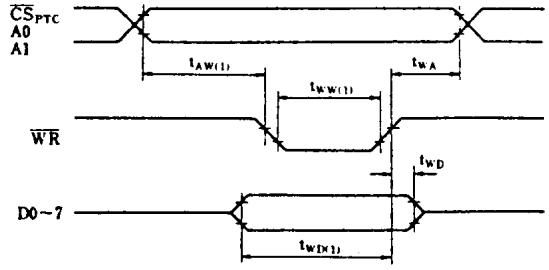


3.Inputtupt controller read cycle

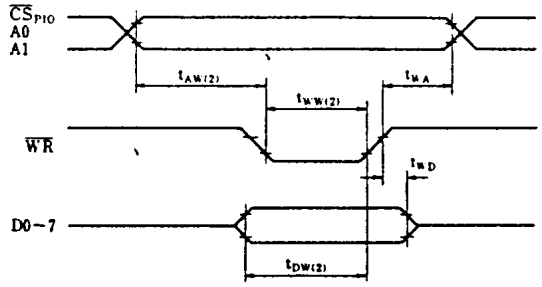


(2) Write Cycles

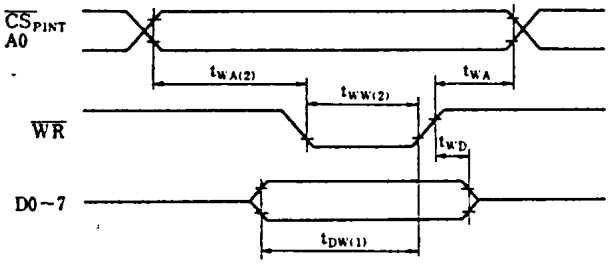
1. Timer/Counter



2. I/O section

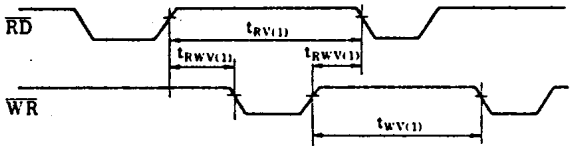


3. Interrupt controller

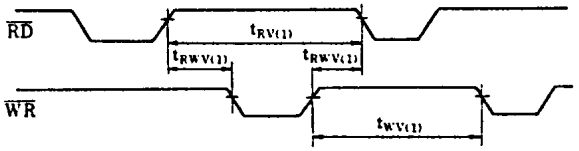


(3) Read/Write Bus Recovery Time

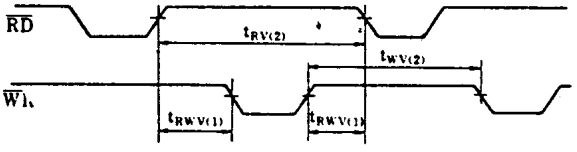
1. Timer/counter

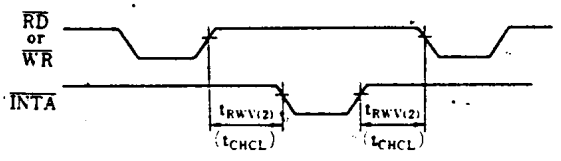


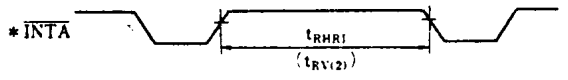
2. I/O section

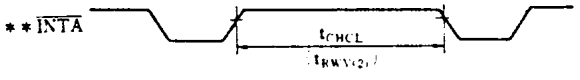


3. Interrupt controller







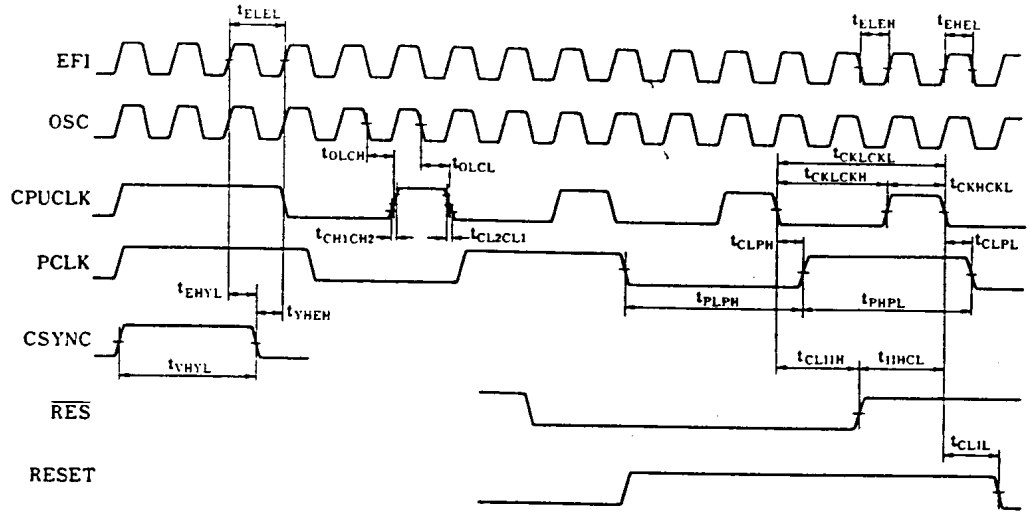


*$\overline{INTA}$ operates identical with the $\overline{RD}$ signal. This timing applies to continuous vector read.

**Applies to new vector read for another interrupt cause after completing one vector read of $\overline{INTA}$.

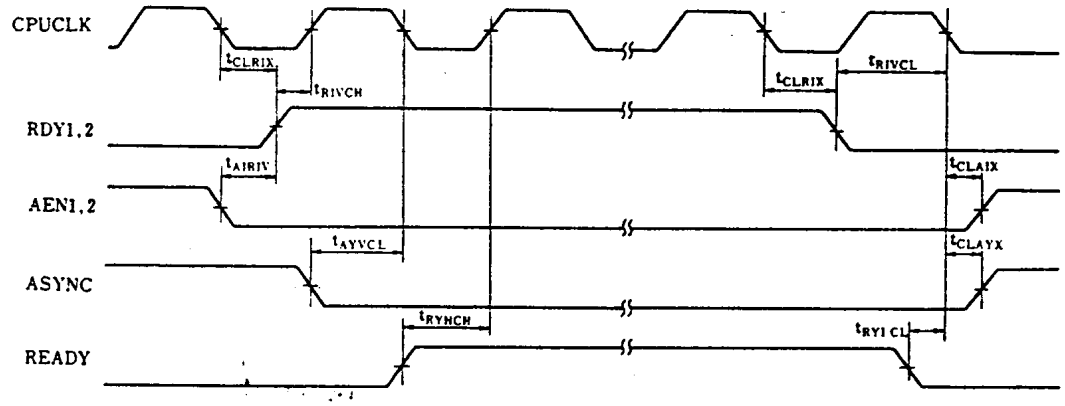
(4) Clock Generator

● CPUCLK and RESET signals

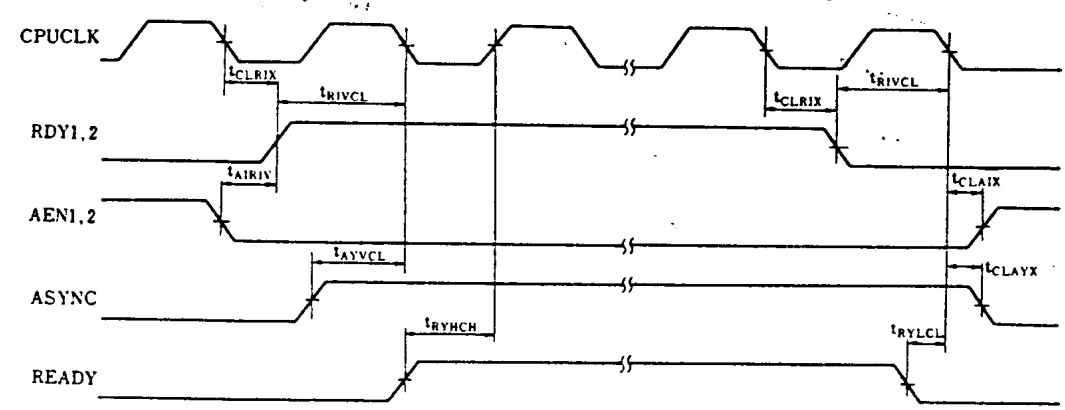


Note) A timing measuring point is at 1.5 V, unless otherwise specified.

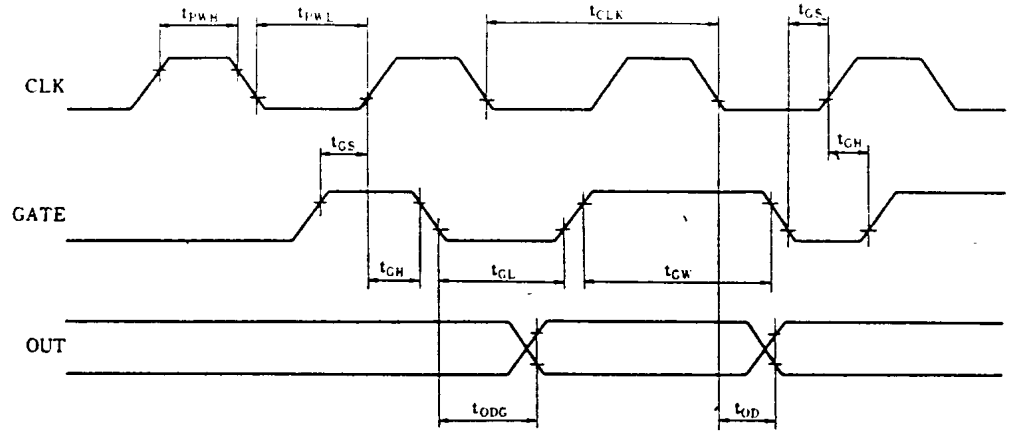
● READY signal(Async. device)



● READY signal(Sync. device)

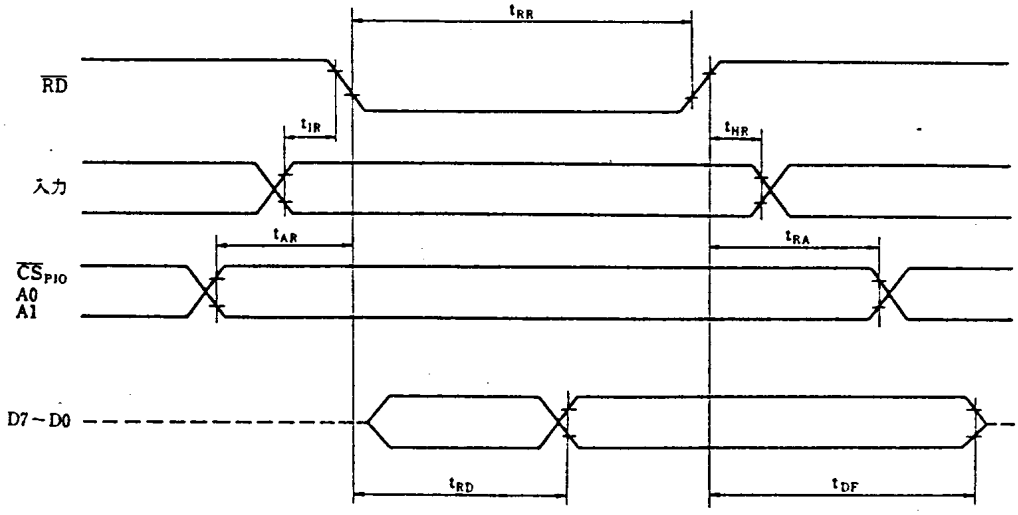


(5) Timer/Counter

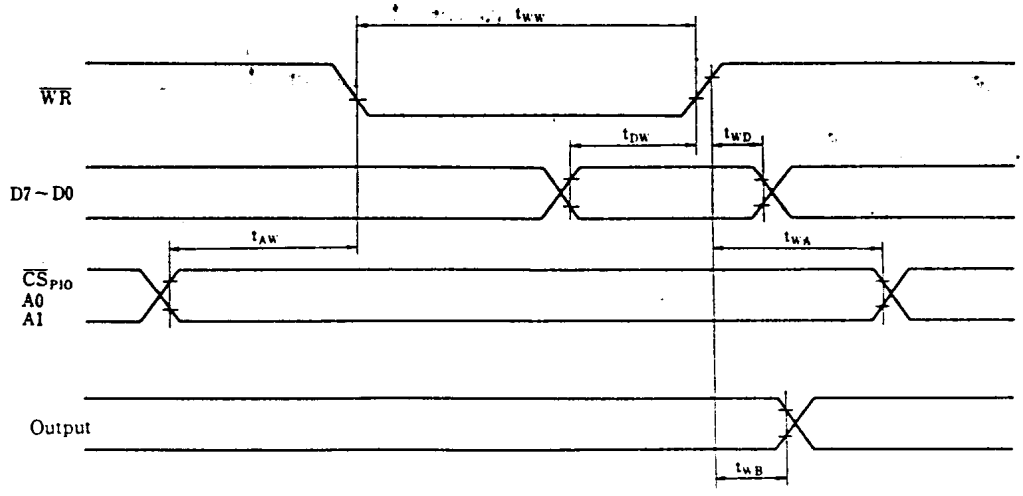


(6) I/O Section

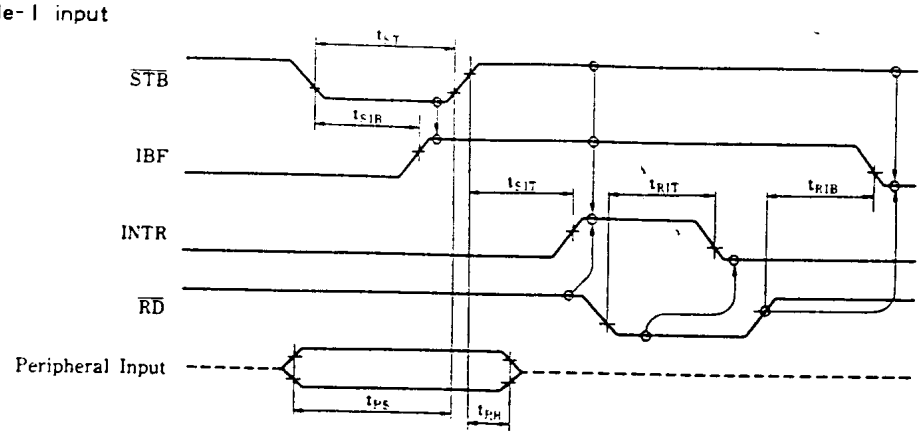
● Mode-0 input



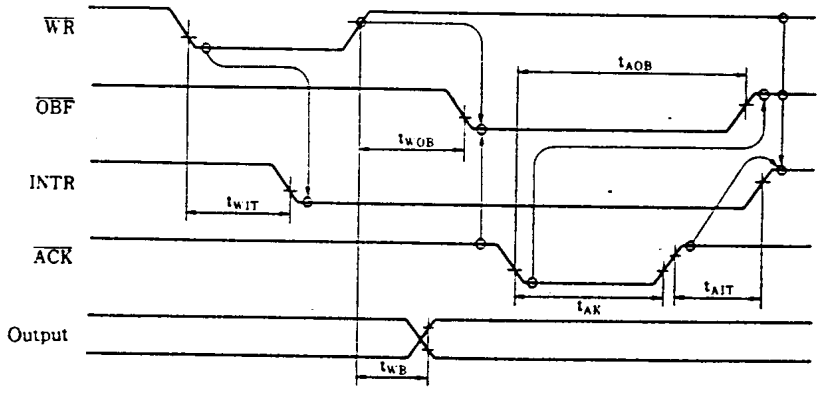
● Mode-0 output



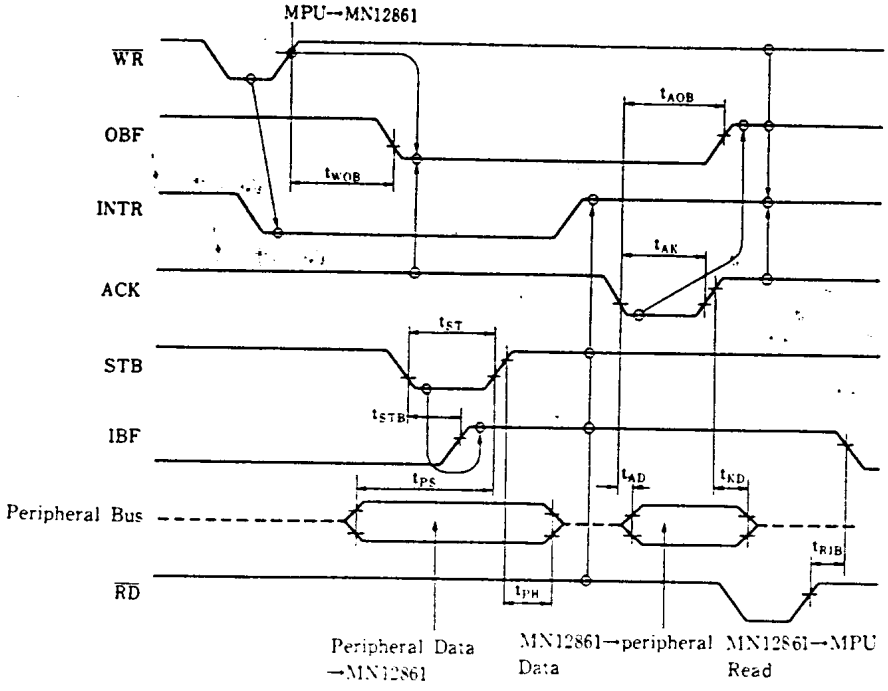
● Mode-1 input



● Model-1 output

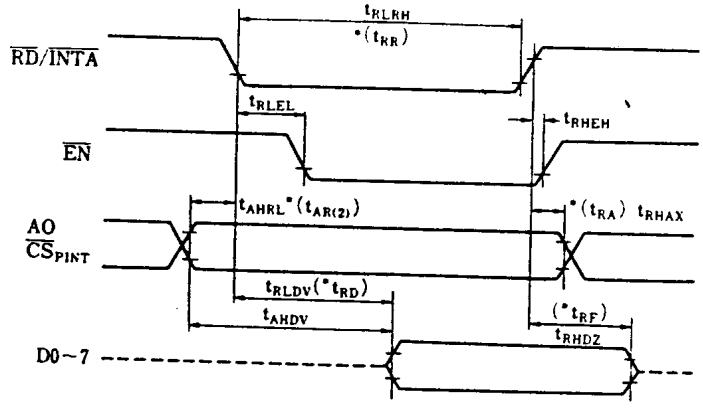


● Mode 2(Bidirectional)

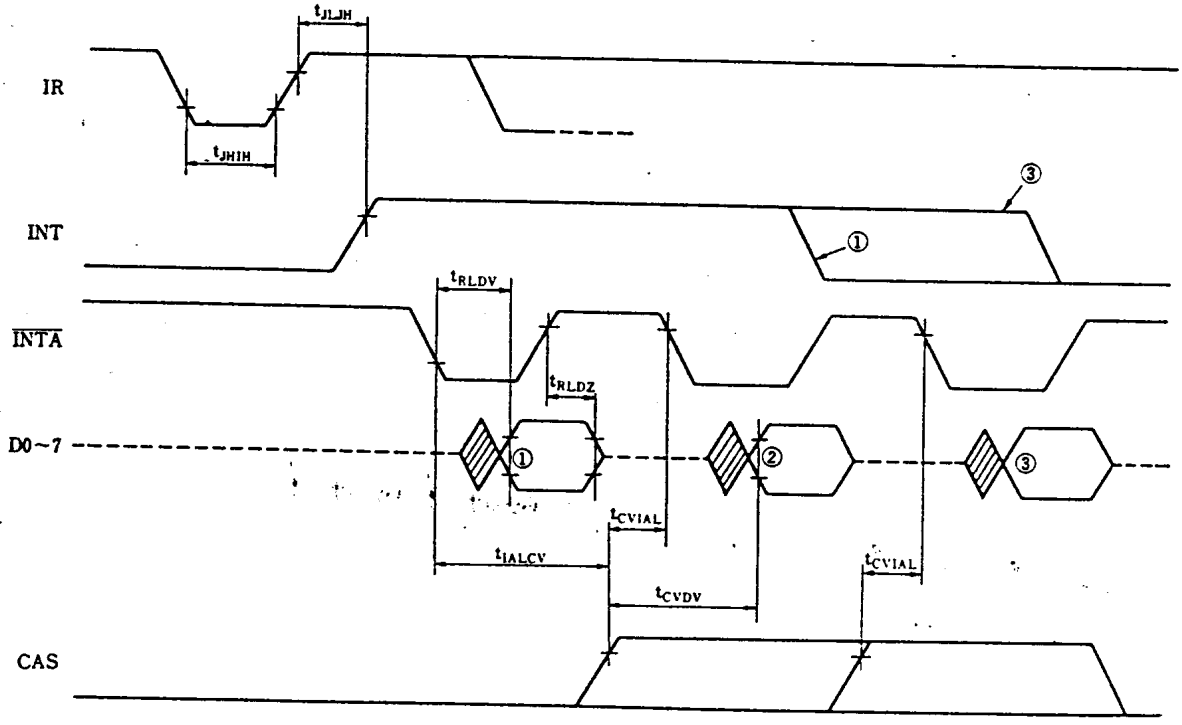


(7) Interrupt Controller

1. Read, interrupt acknowledge operation(∗ : $\overline{RD}$ operation time)



2. Interrupt sequence



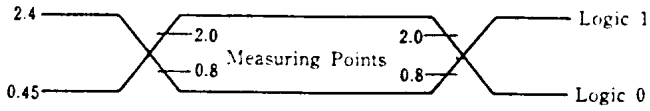
Remark: INT output must keep High at least until the front edge of 1st $\overline{INTA}$.

① Cycle 1 in the 8086/8088 system. The data bus is not driven.

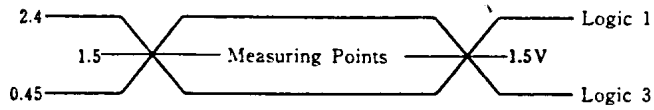
② 8080/8085 system only

■ I/O Waveforms for AC Test

● Other than Clock Generator

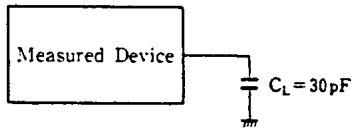


● Clock Generator

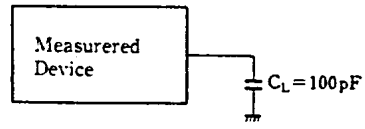


■ Load Conditions

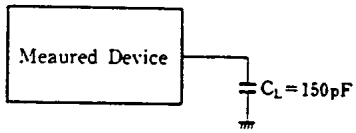
● OSC, PCLK, READY, RESET



● CPUCLK

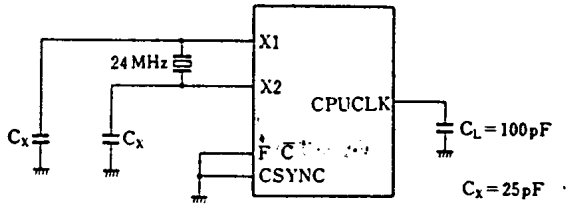


● All Output Terminals other than 5 Terminals Above

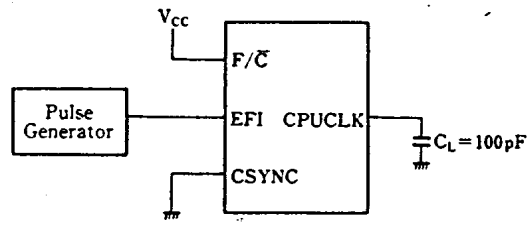


■ Measuring Circuits

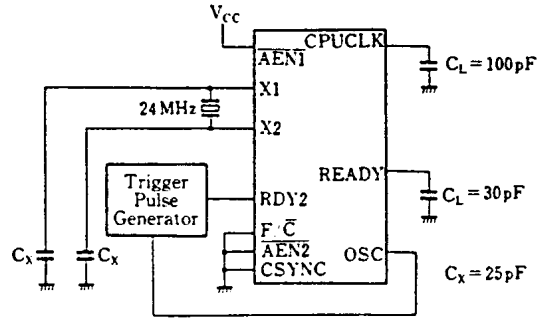
● CPUCLK High/Low Level Width Measuring Circuit(When X1, X2 Used)



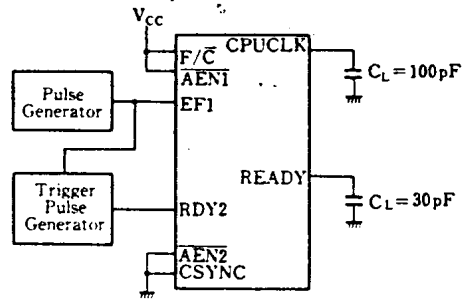
● CPUCLK High/Low Level Width Measuring Circuit(When EFI Used)



● Ready vs. CPUCLK Time Measuring Circuit (When X1, X2 Used)



● Ready vs. CPUCLK Time Measuring Circuit (When EFI Used)



■ MN12861 Address Setting(Table 1)

$\overline{WR}$	$\overline{RD}$	CS PTC	CS PIO	CS PINT	$\overline{INTA}$	D0 ~ 7	Data Bus Operation
1	0	0	1	1	1	OUT	Timer Counter →Data
1	0	1	0	1	1	OUT	I O section →Data
1	0	1	1	0	1	OUT	Interrupt controller →Data
1	1	1	1	1	0	OUT	Interrupt controller →Data
0	1	0	1	1	1	IN	Data→Timer counter
0	1	1	0	1	1	IN	Data→I O section
0	1	1	1	0	1	IN	Data→Interrupt controller
1	1	×	×	×	1	Z	Data bus high impedance
×	×	1	1	1	1	Z	Data bus high impedance
0	0	×	×	×	×	—	Prohibited
×	×	0	0	0	×	—	Prohibited
1	0	0	×	×	0	—	Prohibited
1	0	×	0	×	0	—	Prohibited
1	0	×	×	0	0	—	Prohibited
0	1	0	×	×	0	—	Prohibited
0	1	×	0	×	0	—	Prohibited
0	1	×	×	0	0	—	Prohibited

Note) X denotes either 0(=L) or 1(=H).

■ I/O Section Address Setting(Table 2)

D7	A1	A0	$\overline{WR}$	$\overline{RD}$	CS PIO	Operation	
×	0	0	1	0	0	PA → D	Read
×	0	1	1	0	0	PB → D	
×	1	0	1	0	0	PC → D	
×	1	1	1	0	0	Prohibited	
×	0	0	0	1	0	D → PA	Write
×	0	1	0	1	0	D → PB	
×	1	0	0	1	0	D → PC	
0	1	1	0	1	0	D → CWRIO	
1	1	1	0	1	0	D → Bit control	
×	×	×	×	×	1	D0-D7 high impedance	
×	×	×	1	1	0	D0-D7 high impedance	

■ Timer/Counter Address Setting(Table 3)

A1	A0	$\overline{WR}$	$\overline{RD}$	CS PIO	Bus Operation
0	0	1	0	0	Read from the counter =0
0	1	1	0	0	Read from the counter =1
1	0	1	0	0	Read from the counter =2
1	1	1	0	0	No operation(high impedance)
0	0	0	1	0	Write to the counter =0
0	1	0	1	0	Write to the counter =1
1	0	0	1	0	Write to the counter =2
1	1	0	1	0	Write to CWRTC
×	×	1	1	1	Disable(high impedance)
×	×	1	1	0	No operation(high impedance)

■ Interrupt Control Address Setting(Table 4)

D4	D3	A0	$\overline{WR}$	$\overline{RD}$	CS PINT	$\overline{INTA}$	Bus Operation
×	×	0	1	0	0	1	IRR, ISR, interrupt level read[Note 1]
×	×	1	1	0	0	1	Read from IMR
0	0	0	0	1	0	1	Write to OCW2
0	1	0	0	1	0	1	Write to OCW3
1	×	0	0	1	0	1	Write to ICW1
×	×	1	0	1	0	1	Write to ICW4[Note 2]
×	×	×	1	1	0	1	High impedance
×	×	×	×	×	1	1	High impedance
×	×	×	1	1	1	0	Interrupt vector read

Note 1) OCW3 changes what is read.

Note 2) Write operation is sequentially performed by the sequence circuit.