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The RF MOSFET Line

Power Field-Effect Transistor

N–Channel Enhancement–Mode

MRF275G

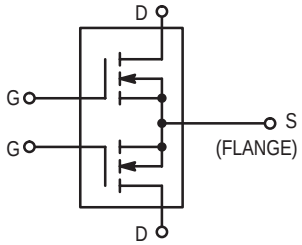
150 W, 28 V, 500 MHz
N–CHANNEL MOS
BROADBAND
100 – 500 MHz
RF POWER FET

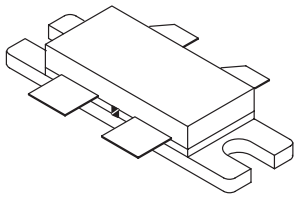
Designed primarily for wideband large–signal output and driver stages from 100 – 500 MHz.

- Guaranteed Performance @ 500 MHz, 28 Vdc
  - Output Power — 150 Watts
  - Power Gain — 10 dB (Min)
  - Efficiency — 50% (Min)
  - 100% Tested for Load Mismatch at all Phase Angles with VSWR 30:1
- Overall Lower Capacitance @ 28 V
  - C_{iss} — 135 pF
  - C_{oss} — 140 pF
  - C_{rss} — 17 pF
- Simplified AVC, ALC and Modulation

Typical data for power amplifiers in industrial and commercial applications:

- Typical Performance @ 400 MHz, 28 Vdc
  - Output Power — 150 Watts
  - Power Gain — 12.5 dB
  - Efficiency — 60%
- Typical Performance @ 225 MHz, 28 Vdc
  - Output Power — 200 Watts
  - Power Gain — 15 dB
  - Efficiency — 65%





CASE 375–04, STYLE 2

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	65	Vdc
Gate–Source Voltage	V_{GS}	±40	Adc
Drain Current — Continuous	I_D	26	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	400 2.27	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.44	°C/W

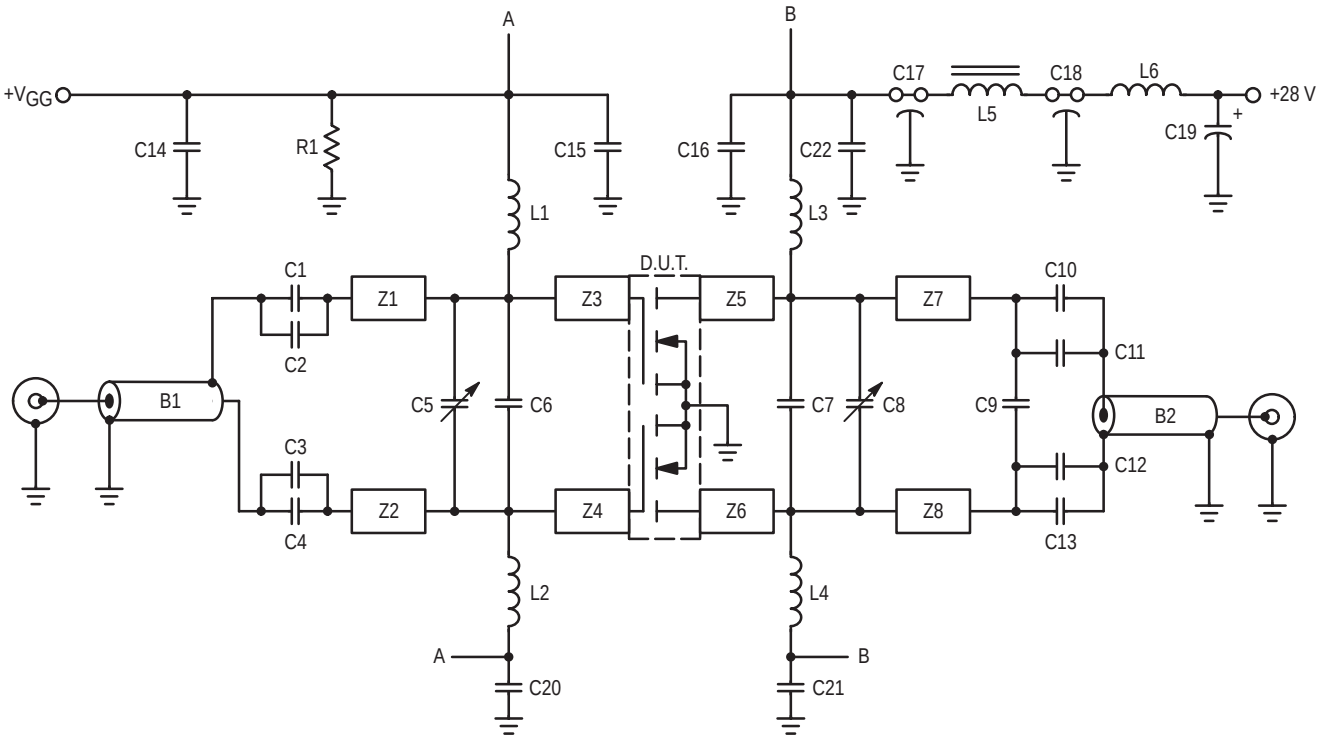
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

tyco Electronics
M/A-COM

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (1)					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 50 mA)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 V, V_{GS} = 0)	I_{DSS}	—	—	1	mA
Gate–Source Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSS}	—	—	1	μA
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 100 mA)	$V_{GS(th)}$	1.5	2.5	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 V, I_D = 5 A)	$V_{DS(on)}$	0.5	0.9	1.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)	g_{fs}	3	3.75	—	mhos
DYNAMIC CHARACTERISTICS (1)					
Input Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	135	—	pF
Output Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	140	—	pF
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	17	—	pF
FUNCTIONAL CHARACTERISTICS (2) (Figure 1)					
Common Source Power Gain (V_{DD} = 28 V, P_{out} = 150 W, f = 500 MHz, I_{DQ} = 2 x 100 mA)	G_{ps}	10	11.2	—	dB
Drain Efficiency (V_{DD} = 28 V, P_{out} = 150 W, f = 500 MHz, I_{DQ} = 2 x 100 mA)	η	50	55	—	%
Electrical Ruggedness (V_{DD} = 28 V, P_{out} = 150 W, f = 500 MHz, I_{DQ} = 2 x 100 mA, VSWR 30:1 at all Phase Angles)	ψ	No Degradation in Output Power			

1. Each side of device measured separately.
2. Measured in push–pull configuration.



B1	Balun, 50 Ω, 0.086″ O.D. 2″ Long, Semi Rigid Coax
B2	Balun, 50 Ω, Coax 0.141″ O.D. 2″ Long, Semi Rigid
C1, C2, C3, C4, C10, C11, C12, C13	270 pF, ATC Chip Capacitor
C5, C8	1.0 – 20 pF, Trimmer Capacitor, Johanson
C6	22 pF, Mini–Unelco Capacitor
C7	15 pF, Unelco Capacitor
C9	2.1 pF, ATC Chip Capacitor
C14, C15, C16, C20, C21, C22	0.1 μF, Ceramic Capacitor
C17, C18	680 pF, Feedthru Capacitor
C19	10 μF, 50 V, Electrolytic Capacitor, Tantalum
L1, L2	10 Turns AWG #24, 0.145″ O.D., 106 nH Taylor–Spring Inductor
L3, L4	10 Turns AWG #18, 0.340″ I.D., Enameled Wire
L5	Ferroxcube VK200 20/4B
L6	4 Turns #16, 0.340″ I.D., Enameled Wire
R1	1.0 kΩ,1/4 W Resistor
W1 – W4	20 x 200 x 250 mils, Wear Pads, Beryllium–Copper, (See Component Location Diagram)
Z1, Z2	1.10″ x 0.245″, Microstrip Line
Z3, Z4, Z5, Z6	0.300″ x 0.245″, Microstrip Line
Z7, Z8	1.00″ x 0.245″, Microstrip Line
Board material	0.060″ Teflon–fiberglass, ε_r = 2.55, copper clad both sides, 2 oz. copper.

Points A are connected together on PCB.
Points B are connected together on PCB.

Figure 1. 500 MHz Test Circuit

TYPICAL CHARACTERISTICS

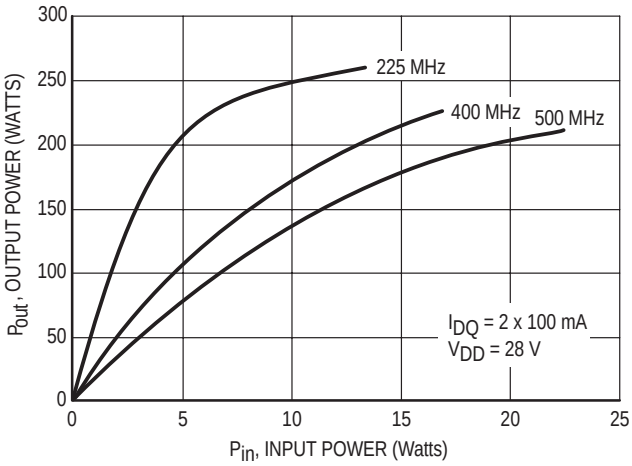


Figure 2. Output Power versus Input Power

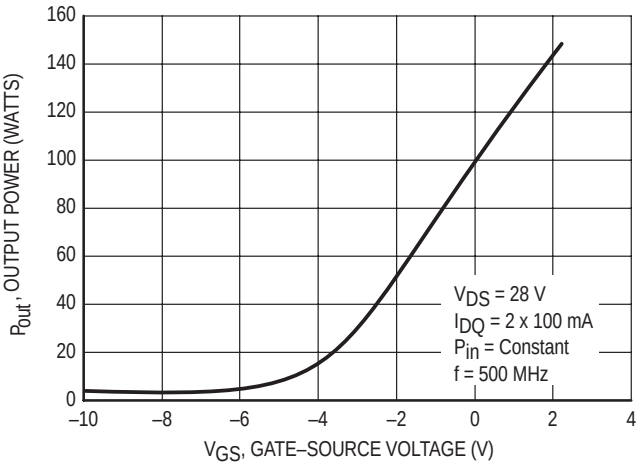


Figure 3. Output Power versus Gate Voltage

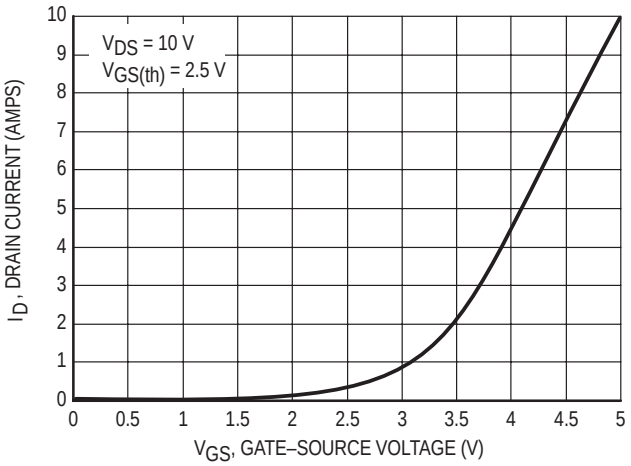


Figure 4. Drain Current versus Gate Voltage (Transfer Characteristics)

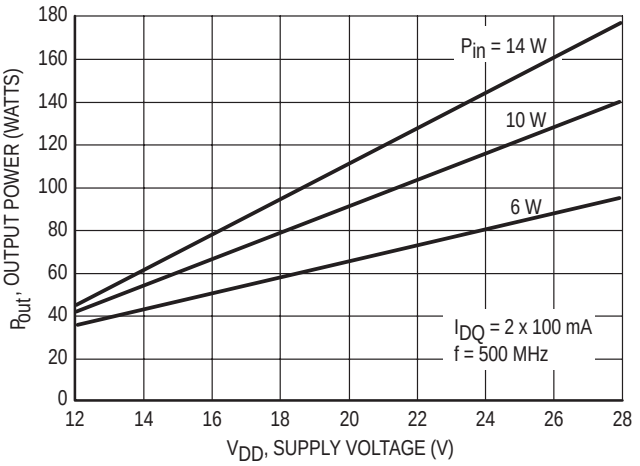


Figure 5. Output Power versus Supply Voltage

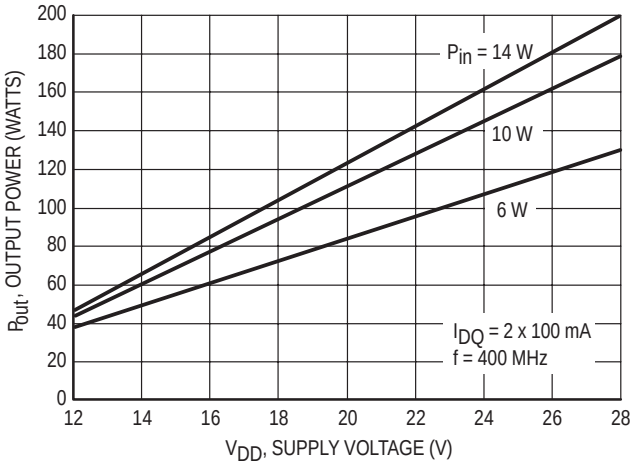


Figure 6. Output Power versus Supply Voltage

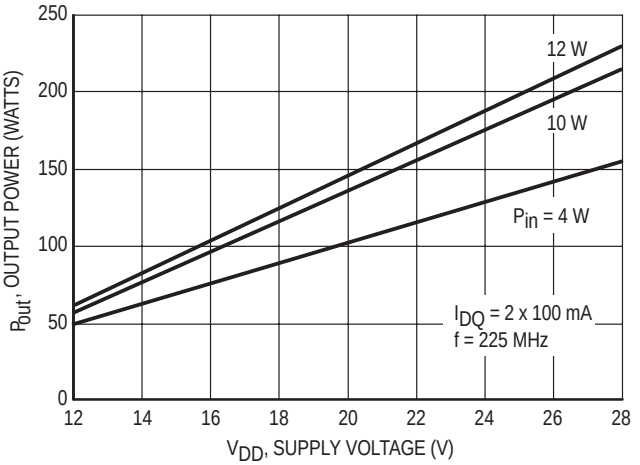


Figure 7. Output Power versus Supply Voltage

TYPICAL CHARACTERISTICS

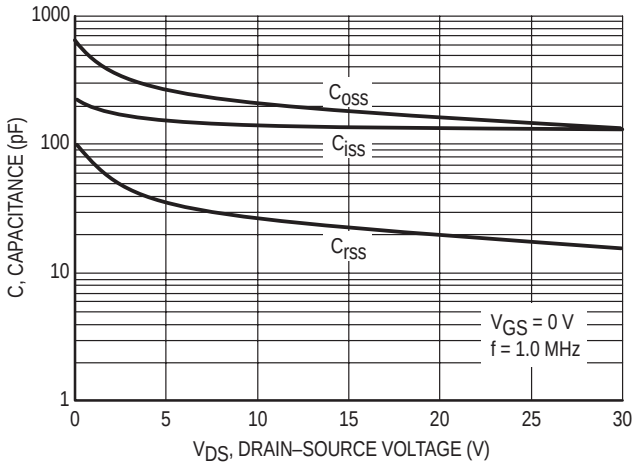


Figure 8. Capacitance versus Drain–Source Voltage*
*Data shown applies only to one half of device, MRF275G

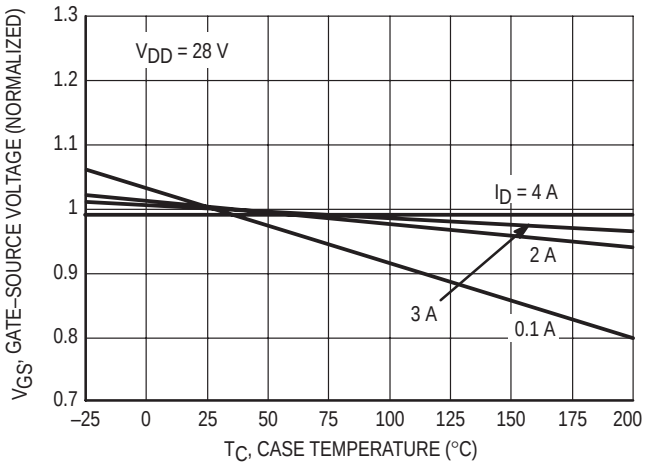


Figure 9. Gate–Source Voltage versus Case Temperature

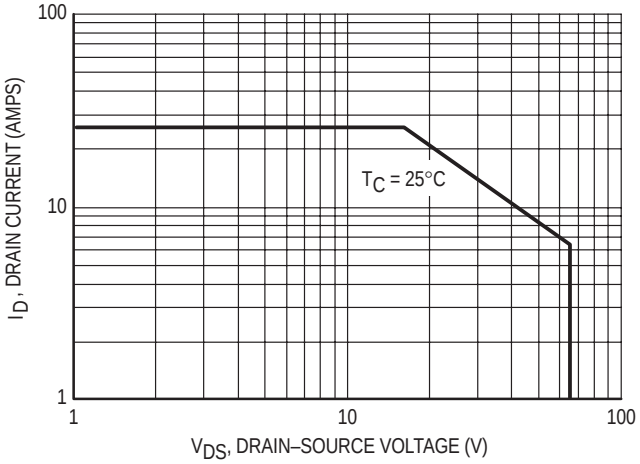
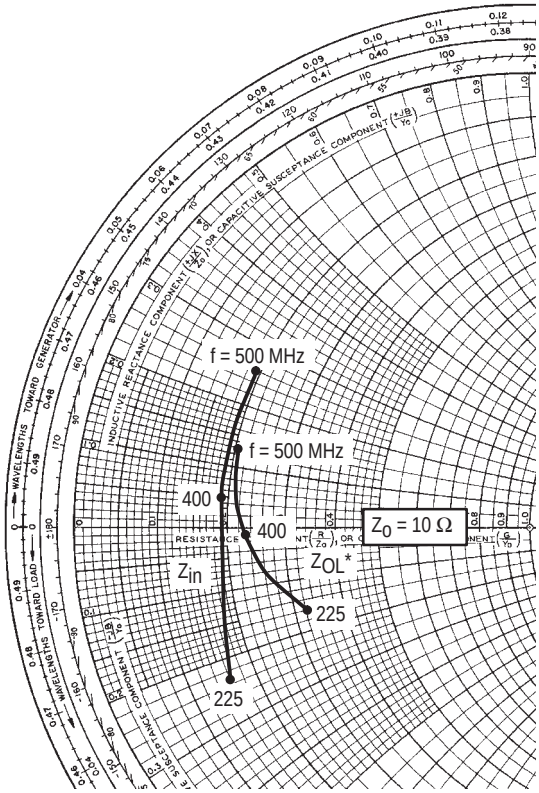


Figure 10. DC Safe Operating Area



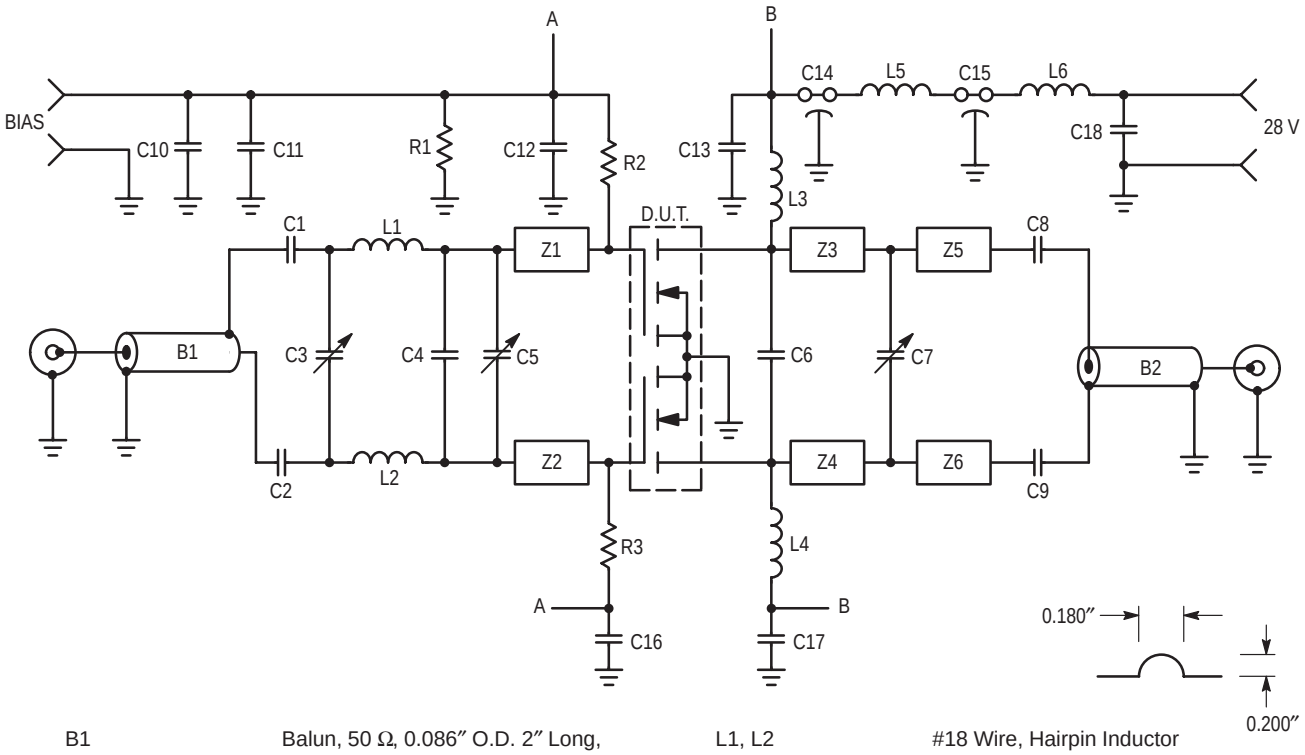
V_{DD} = 28 V, I_{DQ} = 2 x 100 mA, P_{out} = 150 W

f (MHz)	Z_{in} Ohms	Z_{OL}* Ohms
225	1.6 – j2.30	3.2 – j1.50
400	1.9 + j0.48	2.3 – j0.19
500	1.9 + j2.60	2.0 + j1.30

Z_{OL}* = Conjugate of the optimum load impedance into which the device operates at a given output power, voltage and frequency.

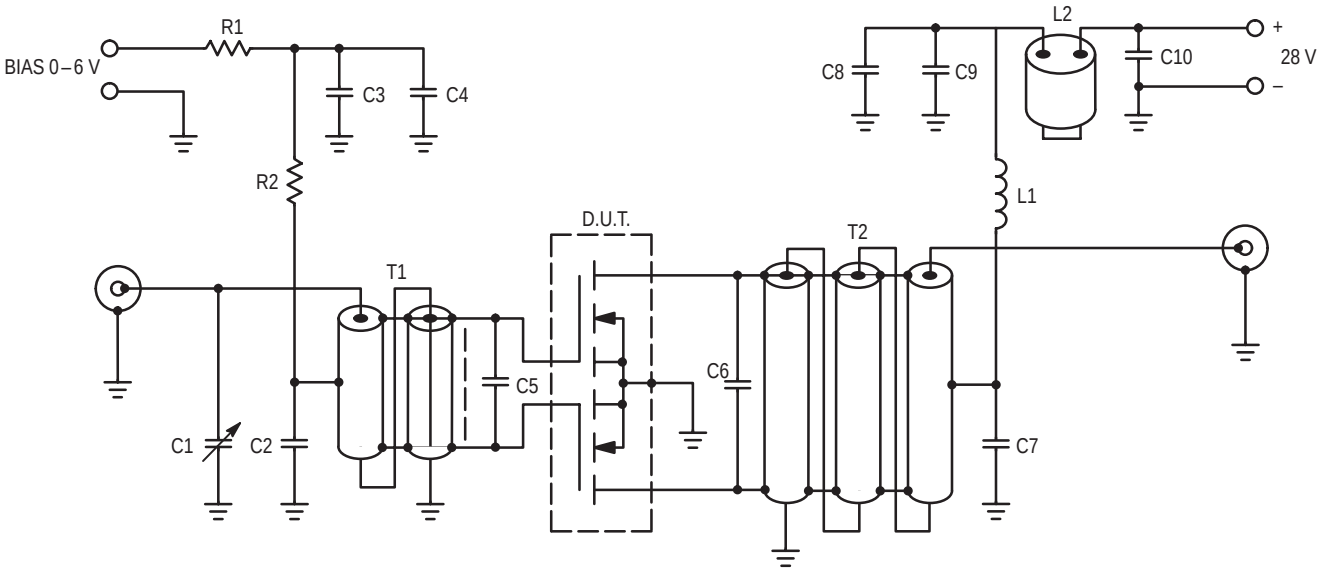
Note: Input and output impedance values given are measured from gate to gate and drain to drain respectively.

Figure 11. Series Equivalent Input/Output Impedance



B1	Balun, 50 Ω, 0.086″ O.D. 2″ Long, Semi Rigid Coax	L1, L2	#18 Wire, Hairpin Inductor
B2	Balun, 50 Ω, 0.141″ O.D. 2″ Long, Semi Rigid Coax	L3, L4	12 Turns #18, 0.340″ I.D., Enameled Wire
C1, C2, C8, C9	270 pF, ATC Chip Capacitor	L5	Ferroxcube VK200 20/4B
C3, C5, C7	1.0–20 pF, Trimmer Capacitor	L6	3 Turns #16, 0.340″ I.D., Enameled Wire
C4	15 pF, ATC Chip Capacitor	R1	1.0 kΩ, 1/4 W Resistor
C6	33 pF, ATC Chip Capacitor	R2, R3	10 kΩ, 1/4 W Resistor
C10, C12, C13, C16, C17	0.01 μF, Ceramic Capacitor	Z1, Z2	0.400″ x 0.250″, Microstrip Line
C11	1.0 μF, 50 V, Tantalum	Z3, Z4	0.870″ x 0.250″, Microstrip Line
C14, C15	680 pF, Feedthru Capacitor	Z5, Z6	0.500″ x 0.250″, Microstrip Line
C18	20 μF, 50 V, Tantalum	Board material	0.060″ Teflon–fiberglass, ε_r = 2.55, copper clad both sides, 2 oz. copper.

Figure 12. 400 MHz Test Circuit



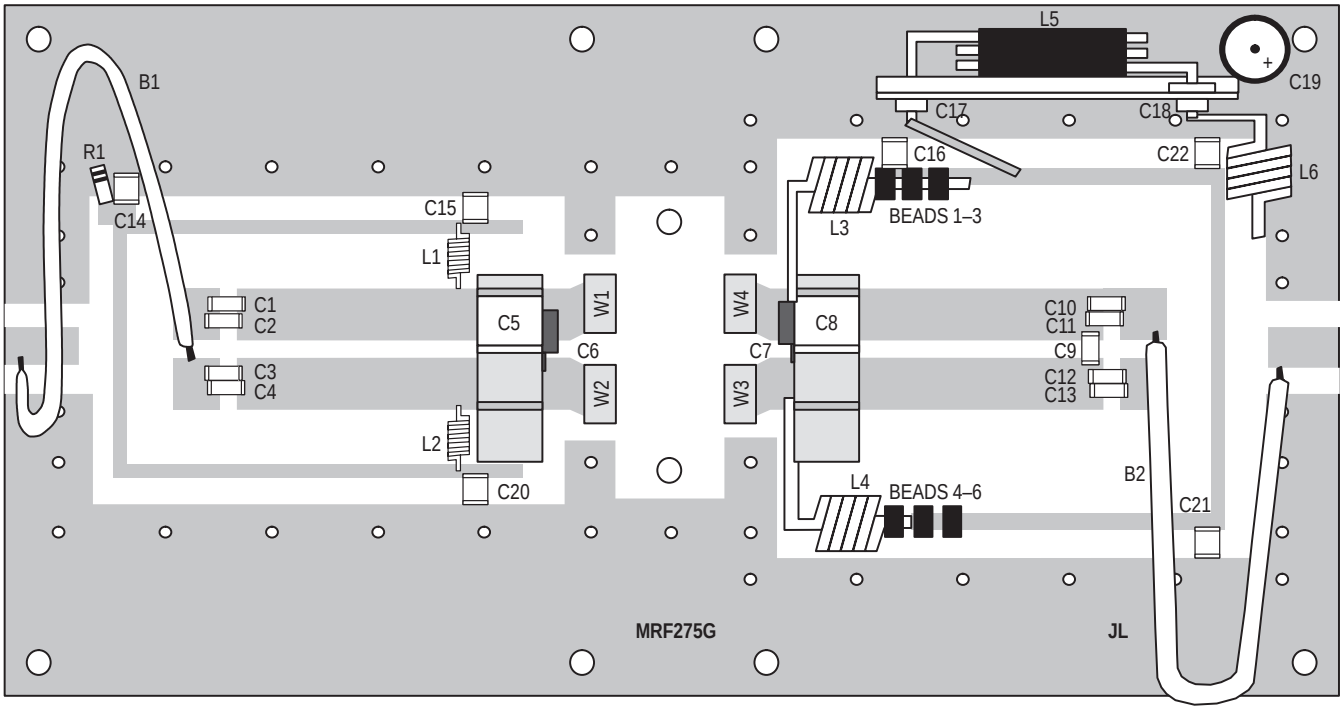
C1	8.0–60 pF, Arco 404
C2, C3, C7, C8	1000 pF, Chip Capacitor
C4, C9	0.1 μF, Chip Capacitor
C5	180 pF, Chip Capacitor
C6	100 pF and 130 pF, Chips in Parallel
C10	0.47 μF, Chip Capacitor, 1215 or Equivalent, Kemet
L1	10 Turns AWG #16, 1/4″ I.D., Enamel Wire, Close Wound
L2	Ferrite Beads of Suitable Material for 1.5–2.0 μH Total Inductance
Board material	062″ fiberglass (G10), $\varepsilon_r \cong 5$, Two sided, 1 oz. Copper.

Unless otherwise noted, all chip capacitors are ATC Type 100 or Equivalent.

R1	100 Ω, 1/2 W
R2	1.0 k Ω, 1/2 W
T1	4:1 Impedance Ratio, RF Transformer Can Be Made of 25 Ω, Semi Rigid Coax, 47–52 Mils O.D.
T2	1:9 Impedance Ratio, RF Transformer. Can Be Made of 15–18 Ω, Semi Rigid Coax, 62–90 Mils O.D.

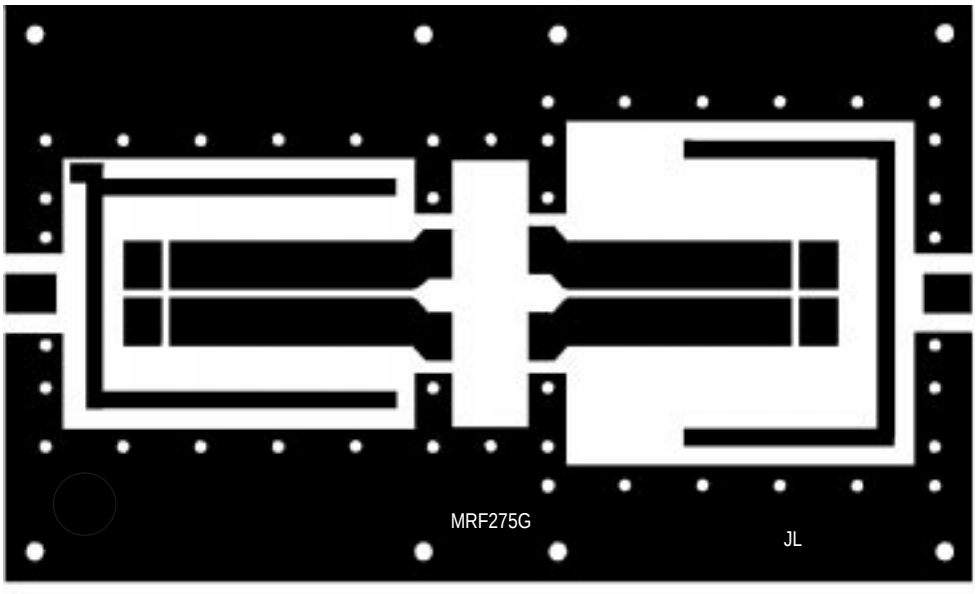
NOTE: For stability, the input transformer T1 should be loaded with ferrite toroids or beads to increase the common mode inductance. For operation below 100 MHz. The same is required for the output transformer.

Figure 13. 225 MHz Test Circuit



(Not to Scale)

Figure 14. MRF275G Component Location (500 MHz)



(Scale 1:1)

Figure 15. MRF275G Circuit Board Photo Master (500 MHz)

NOTE: S–Parameter data represents measurements taken from one chip only.

Table 1. Common Source S–Parameters (V_{DS} = 12 V, I_D = 4.5 A)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.822	–172	6.34	91	0.027	3	0.946	–173
40	0.846	–173	4.32	81	0.027	–6	0.859	–172
50	0.842	–174	3.62	79	0.027	–8	0.863	–175
60	0.838	–175	3.03	79	0.027	–5	0.923	–177
70	0.836	–175	2.76	80	0.028	–3	1.010	–178
80	0.841	–176	2.43	78	0.029	–4	1.080	–178
90	0.849	–176	2.19	74	0.029	–7	1.150	–176
100	0.857	–176	1.89	68	0.028	–13	1.110	–176
110	0.864	–176	1.66	63	0.026	–19	1.050	–177
120	0.868	–176	1.43	60	0.024	–19	0.958	–175
130	0.871	–176	1.25	59	0.023	–19	0.905	–176
140	0.874	–176	1.15	59	0.023	–17	0.914	–177
150	0.876	–176	1.11	59	0.023	–16	0.969	–178
160	0.880	–176	1.06	59	0.023	–17	1.060	–178
170	0.885	–177	1.01	55	0.023	–18	1.130	–177
180	0.891	–177	0.96	51	0.023	–23	1.190	–178
190	0.896	–177	0.87	45	0.022	–26	1.140	–179
200	0.900	–177	0.77	43	0.020	–26	1.050	–177
210	0.904	–177	0.69	42	0.018	–25	0.958	–176
220	0.907	–177	0.63	43	0.017	–23	0.924	–175
230	0.909	–177	0.60	43	0.018	–23	0.981	–178
240	0.912	–178	0.58	44	0.017	–22	0.981	–180
250	0.915	–178	0.58	42	0.017	–20	1.040	–179
260	0.918	–178	0.56	40	0.016	–20	1.150	–180
270	0.922	–178	0.54	34	0.015	–24	1.170	179
280	0.925	–179	0.49	32	0.014	–27	1.130	–180
290	0.927	–179	0.43	28	0.013	–27	1.010	–178
300	0.930	–179	0.41	30	0.013	–23	0.964	–178
310	0.932	–179	0.40	32	0.013	–14	0.936	–178
320	0.934	–180	0.39	31	0.012	–9	0.948	180
330	0.936	–180	0.35	32	0.011	–9	1.000	180
340	0.938	180	0.38	31	0.011	–12	1.070	178
350	0.941	180	0.35	28	0.011	–12	1.100	180
360	0.943	179	0.33	23	0.011	–10	1.120	–180
370	0.944	179	0.30	21	0.011	–4	1.080	180
380	0.945	179	0.29	21	0.009	1	1.020	180
390	0.947	179	0.28	22	0.008	3	0.966	–180
400	0.948	179	0.26	25	0.008	4	0.936	–179
410	0.949	178	0.26	24	0.010	5	1.010	179
420	0.951	178	0.25	25	0.010	11	1.040	178

Table 1. Common Source S–Parameters (V_{DS} = 12 V, I_D = 4.5 A) continued

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
430	0.952	178	0.25	22	0.010	19	1.080	177
440	0.953	177	0.24	19	0.009	22	1.100	178
450	0.955	177	0.24	16	0.008	21	1.100	179
460	0.956	177	0.21	15	0.008	11	1.080	177
470	0.956	177	0.20	16	0.009	16	0.992	178
480	0.957	176	0.19	18	0.010	27	0.975	179
490	0.958	176	0.19	18	0.010	40	0.974	178
500	0.960	176	0.19	19	0.010	46	1.010	177
600	0.956	175	0.18	12	0.007	49	0.940	175
700	0.958	172	0.11	14	0.018	61	0.989	173
800	0.962	170	0.10	12	0.029	51	0.967	172
900	0.965	168	0.08	16	0.021	72	0.973	170
1000	0.964	165	0.07	12	0.021	57	1.010	168

Table 2. Common Source S–Parameters (V_{DS} = 24 V, I_D = 0.35 mA)

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.829	–170	9.20	92	0.023	4	0.915	–171
40	0.858	–172	6.30	83	0.022	–4	0.834	–170
50	0.852	–173	5.28	80	0.023	–6	0.836	–174
60	0.846	–174	4.42	80	0.023	–3	0.892	–175
70	0.843	–175	4.01	81	0.024	–1	0.978	–177
80	0.847	–175	3.53	80	0.024	–2	1.050	–177
90	0.855	–175	3.18	76	0.024	–5	1.110	–176
100	0.865	–176	2.75	70	0.023	–10	1.080	–175
110	0.872	–176	2.43	65	0.022	–16	1.020	–176
120	0.874	–176	2.10	62	0.020	–16	0.932	–174
130	0.876	–176	1.84	61	0.019	–15	0.882	–175
140	0.878	–176	1.70	61	0.019	–14	0.889	–176
150	0.880	–176	1.63	61	0.019	–13	0.943	–177
160	0.883	–176	1.56	61	0.019	–13	1.030	–177
170	0.888	–177	1.49	58	0.019	–14	1.100	–176
180	0.894	–177	1.42	53	0.019	–18	1.160	–176
190	0.899	–177	1.29	47	0.018	–22	1.120	–177
200	0.902	–177	1.14	45	0.017	–24	1.030	–176
210	0.905	–177	1.02	44	0.015	–23	0.941	–175
220	0.907	–177	0.94	46	0.015	–19	0.903	–174
230	0.909	–178	0.89	45	0.015	–16	0.957	–177
240	0.912	–178	0.87	46	0.014	–15	0.961	–179
250	0.915	–178	0.86	44	0.014	–15	1.020	–178
260	0.918	–178	0.83	42	0.014	–17	1.120	–178
270	0.922	–178	0.80	36	0.013	–19	1.140	–180

Table 2. Common Source S–Parameters (V_{DS} = 24 V, I_D = 0.35 mA) continued

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
280	0.925	–179	0.73	34	0.013	–20	1.110	–179
290	0.927	–179	0.65	32	0.011	–18	0.994	–177
300	0.929	–179	0.62	32	0.011	–15	0.948	–177
310	0.931	–179	0.60	34	0.010	–9	0.916	–177
320	0.932	–180	0.57	33	0.010	–6	0.934	–180
330	0.934	–180	0.53	34	0.010	–4	0.985	–180
340	0.937	180	0.56	33	0.010	–2	1.050	179
350	0.939	180	0.53	30	0.010	0	1.090	–179
360	0.941	179	0.50	25	0.010	0	1.110	–178
370	0.943	179	0.46	23	0.009	0	1.080	–179
380	0.944	179	0.44	22	0.009	2	1.010	–179
390	0.945	179	0.41	24	0.008	8	0.956	–179
400	0.946	178	0.40	27	0.008	16	0.926	–178
410	0.947	178	0.38	26	0.009	20	1.000	–180
420	0.949	178	0.38	26	0.009	22	1.040	179
430	0.950	178	0.37	23	0.009	25	1.070	179
440	0.952	177	0.36	21	0.009	26	1.090	180
450	0.953	177	0.36	18	0.009	28	1.090	–180
460	0.954	177	0.31	17	0.009	24	1.070	178
470	0.955	177	0.30	17	0.009	29	0.990	179
480	0.956	176	0.29	19	0.009	36	0.963	–179
490	0.957	176	0.29	20	0.010	45	0.959	180
500	0.958	176	0.28	20	0.010	50	0.996	178
600	0.956	175	0.24	12	0.006	90	0.924	176
700	0.959	172	0.16	13	0.019	63	0.986	174
800	0.963	170	0.14	10	0.023	63	0.963	173
900	0.968	168	0.12	11	0.026	84	0.967	171
1000	0.969	165	0.09	7	0.025	70	1.000	169

Table 3. Common Source S–Parameters (V_{DS} = 28 V, I_D = 0.39 mA)

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
30	0.834	–169	10.08	93	0.021	4	0.807	–171
40	0.863	–172	6.91	83	0.021	–4	0.828	–170
50	0.857	–173	5.79	81	0.021	–5	0.830	–173
60	0.851	–174	4.86	81	0.022	–3	0.883	–175
70	0.848	–175	4.41	82	0.022	–1	0.970	–177
80	0.852	–175	3.87	80	0.022	–1	1.040	–177
90	0.860	–175	3.49	77	0.023	–5	1.100	–176
100	0.869	–176	3.03	71	0.022	–9	1.070	–175
110	0.876	–176	2.68	66	0.021	–14	1.010	–176
120	0.878	–176	2.31	63	0.019	–14	0.923	–174
130	0.879	–176	2.03	62	0.018	–15	0.876	–175

Table 3. Common Source S–Parameters (V_{DS} = 28 V, I_D = 0.39 mA) continued

f	S_{11}		S_{21}		S_{12}		S_{22}	
MHz	$\|S_{11}\|$	ϕ	$\|S_{21}\|$	ϕ	$\|S_{12}\|$	ϕ	$\|S_{22}\|$	ϕ
140	0.881	–176	1.87	62	0.018	–13	0.884	–176
150	0.883	–176	1.79	62	0.018	–11	0.934	–177
160	0.886	–177	1.72	62	0.018	–11	1.020	–177
170	0.890	–177	1.64	58	0.018	–12	1.090	–176
180	0.896	–177	1.56	54	0.018	–16	1.150	–176
190	0.901	–177	1.42	48	0.018	–21	1.110	–177
200	0.904	–177	1.26	46	0.017	–19	1.030	–176
210	0.907	–177	1.13	45	0.015	–14	0.938	–175
220	0.908	–177	1.03	47	0.013	–13	0.897	–174
230	0.910	–178	0.99	46	0.014	–15	0.948	–176
240	0.912	–178	0.96	47	0.014	–13	0.956	–179
250	0.916	–178	0.95	45	0.014	–10	1.020	–178
260	0.919	–178	0.93	42	0.013	–12	1.120	–178
270	0.922	–179	0.89	37	0.012	–15	1.140	–179
280	0.925	–179	0.81	35	0.012	–16	1.110	–178
290	0.927	–179	0.72	33	0.011	–16	0.988	–176
300	0.929	–179	0.69	33	0.011	–10	0.944	–177
310	0.931	–179	0.66	35	0.012	5	0.920	–177
320	0.933	–180	0.63	34	0.011	16	0.936	–180
330	0.934	–180	0.59	35	0.009	14	0.989	–180
340	0.937	180	0.62	34	0.009	3	1.050	180
350	0.939	180	0.59	31	0.010	4	1.080	–179
360	0.941	179	0.55	26	0.010	8	1.110	–178
370	0.943	179	0.51	24	0.009	11	1.070	–179
380	0.944	179	0.49	23	0.008	17	1.010	–178
390	0.945	179	0.46	25	0.008	24	0.949	–178
400	0.946	178	0.44	27	0.007	20	0.922	–178
410	0.947	178	0.43	26	0.010	19	0.995	–180
420	0.949	178	0.42	27	0.012	29	1.030	179
430	0.950	178	0.41	24	0.010	41	1.060	179
440	0.951	177	0.40	21	0.008	40	1.090	180
450	0.953	177	0.39	19	0.008	34	1.090	–180
460	0.953	177	0.35	17	0.009	26	1.070	178
470	0.954	177	0.33	18	0.010	30	0.983	179
480	0.955	176	0.32	19	0.012	43	0.964	–180
490	0.956	176	0.32	20	0.012	60	0.956	179
500	0.957	176	0.31	21	0.010	65	0.993	178
600	0.955	174	0.26	13	0.012	67	0.926	176
700	0.958	172	0.18	12	0.018	64	0.984	174
800	0.963	170	0.15	9	0.020	89	0.961	173
900	0.966	168	0.13	9	0.028	81	0.967	171
1000	0.968	165	0.10	6	0.033	73	0.997	169

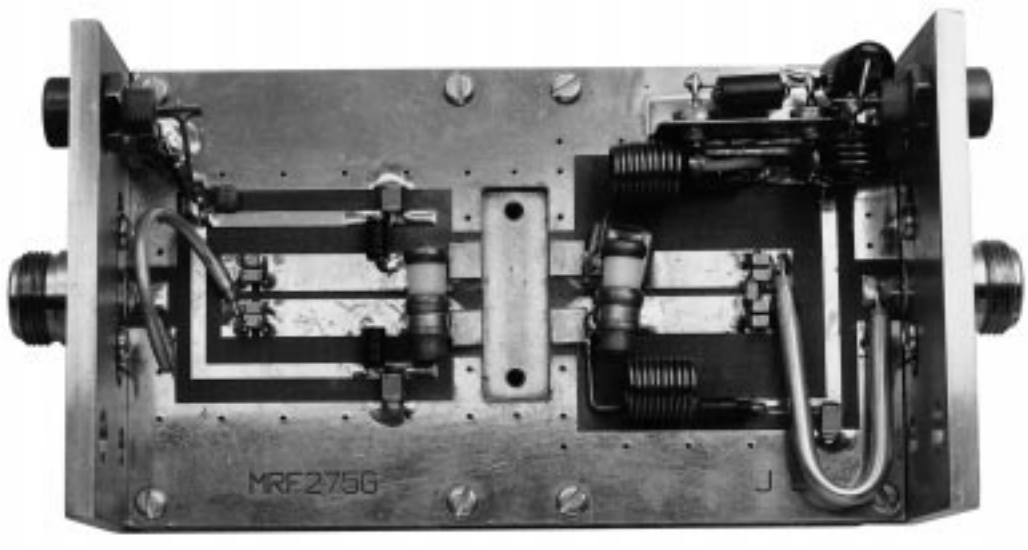


Figure 16. MRF275G Test Fixture

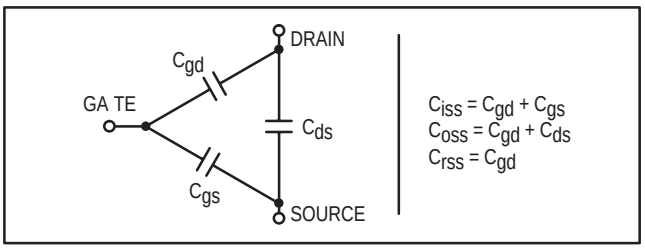
RF POWER MOSFET CONSIDERATIONS

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate–to–drain (C_{gd}), and gate–to–source (C_{gs}). The PN junction formed during the fabrication of the MOSFET results in a junction capacitance from drain–to–source (C_{ds}).

These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter–terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate. In the latter case the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



The C_{iss} given in the electrical characteristics table was measured using method 2 above. It should be noted that C_{iss}, C_{oss}, C_{rss} are measured at zero drain current and are provided for general information about the device. They are not RF design parameters and no attempt should be made to use them as such.

DRAIN CHARACTERISTICS

One figure of merit for a FET is its static resistance in the full–on condition. This on–resistance, $V_{DS(on)}$, occurs in the linear region of the output characteristic and is specified under specific test conditions for gate–source voltage and drain current. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient and constitutes an important design consideration at high temperatures, because it contributes to the power dissipation within the device.

GATE CHARACTERISTICS

The gate of the MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The input resistance is very high — on the order of 10^9 ohms — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage slightly in excess of the gate–to–source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating (or any of the maximum ratings on the front page). Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of this device are essentially capacitors. Circuits that leave the gate open–circuited or floating should be avoided. These conditions can result in turn–on of the devices due to voltage build–up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate–to–source. If gate protection is required, an external zener diode is recommended.

Using a resistor to keep the gate–to–source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate–drain capacitance. If the gate–to–source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate

may be large enough to exceed the gate–threshold voltage and turn the device on.

HANDLING CONSIDERATIONS

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with grounded equipment.

DESIGN CONSIDERATIONS

The MRF275G is a RF power N–channel enhancement mode field–effect transistor (FETs) designed for HF, VHF and UHF power amplifier applications. M/A-COM RF MOSFETs feature a vertical structure with a planar design.

M/A-COM Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal.

DC BIAS

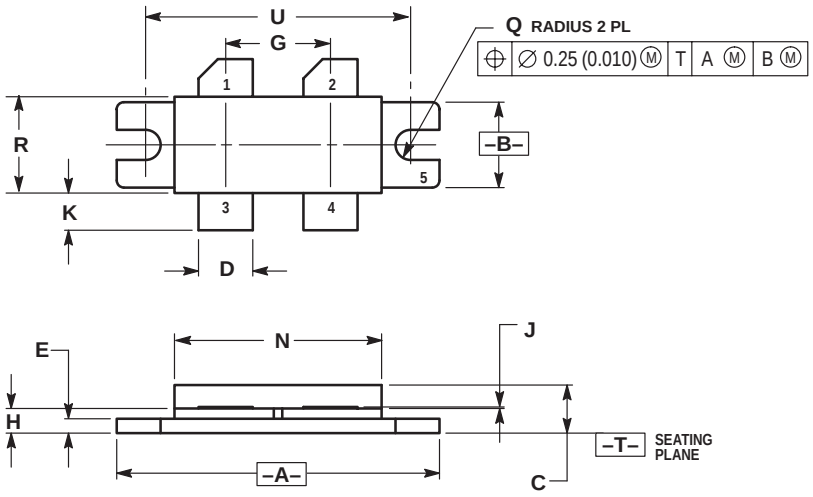
The MRF275G is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF275G was characterized at I_{DQ} = 100 mA, each side, which is the suggested minimum value of I_{DQ}. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may be just a simple resistive divider network. Some applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF275G may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.330	1.350	33.79	34.29
B	0.370	0.410	9.40	10.41
C	0.190	0.230	4.83	5.84
D	0.215	0.235	5.47	5.96
E	0.050	0.070	1.27	1.77
G	0.430	0.440	10.92	11.18
H	0.102	0.112	2.59	2.84
J	0.004	0.006	0.11	0.15
K	0.185	0.215	4.83	5.33
N	0.845	0.875	21.46	22.23
Q	0.060	0.070	1.52	1.78
R	0.390	0.410	9.91	10.41
U	1.100 BSC		27.94 BSC	

STYLE 2:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

CASE 375–04
ISSUE D

Specifications subject to change without notice.

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Visit www.macom.com for additional data sheets and product information.