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# **MSM7617**

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## **2-Channel Echo Canceler**

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### **GENERAL DESCRIPTION**

The MSM7617 cancels echoes (acoustic or line echoes) generated in voice channels. It is a low-power CMOS LSI device with two channels.

MSM7617 echo canceling is performed by digital signal processing. It negates echoes by estimating the echo channel and then generating a pseudo-echo signal.

When used as an acoustic echo canceler, the MSM7617 can cancel acoustic echoes between speaker and microphone that occur during hands-free speaking with car phones, conferencing system phones, etc. When used as a line echo canceler, the MSM7617 can cancel line echoes returned by hybrid impedance mismatches.

By setting its mode for use as a single cross-connected channel, the MSM7617 can cancel both acoustic and line echoes.

Also, the MSM7617 can improve voice communication by using its howling detection, double-talk detection, attenuation, and gain control functions to prevent and suppress howling levels, and by using its center clipping function to suppress low level noise.

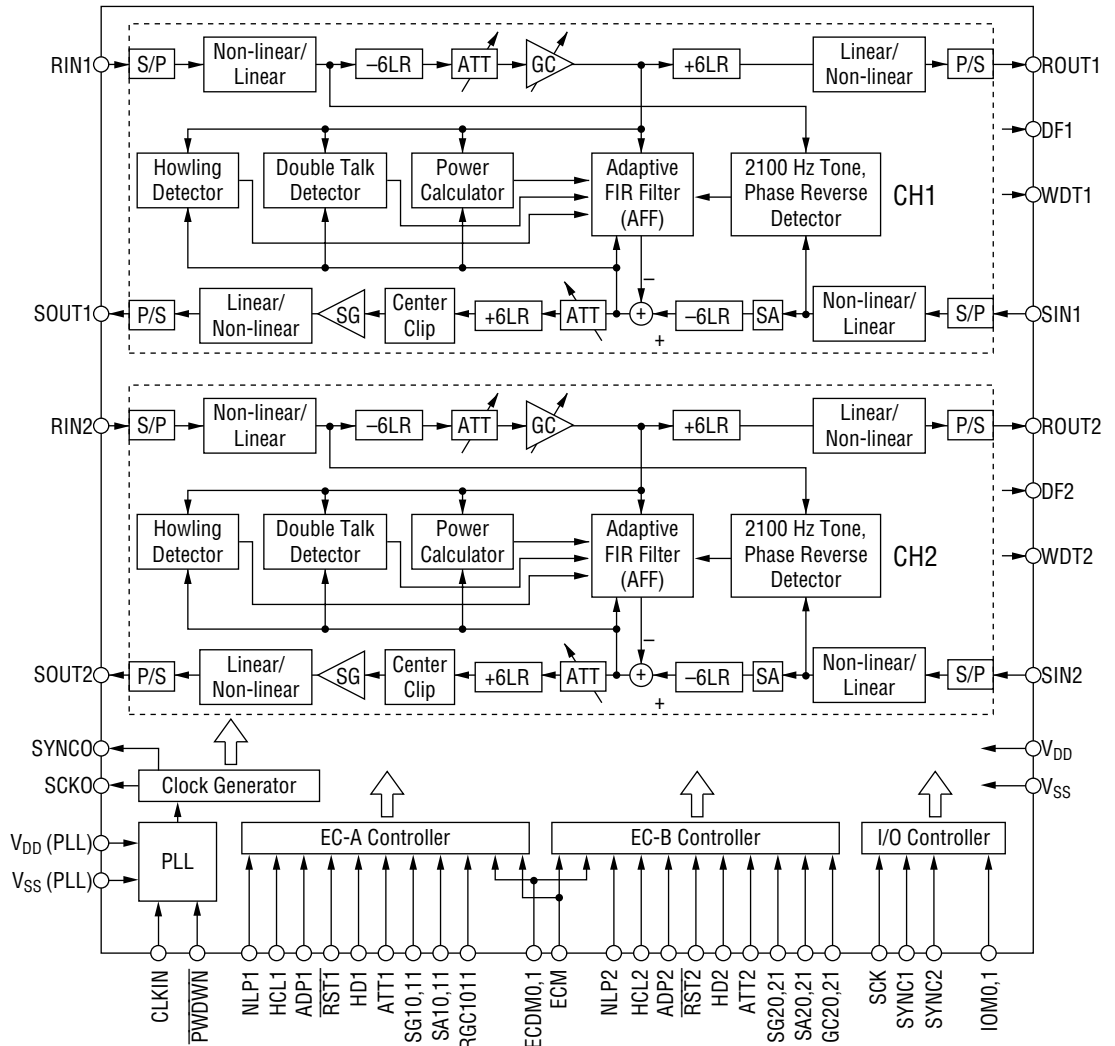
Furthermore, the MSM7617 can disable echo canceling during data communication with its 2100 Hz tone detector and 2100 Hz phase reversal detector. It also provides the ability to attenuate SIN levels, to amplify SOUT levels, and to adjust input/output levels.

An economical and highly efficient echo canceler unit can be constructed by using a 2-channel single-chip CODEC like the MSM7533 together with the MSM7617.

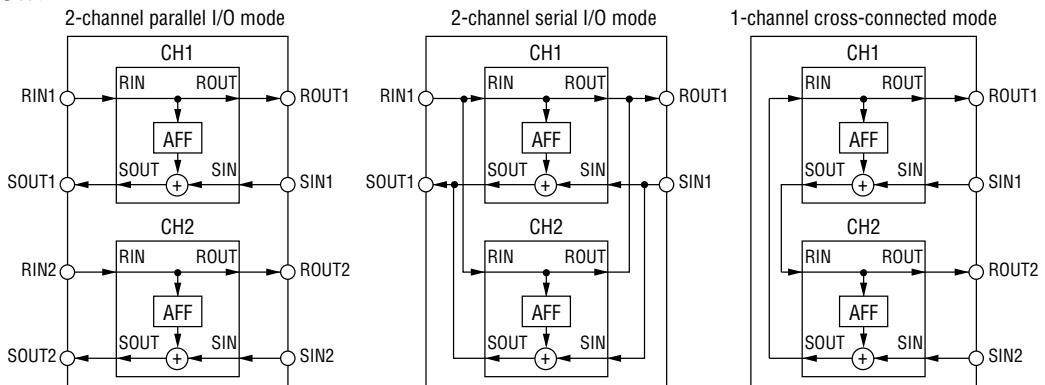
## FEATURES

- Echo canceler has two channels, which can be used for acoustic and line echoes. Set as a single cross-connected channel, it can be used for both acoustic and line echoes.
- ITU-T G164/G165 standard tone disabler.
- PCM line level adjustment possible with SIN level attenuator (SA pin) and SOUT level amplifier (SG pin). Can also be used for ERL amplification with the SIN level attenuator (SA pin).
- RGC pin provides input/output adjustment mode ( $\pm 6$ LR mode) that can prevent malfunction due to excessive inputs without changing the RIN-ROUT input/output levels.
- Cancelable echo delay time: 55 ms (max.)
- Echo attenuation: 30 dB (typ.)
- Clock frequency: 18 to 20 MHz  
19.2 MHz if using internal clock signal
- Power supply voltage: 4.5 to 5.5 V
- Package: 64-pin plastic QFP (QFP64-P-1414-0.80-BK)
- Product name: MSM7617-001GS-BK ( $\mu$ -law)

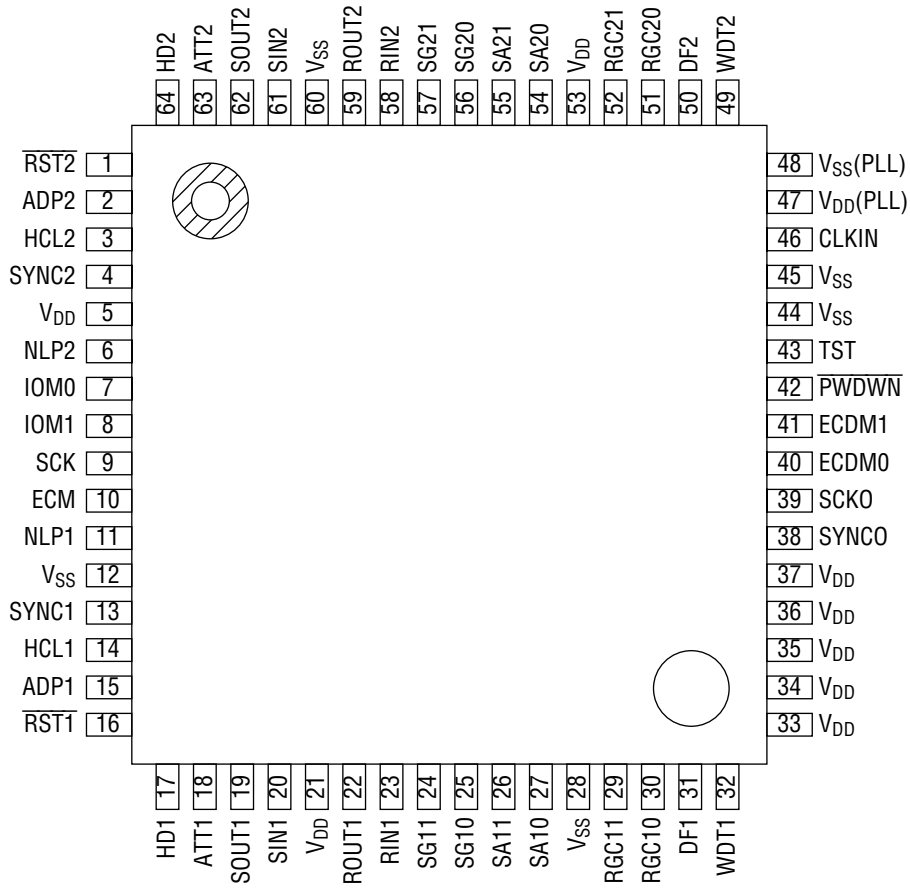
**BLOCK DIAGRAM**



The above diagram shows internal connections for 2-channel parallel mode. The internal connections for 2-channel serial I/O mode and 1-channel cross-connected mode are shown below.



**PIN CONFIGURATION (TOP VIEW)**



**64-Pin Plastic QFP**

**PIN DESCRIPTIONS**

Pin	Symbol	Type	Description															
1	RST2	I	<p>Reset signal input pin for channel 2.</p> <p>"L": Reset</p> <p>"H": Normal operation</p> <p>Input signals are invalid for 100 μs after reset (after RST returns to "H" from "L") for setting initial values.</p> <p>Input the basic clock during reset. Output pins will be placed in the following states during reset.</p> <p>Hi-Z: ROUT2, SOUT2</p> <p>No effect: SYNCO, SCKO, ROUT1, SOUT1, DF1, WDT1</p> <p>Previous state: DF2, WDT2</p>															
2	ADP2	I	<p>AFF coefficient control pin for channel 2.</p> <p>This pin stops coefficient variation of the adaptive FIR filter (AFF), fixing the coefficients. It allows once acquired AFF coefficients to be saved.</p> <p>"H": Fixed coefficient mode</p> <p>"L": Normal mode (variable coefficients)</p>															
3	HCL2	I	<p>Echo canceler disable pin for channel 2.</p> <p>This pin disables the echo canceler and enables data from SIN to SOUT to be output in "through mode". The input and output levels of SIN and SOUT are changed by the setting of the SG and SA pins; therefore, to output data from SIN to SOUT in "through mode", set the SA and SG pins to "0 dB".</p> <p>It simultaneously clears the adaptive FIR filter coefficients.</p> <p>"H": Disable mode</p> <p>"L": Normal mode (echo canceller enabled)</p>															
4	SYNC2	I	<p>Sync signal input pin for channel 2 transmit/receive PCM data while in parallel I/O mode.</p> <p>Input the transmit/receive sync signal (8 kHz) of the PCM CODEC connected to channel 2. Input "L" if not in parallel I/O mode.</p>															
6	NLP2	I	<p>NLP control pin for channel 2.</p> <p>This pin controls center clipping, forcing SOUT2 output to the minimum positive value when it is below -54 dBm0. It is effective for reducing uncanceled echoes and low-level noise.</p> <p>"H": Center clipping on</p> <p>"L": Center clipping off</p>															
7 8	IOM0 IOM1	I	<p>Sets I/O mode of PCM data.</p> <table border="1"> <thead> <tr> <th>IOM1</th> <th>IOM0</th> <th>Mode Setting</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>2-channel parallel I/O mode</td> </tr> <tr> <td>0</td> <td>1</td> <td>2-channel serial I/O mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>1-channel cross-connected mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>Inhibited</td> </tr> </tbody> </table>	IOM1	IOM0	Mode Setting	0	0	2-channel parallel I/O mode	0	1	2-channel serial I/O mode	1	0	1-channel cross-connected mode	1	1	Inhibited
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## PIN DESCRIPTIONS (Continued)

Pin	Symbol	Type	Description
9	SCK	I	Common pin for channel 1 and channel 2. Clock input pin for PCM data transmission. Input the same clock as the transmit/receive clock of the PCM CODEC. Frequencies below 128 kHz cannot be used in serial mode.
10	ECM	I	Not used. Fix input to "H".
11	NLP1	I	NLP control pin for channel 1. This pin controls center clipping, forcing SOUT1 output to the minimum positive value when it is below -54 dBm0. It is effective for reducing uncanceled echoes and low-level noise. "H": Center clipping on "L": Center clipping off
13	SYNC1	I	Sync signal input pin for channel 1 transmit/receive PCM data while in 2-channel parallel I/O mode, 2-channel serial I/O mode, or 1-channel cross-connected mode. Input the transmit/receive sync signal (8 kHz) of the PCM CODEC.
14	HCL1	I	Echo canceler disable control pin for channel 1. This pin disables the echo canceler and enables data from SIN to SOUT to be output in "through mode". The input and output levels of SIN and SOUT are changed by the setting of the SG and SA pins; therefore, to output data from SIN to SOUT in "through mode", set the SA and SG pins to "0 dB". It simultaneously clears the adaptive FIR filter coefficients. "H": Disable mode "L": Normal mode (echo canceler enabled)
15	ADP1	I	AFF coefficient control pin for channel 1. This pin stops coefficient variation of the adaptive FIR filter (AFF), fixing the coefficients. It allows once acquired AFF coefficients to be saved. "H": Fixed coefficient mode "L": Normal mode (variable coefficients)
16	$\overline{\text{RST1}}$	I	Reset signal input pin for channel 1. "L": Reset "H": Normal operation Input signals are invalid for 100 $\mu\text{s}$ after reset (after $\overline{\text{RST1}}$ returns to "H" from "L") for setting initial values. Input the base clock during reset. Output pins will be placed in the following states during reset. Hi-Z: ROUT1, SOUT1 No effect: SYNC0, SCKO, ROUT2, SOUT2, DF2, WDT2 Previous state: DF1, WDT1

**PIN DESCRIPTIONS (Continued)**

<b>Pin</b>	<b>Symbol</b>	<b>Type</b>	<b>Description</b>
17	HD1	I	<p>Howling detection control pin for channel 1.</p> <p>This pin controls detection and canceling of howling generated by the acoustics of handsfree telephones.</p> <p>"L": Howling detector on  "H": Howling detector off</p>
18	ATT1	I	<p>ATT control pin for channel 1.</p> <p>This pin controls the ATT function for preventing howling with the attenuators (ATT) provided on RIN and SOUT. When input is only on RIN, the SOUT attenuator is activated. When there is no input on RIN or there is input on both SIN and RIN, the RIN input attenuator is activated. Either the ATT for the RIN output or the ATT for the SOUT is always activated in all cases, and the attenuation of ATT is 6 dB.</p> <p>"H": Attenuator off  "L": Attenuator on</p> <p>Because the attenuator is inserted opposite the speaker, it is effective for further reducing echo.</p>
19	SOUT1	O	<p>PCM data output pin. Output signal changes depending on the setting of the IOM pins (refer to the block diagram).</p> <p>Data is always output on the rising edge of SCK. This pin is put in high impedance state while there is no data or during reset.</p> <p>In 2-channel parallel I/O mode, this pin becomes SOUT for channel 1 and outputs the PCM signal synchronous with SYNC1. In 2-channel serial I/O mode, this pin outputs the SOUT signal as a multiplexed PCM signal of SOUT signal for channel 1 and channel 2 synchronous with SYNC1.</p> <p>In 1-channel cross-connected mode, this pin becomes high impedance.</p>

**PIN DESCRIPTIONS (Continued)**

<b>Pin</b>	<b>Symbol</b>	<b>Type</b>	<b>Description</b>
20	SIN1	I	<p>PCM data input pin. Pin use changes depending on the setting of the IOM pins (refer to the block diagram).</p> <p>In 2-channel parallel I/O mode, this pin becomes SIN for channel 1 and inputs the PCM signal synchronous with SYNC1. In 2-channel serial I/O mode, this pin sequentially inputs SIN as a multiplexed PCM signal from channel 1 and channel 2 synchronous with SYNC1. In 1-channel cross-connected mode, this pin becomes the cross-connected SIN pin for channel 1, and inputs the PCM signal synchronous with SYNC1.</p> <p>Data is captured on the falling edge of SCK.</p>
22	ROUT1	O	<p>PCM data output pin. Output signal changes depending on the setting of the IOM pins (refer to the block diagram).</p> <p>Data is always output on the rising edge of SCK. This pin becomes high impedance while there is no data or during reset.</p> <p>In 2-channel parallel I/O mode, this pin becomes ROUT for channel 1 and outputs the PCM signal synchronous with SYNC1. In 2-channel serial I/O mode, this pin outputs the ROUT signal as a multiplexed PCM signal of ROUT signals for channel 1 and channel 2 synchronous with SYNC1.</p> <p>In 1-channel cross-connected mode, this pin becomes the cross-connected ROUT pin for channel 1, and outputs the PCM signal synchronous with SYNC1.</p>
23	RIN1	I	<p>PCM data input pin. Pin use changes depending on the setting of the IOM pins (refer to the block diagram).</p> <p>In 2-channel parallel I/O mode, this pin becomes RIN for channel 1 and inputs the PCM signal synchronous with SYNC1. In 2-channel serial I/O mode, this pin sequentially inputs RIN as a multiplexed PCM signal from channel 1 and channel 2 synchronous with SYNC1. In 1-channel cross-connected mode, this pin is not used, and should be fixed at "L".</p> <p>Data is captured on the falling edge of SCK.</p>



**PIN DESCRIPTIONS (Continued)**

Pin	Symbol	Type	Description															
24 25	SG11 SG10	I	<p>S output gain control pins for channel 1 (refer to the block diagram). These pins amplify the output level of SOUT. The gain level can be set even during the echo canceler disable mode.</p> <table border="1"> <thead> <tr> <th>SG11</th> <th>SG10</th> <th>Gain Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0 dB</td> </tr> <tr> <td>0</td> <td>1</td> <td>+6 dB</td> </tr> <tr> <td>1</td> <td>0</td> <td>+12 dB</td> </tr> <tr> <td>1</td> <td>1</td> <td>Not used</td> </tr> </tbody> </table>	SG11	SG10	Gain Level	0	0	0 dB	0	1	+6 dB	1	0	+12 dB	1	1	Not used
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26 27	SA11 SA10	I	<p>S input attenuator control pins for channel 1 (refer to the block diagram). These pins attenuate the input level of SIN. Use them if ERL is large. The attenuation level can be set even during the echo canceler disable mode.</p> <table border="1"> <thead> <tr> <th>SA11</th> <th>SA10</th> <th>Attenuation Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0 dB</td> </tr> <tr> <td>0</td> <td>1</td> <td>-6 dB</td> </tr> <tr> <td>1</td> <td>0</td> <td>-12 dB</td> </tr> <tr> <td>1</td> <td>1</td> <td>Not used</td> </tr> </tbody> </table>	SA11	SA10	Attenuation Level	0	0	0 dB	0	1	-6 dB	1	0	-12 dB	1	1	Not used
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29 30	RGC11 RGC10	I	<p>R input level control pins for channel 1 (refer to the block diagram). Excessive input (PCM level is at maximum value) causes a malfunction. Use these pins when there is a possibility of excessive input.</p> <table border="1"> <thead> <tr> <th>RGC11</th> <th>RGC10</th> <th>Level Control Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>GC: On (control level = -20 dBm0) By the R gain controller, levels from -20 to -11.5 dBm0 will be suppressed to -20 dBm0 and those above -11.5 dBm0 will always be attenuated by 8.5 dB. This is effective to prevent excessive input and howling for hands-free applications.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Inhibited</td> </tr> <tr> <td>1</td> <td>1</td> <td>±6LR: On Applies -6 dB to excessive inputs using the level adjuster provided on R and S I/O. Since +6 dB also is applied at the output, the total level will not change, making this effective against line echo.</td> </tr> </tbody> </table>	RGC11	RGC10	Level Control Mode	0	0	Off	0	1	GC: On (control level = -20 dBm0) By the R gain controller, levels from -20 to -11.5 dBm0 will be suppressed to -20 dBm0 and those above -11.5 dBm0 will always be attenuated by 8.5 dB. This is effective to prevent excessive input and howling for hands-free applications.	1	0	Inhibited	1	1	±6LR: On Applies -6 dB to excessive inputs using the level adjuster provided on R and S I/O. Since +6 dB also is applied at the output, the total level will not change, making this effective against line echo.
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**PIN DESCRIPTIONS (Continued)**

Pin	Symbol	Type	Description															
31	DF1	0	Tone disabler flag output pin for channel 1. This pin outputs a disable flag when the ECDM pins are used for tone disabler mode. "H": Echo canceler disabled "L": Echo canceler enabled															
32	WDT1	0	Not used. Leave this pin open.															
38	SYNCO	0	Output pin for internal SYNC signal (8 kHz). This pin is used as the transmit/receive synchronization signal for PCM signals. Connect it to the SYNC pin and PCM CODEC's synchronization signal pin. Leave this pin open if using an external SYNC.															
39	SCKO	0	Output pin for internal SCK signal (256 kHz). This pin is used for the transfer clock of PCM signals. Connect it to the PCM CODEC's synchronization signal pin. Leave open if using an external SYNC.															
40 41	ECDM0 ECDM1	I	Tone disabler control pin common to channel 1 and channel 2. These pins detect answer tones generated by modems (2100 Hz), and then disable the echo canceler. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>ECDM1</th> <th>ECDM0</th> <th>Tone Disabler Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>2100 Hz tone detection: On</td> </tr> <tr> <td>1</td> <td>0</td> <td>2100 Hz and phase reversal detection: On</td> </tr> <tr> <td>1</td> <td>1</td> <td>Inhibited</td> </tr> </tbody> </table>	ECDM1	ECDM0	Tone Disabler Mode	0	0	Off	0	1	2100 Hz tone detection: On	1	0	2100 Hz and phase reversal detection: On	1	1	Inhibited
ECDM1	ECDM0	Tone Disabler Mode																
0	0	Off																
0	1	2100 Hz tone detection: On																
1	0	2100 Hz and phase reversal detection: On																
1	1	Inhibited																
42	$\overline{\text{PWDWN}}$	I	Common pin for channel 1 and channel 2. This pin controls the power-down mode to reduce current consumption when the device is not being used. "L": Power down "H": Normal operation During power-down mode all input pins are invalid, and output pins will enter the following states. Hi-Z: SOUT1, SOUT2, ROUT1, ROUT2 "L": SYNCO, SCKO Previous state: DF1, WDT1, DF2, WDT2 Reset the device after power-down mode is released.															

**PIN DESCRIPTIONS (Continued)**

Pin	Symbol	Type	Description
43	TST	0	Not used. Leave this pin open.
46	CLKIN	I	Basic clock input pin. Input a clock 18 to 20 MHz. Use 19.2 MHz if using internal synchronization signals (SYNCO, SCKO).
47	V <sub>DD</sub> (PLL)	I	Power supply for PLL circuit that uses the basic clock. Insert a 0.1µF capacitor with excellent high frequency characteristics between V <sub>DD</sub> (PLL) and V <sub>SS</sub> (PLL).
48	V <sub>SS</sub> (PLL)	I	Ground for PLL circuit that uses the basic clock. Insert a 0.1µF capacitor with excellent high frequency characteristics between V <sub>DD</sub> (PLL) and V <sub>SS</sub> (PLL).
49	WDT2	0	Not used. Leave this pin open.
50	DF2	0	Tone disabler flag output pin for channel 2. This pin outputs a disable flag when the ECDM pins are used for tone disabler. "H": Echo canceler disabled "L": Echo canceler enabled
51 52	RGC20 RGC21	I	R input level control pins for channel 2 (refer to the block diagram). Excessive input (PCM level is at maximum value) causes a malfunction. Use these pins when there is a possibility of excessive input.
	RGC21	RGC20	Level Control Mode
	0	0	Off
	0	1	GC: On (control level = -20 dBm0) By the R gain controller, levels from -20 to -11.5 dBm0 will be suppressed to -20 dBm0 and those above -11.5 dBm0 will always be attenuated by 8.5 dB. This is effective to prevent excessive input and howling for hands-free applications.
	1	0	Inhibited
	1	1	±6LR: On Apply -6 dB to excessive inputs using the level adjuster provided on R and S I/O. Since +6 dB also is applied at the output, the total level will not change, making this effective against line echo.

**PIN DESCRIPTIONS (Continued)**

Pin	Symbol	Type	Description															
54 55	SA20 SA21	I	<p>S input attenuator control pins for channel 2 (refer to the block diagram). These pins attenuate the input level of SIN. Use them if ERL is large. The attenuation level can be set even during the echo canceler disable mode.</p> <table border="1"> <thead> <tr> <th>SA21</th> <th>SG20</th> <th>Attenuation Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0 dB</td> </tr> <tr> <td>0</td> <td>1</td> <td>-6 dB</td> </tr> <tr> <td>1</td> <td>0</td> <td>-12 dB</td> </tr> <tr> <td>1</td> <td>1</td> <td>Not used</td> </tr> </tbody> </table>	SA21	SG20	Attenuation Level	0	0	0 dB	0	1	-6 dB	1	0	-12 dB	1	1	Not used
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56 57	SG20 SG21	I	<p>S output gain control pins for channel 2 (refer to the block diagram). These pins amplify the output level of SOUT. The gain level can be set even during the echo canceler disable mode.</p> <table border="1"> <thead> <tr> <th>SG21</th> <th>SG20</th> <th>Gain Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0 dB</td> </tr> <tr> <td>0</td> <td>1</td> <td>+6 dB</td> </tr> <tr> <td>1</td> <td>0</td> <td>+12 dB</td> </tr> <tr> <td>1</td> <td>1</td> <td>Not used</td> </tr> </tbody> </table>	SG21	SG20	Gain Level	0	0	0 dB	0	1	+6 dB	1	0	+12 dB	1	1	Not used
SG21	SG20	Gain Level																
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58	RIN2	I	<p>PCM data input pin. Pin use changes depending on the setting of the IOM pins (refer to the block diagram). In 2-channel parallel I/O mode, this pin becomes RIN for channel 2 and inputs the PCM signal synchronous with SYNC2. Data is captured on the falling edge of SCK. In other modes, this pin is not used, and should be fixed at "L".</p>															
59	ROUT2	O	<p>PCM data output pin. Output signal changes depending on the setting of the IOM pins (refer to the block diagram). Data is always output on the rising edge of SCK. This pin becomes high impedance while there is no data. In 2-channel parallel I/O mode, this pin becomes ROUT for channel 2 and outputs the PCM signal synchronous with SYNC2. In 2-channel serial I/O mode, this pin is not used and should be left open. In 1-channel cross-connected mode, this pin becomes the cross-connected ROUT pin for channel 2, and outputs the PCM signal synchronous with SYNC1.</p>															

**PIN DESCRIPTIONS (Continued)**

<b>Pin</b>	<b>Symbol</b>	<b>Type</b>	<b>Description</b>
61	SIN2	I	PCM data input pin. Pin use changes depending on the setting of the IOM pins (refer to the block diagram). Data is captured on the falling edge of SCK. In 2-channel parallel I/O mode, this pin becomes SIN for channel 2 and inputs the PCM signal synchronous with SYNC2. In 2-channel serial I/O mode, this pin is not used and should be fixed at "L". In 1-channel cross-connected mode, this pin becomes the cross-connected SIN pin for channel 2, and inputs the PCM signal synchronous with SYNC1.
62	SOUT2	O	PCM data output pin. Output signal changes depending on the setting of the IOM pins (refer to the block diagram). Data is always output on the rising edge of SCK. This pin becomes high impedance while there is no data. In 2-channel parallel I/O mode, this pin becomes SOUT for channel 2 and outputs the PCM signal synchronous with SYNC2. In other modes, this pin is not used and should be left open.
63	ATT2	I	ATT control pin for channel 2. This pin controls the ATT function for preventing howling with the attenuators (ATT) provided on RIN and SOUT. When input is only on RIN, the SOUT attenuator is activated. When there is no input on SIN or there is input on both SIN and RIN, the RIN input attenuator is activated. Either the ATT for the RIN output or the ATT for the SOUT is always activated in all cases, and the attenuation of ATT is 6 dB. "H": Attenuator off "L": Attenuator on Because the attenuator is activated opposite the speaker, it is effective for further reducing echo.
64	HD2	I	Howling detection control pin for channel 2. This pin controls detection and canceling of howling generated by the acoustics of handsfree telephones. "L": Howling detector on "H": Howling detector off

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	$V_{DD}$	$T_a = 25^\circ\text{C}$	-0.3 to +7	V
Input Voltage	$V_{IN}$		-0.3 to $V_{DD} + 0.3$	V
Power Dissipation	$P_D$		1	W
Storage Temperature	$T_{STG}$	—	-55 to +150	$^\circ\text{C}$

**RECOMMENDED OPERATING CONDITIONS** $(V_{DD} = 4.5\text{ V to } 5.5\text{ V})$ 

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{DD}$	—	4.5	5	5.5	V
Power Supply Voltage	$V_{SS}$	—	—	0	—	V
High Level Input Voltage	$V_{IH}$	—	2.4	—	$V_{DD}$	V
Low Level Input Voltage	$V_{IL}$	—	0	—	0.8	V
Operating Temperature	$T_a$	—	-40	+25	+85	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS****DC Characteristics** $(V_{DD} = 4.5\text{ V to } 5.5\text{ V}, T_a = -40^\circ\text{C to } +85^\circ\text{C})$ 

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High Level Output Voltage	$V_{OH}$	$I_{OH} = 40\ \mu\text{A}$	4.2	—	$V_{DD}$	V
Low Level Output Voltage	$V_{OL}$	$I_{OL} = 1.6\ \text{mA}$	0	—	0.4	V
High Level Input Current	$I_{IH}$	$V_{IH} = V_{DD}$	—	0.1	10	$\mu\text{A}$
Low Level Input Current	$I_{IL}$	$V_{IL} = V_{SS}$	-10	-0.1	—	$\mu\text{A}$
High Level Output Leakage Current	$I_{OZH}$	$V_{OH} = V_{DD}$	—	0.1	10	$\mu\text{A}$
Low Level Output Leakage Current	$I_{OZL}$	$V_{OL} = V_{SS}$	-10	-0.1	—	$\mu\text{A}$
Power Supply Current (operation mode)	$I_{DDO}$	—	—	80	130	mA
Power Supply Current (power-down mode)	$I_{DDS}$	$\overline{\text{PWDWN}} = \text{"L"}$	—	0.5	2	mA
Input Capacitance	$C_i$	—	—	—	15	pF
Output Load Capacitance	$C_{LOAD}$	—	—	—	20	pF

**Echo Canceler Characteristics (refer to characteristics diagram)**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Echo Reduction (Common to Channel 1 and Channel 2)	L <sub>RES</sub>	R <sub>IN</sub> = -10 dBm0 (5 kHz white noise band) E. R. L. = 6 dB T <sub>D</sub> = 50 ms ATT, GC, NLP: OFF	—	30	—	dB
Cancelable Echo Delay Time (Common to Channel 1 and Channel 2)	T <sub>D</sub>	R <sub>IN</sub> = -10 dBm0 (5 kHz white noise band) E. R. L. = 6 dB ATT, GC, NLP: OFF	—	—	55	ms

**Tone Disabler Characteristics**

Parameter		Min.	Typ.	Max.	Unit
Tone Detection	Detection frequency	2075	2100	2125	Hz
	Detection level	-32	—	—	dBm0
	Detection time	380	—	—	ms
Phase Reversal Detection	Detection condition	2100Hz. 180° out-of-phase detected before and after 450±25ms.			
	Detection frequency	2075	2100	2125	Hz
	Detection level	-32	—	—	dBm0
	Phase reversal	135	180	225	°
Release	Detection level	—	—	-32	dBm0
	Release time	—	250	—	ms

AC Characteristics

(V<sub>DD</sub> = 4.5 V to 5.5 V, T<sub>a</sub> = -40°C to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock Frequency	f <sub>C</sub>	—	19.2	—	MHz
If Used Without Internal Sync Signal		18	—	20	
Clock Cycle Time	t <sub>MCK</sub>	—	52.08	—	ns
If Used Without Internal Sync Signal		50	—	55.56	
Clock Duty Cycle	t <sub>DMC</sub>	40	—	60	%
Clock High Level Pulse Width	t <sub>MCH</sub>	t <sub>MCK</sub> × 0.4	—	t <sub>MCK</sub> × 0.6	ns
Clock Low Level Pulse Width	t <sub>MCL</sub>	t <sub>MCK</sub> × 0.4	—	t <sub>MCK</sub> × 0.6	ns
Clock Rise Time	t <sub>r</sub>	—	—	5	ns
Clock Fall Time	t <sub>f</sub>	—	—	5	ns
Internal Sync Clock Output Time	t <sub>DCM</sub>	—	—	40	ns
Internal Sync Clock Frequency	f <sub>CO</sub>	—	256	—	kHz
Internal Sync Clock Cycle Time	t <sub>CO</sub>	—	3.9	—	μs
Internal Sync Clock Duty Cycle	t <sub>DCO</sub>	—	50	—	%
Internal Sync Signal Output Time	t <sub>DCC</sub>	—	—	5	ns
Internal Sync Signal Period	t <sub>CYO</sub>	—	125	—	μs
Internal Sync Signal Pulse Width	t <sub>WSO</sub>	—	t <sub>CO</sub>	—	μs
Transmit/Receive Sync Clock Frequency	f <sub>SCK</sub>	64	—	2048	kHz
In Serial I/O Mode		128	—	2048	
Transmit/Receive Sync Clock Cycle Time	t <sub>SCK</sub>	0.488	—	15.62	μs
In Serial I/O Mode		0.488	—	7.81	
Transmit/Receive Sync Clock Duty Cycle	t <sub>DSC</sub>	40	50	60	%
Transmit/Receive Sync Signal Period	t <sub>CYC</sub>	—	125	—	μs
Sync Timing	t <sub>XS</sub>	45	—	—	ns
	t <sub>SX</sub>	45	—	—	ns
Sync Signal Width	t <sub>WSY</sub>	t <sub>SCK</sub>	—	t <sub>CYC</sub> - t <sub>SCK</sub>	μs
Receive Signal Setup Time	t <sub>DS</sub>	45	—	—	ns
Receive Signal Hold Time	t <sub>DH</sub>	45	—	—	ns
Receive Signal Input Time	t <sub>ID</sub>	—	7t <sub>SCK</sub>	—	μs
In 2-Channel Serial Mode	t <sub>ID2</sub>	—	15t <sub>SCK</sub>	—	μs



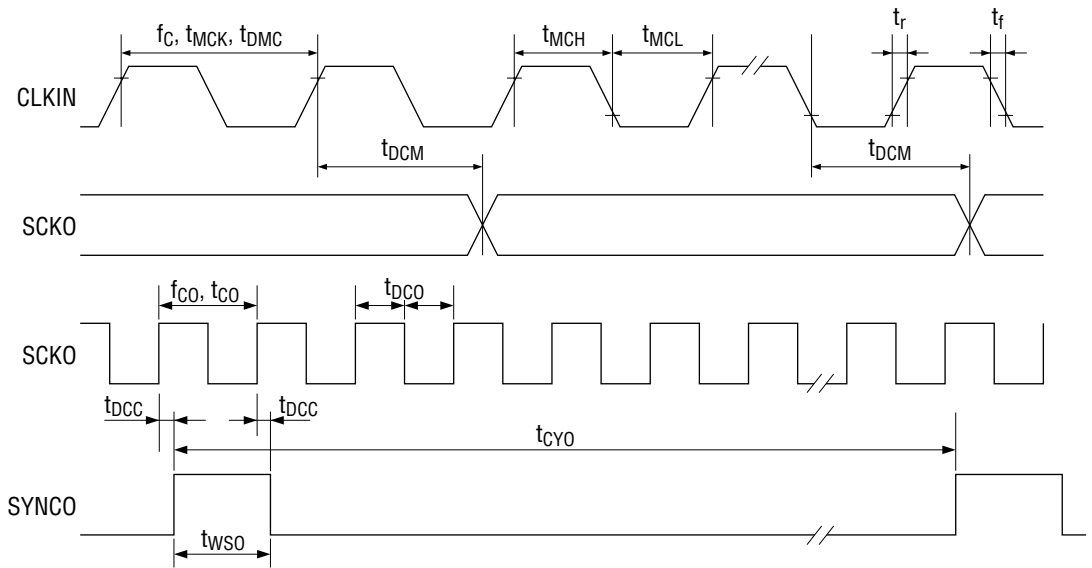
## AC Characteristics (Continued)

(V<sub>DD</sub> = 4.5 V to 5.5 V, T<sub>a</sub> = -40°C to +85°C)

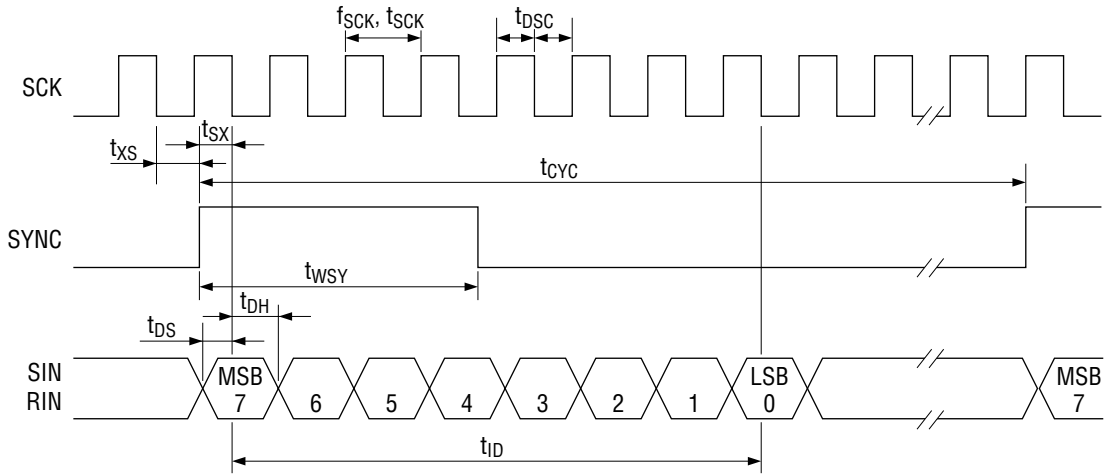
Parameter	Symbol	Min.	Typ.	Max.	Unit
Serial Output Delay Time	t <sub>SD</sub>	—	—	90	ns
	t <sub>XD</sub>	—	—	90	ns
Reset Signal Input Width	t <sub>WR</sub>	1	—	—	μs
Reset Start Time	t <sub>DRS</sub>	5	—	—	ns
Reset End Time	t <sub>DRE</sub>	—	—	52	ns
Process Operation Start Time	t <sub>DIT</sub>	100	—	—	μs
Power-Down Start Time	t <sub>DPS</sub>	—	—	111	ns
Power-Down End Time	t <sub>DPE</sub>	—	—	15	ns
RST Width After Power-Down	t <sub>WPR</sub>	10	—	—	μs
$\overline{\text{RST}}$ Control Pin Setup Time	t <sub>DSR</sub>	20	—	—	ns
$\overline{\text{RST}}$ Control Pin Hold Time	t <sub>DHR</sub>	20	—	—	ns
SCK Control Pin Setup Time	t <sub>DCS</sub>	120	—	—	ns
SCK Control Pin Hold Time	t <sub>DCH</sub>	120	—	—	ns

**TIMING DIAGRAMS**

**Clock Timing**

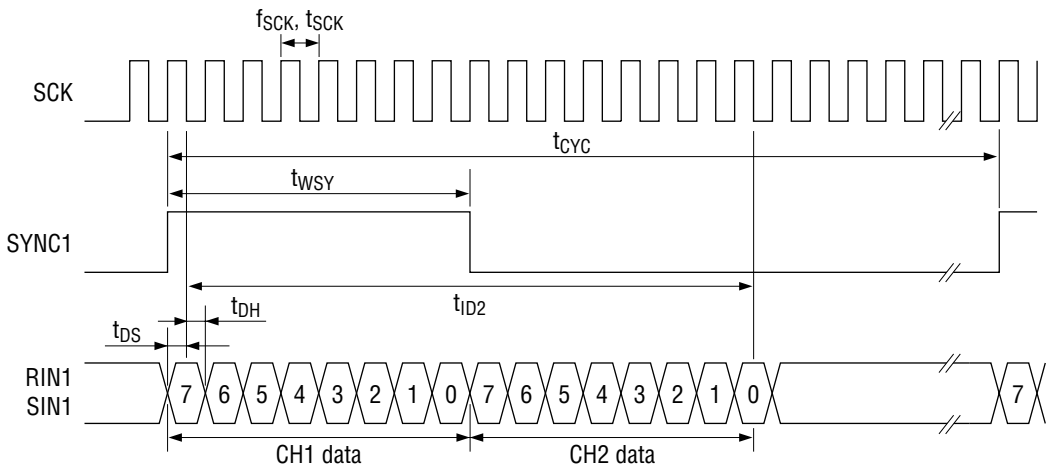


**Serial Data Input Timing (Parallel Mode, FTF Mode)**

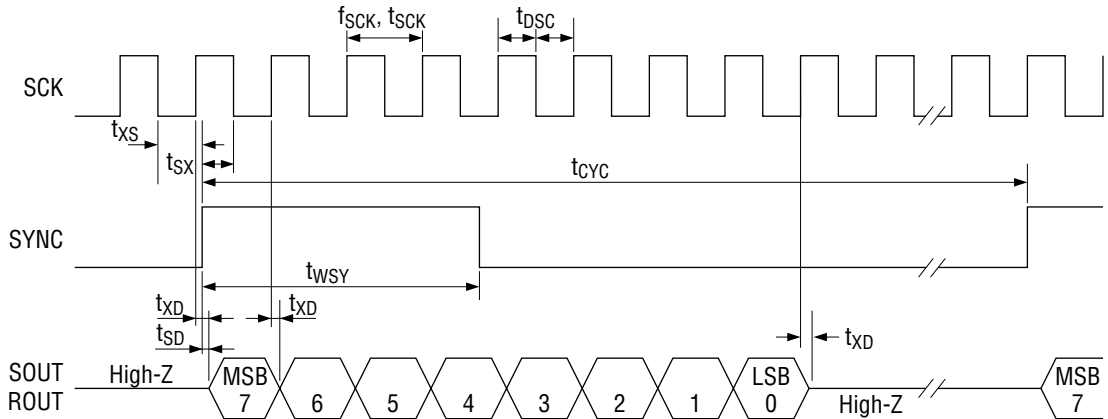


**Serial Data Input Timing (Serial Mode)**

Note: Refer to parallel mode for detailed timing

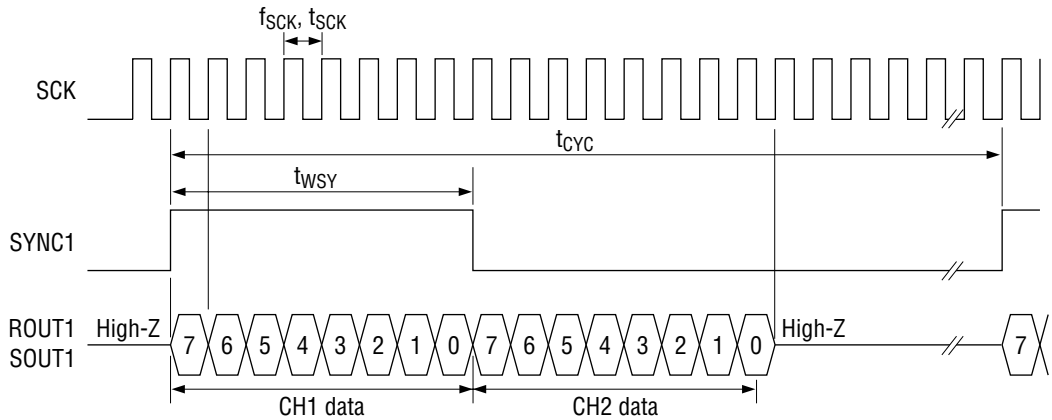


**Serial Data Output Timing (Parallel Mode, FTF Mode)**

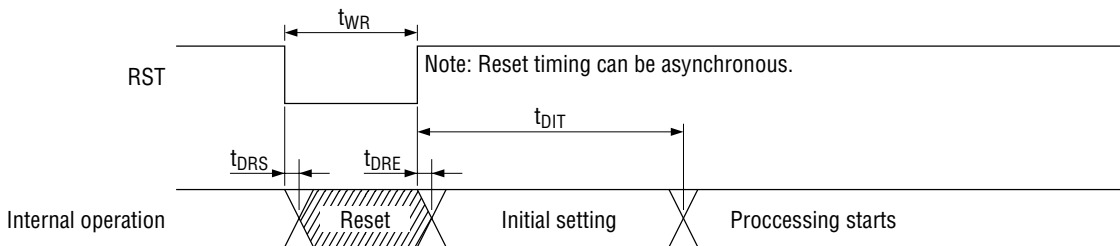


**Serial Data Output Timing (Serial Mode)**

Note: Refer to parallel mode for detailed timing

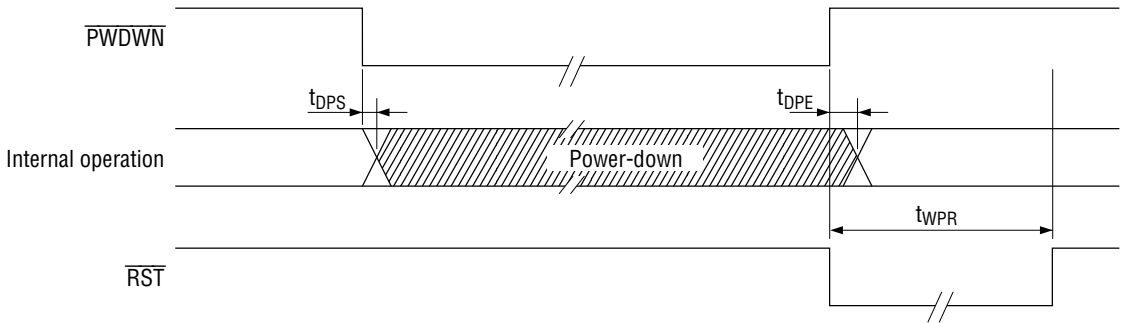


**Operation Timing After Reset**



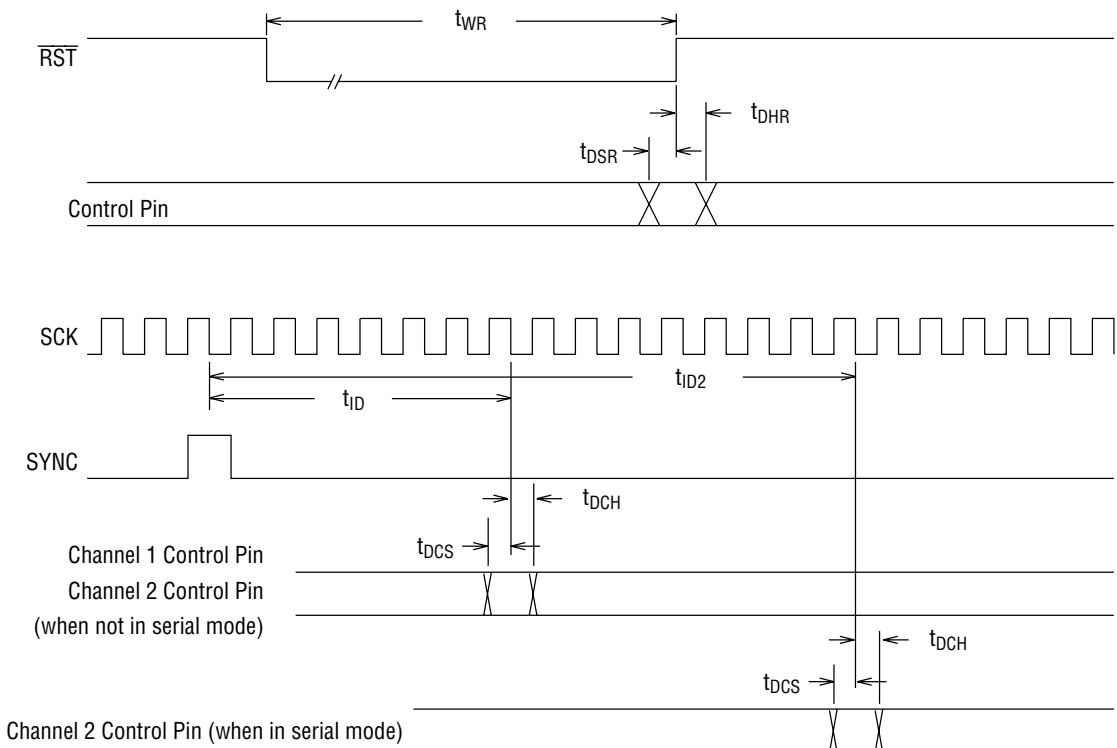
### Power-Down Timing

Note: All inputs are invalid during power-down. Always reset the device after power-down.



### Capture Timing of Control Pins

Control pin states are captured during reset and during each period's serial data capture.

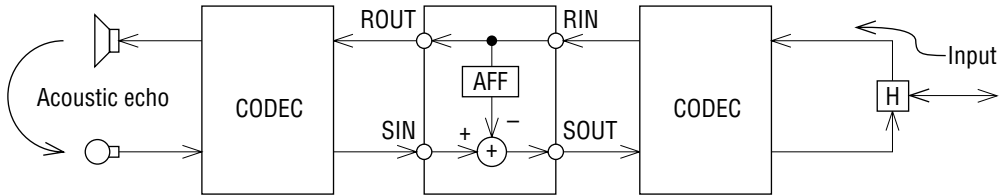


## HOW TO USE THE MSM7617

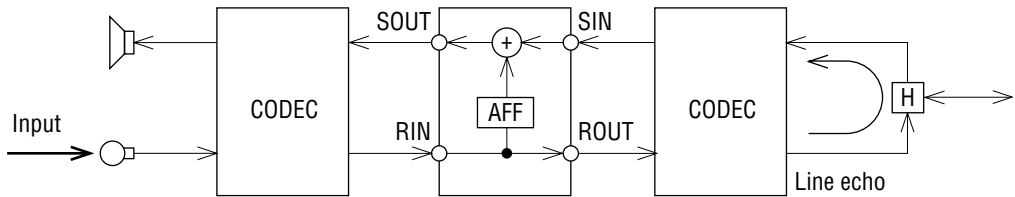
The echo canceler cancels the echo on the RIN signal as returned by SIN. Connect the original signal to the R side, and the signal generating the echo to the S side.

### Connection Methods According to Echoes

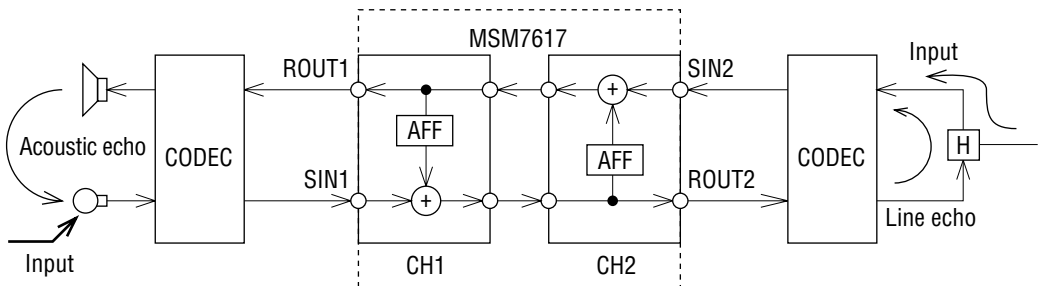
Example 1. Cancel Acoustic Echo (applies to acoustic echo from line input)



Example 2. Cancel Line Echo (applies to line echo from microphone input)

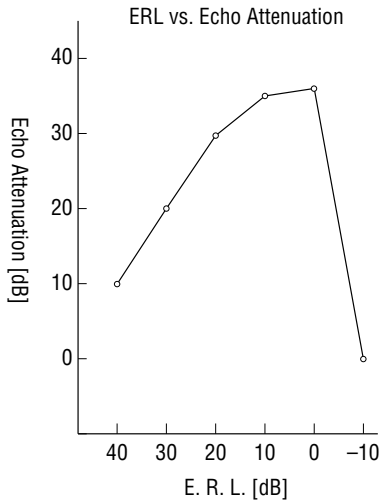


Example 3. Cancel Both Acoustic Echo And Line Echo

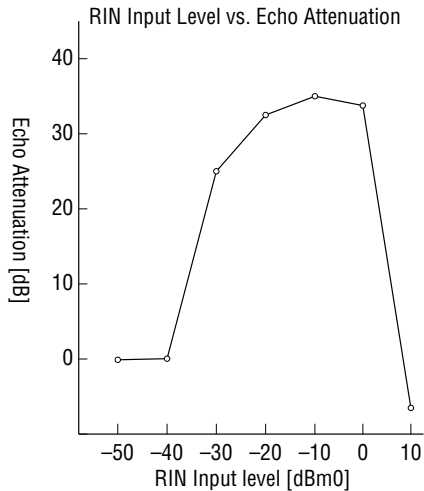


### ECHO CANCELER CHARACTERISTICS DIAGRAM

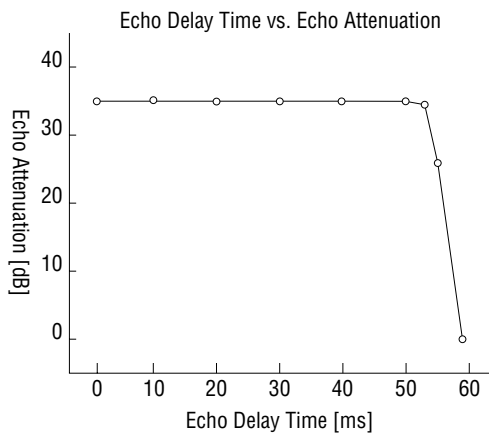
Characteristics of  $\mu$ -law and A-law are identical. (Characteristic graphs below are reference data.)



Measuring Conditions:  
 RIN input level = -10 dBm0 white noise  
 Echo delay time = 50 ms  
 ATT, GC, NLP, LR all off



Measuring Conditions:  
 RIN input = white noise  
 Echo delay time = 50 ms  
 E.R.L. = 6 [dB]  
 ATT, GC, NLP, LR all off



Measuring Conditions:  
 RIN input level = -10 dBm0 white noise  
 Echo delay time = 50 ms  
 E.R.L. = 6 dB  
 ATT, GC, NLP, LR all off

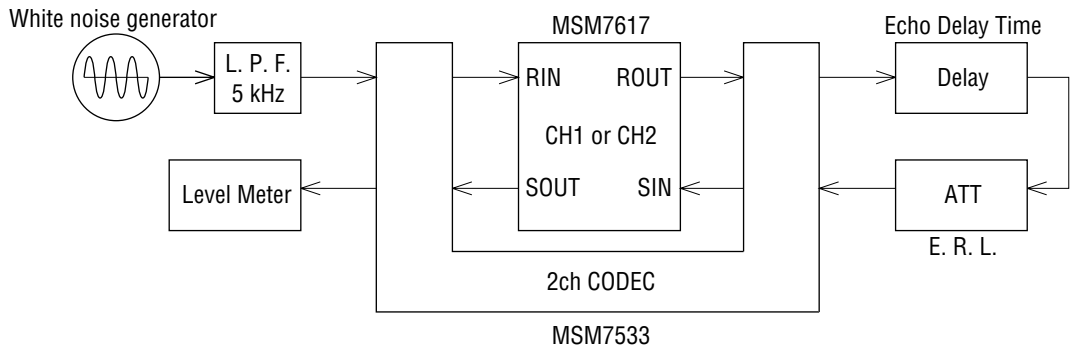
Note: regarding dBm0:

The "dBm0" unit used in the characteristic graphs is a unit that expresses PCM CODEC digital values. Therefore, be aware that the same value 0 [dBm0] might correspond to different analog input levels depending on the PCM CODEC being used. Please check the data sheet of the PCM CODEC being used.

Example MSM7533      0 [dBm0] = 0.85 [Vrms] = 2.4 [Vp-p] = 0.8 [dBm] 600  $\Omega$   
                              -10 [dBm0] = 0.27 [Vrms] = 0.76 [Vp-p] = -9.2 [dBm] 600  $\Omega$

MSM7543      0 [dBm0] = 0.6007 [Vrms] = 1.7 [Vp-p] = -2.2 [dBm] 600  $\Omega$   
                              -10 [dBm0] = 0.19 [Vrms] = 0.54 [Vp-p] = -12.2 [dBm] 600  $\Omega$

Measurement System Block Diagram





## NOTES ON USE

1. Set echo return loss (E. R. L) to be attenuated. If the echo return loss is set to be amplified, the echo cannot be canceled. (Refer to the "E. R. L vs Echo Attenuation" characteristic graph.)

When the echo return loss is amplified, adjust the input level to be attenuated by setting the mode with the SA pin. If the level from the SA pin is too low by setting the mode with the SA pin, then amplify the output level by setting the mode with the SG pin.

2. Set RIN input so that there is not excessive input (above 0 dBm0) from the PCM CODEC. Echo cancellation is not possible with excessive input. (Refer to the "RIN vs Echo Attenuation" characteristic graph.)

Recommended input levels are -10 to -20 dBm0. If there is a possibility of excessive input, then set GC mode or 6LR mode with the RGC pins.

3. Applying the tone signals to this echo canceler will decrease echo attenuation.
4. For changes in the echo path (retransmit, circuit switching during transmission, and so on), convergence may be difficult.  
Perform a reset to make it converge.  
If the state of the echo path changes after a reset, convergence may again be difficult.  
In cases such as a change in the echo path, perform a reset each time.
5. If a clock is not input after power is applied, then the internal circuits will not stabilize, possibly damaging the device.

When power is applied, set the  $\overline{\text{PVDWN}}$  pin to "H" and input the basic clock.

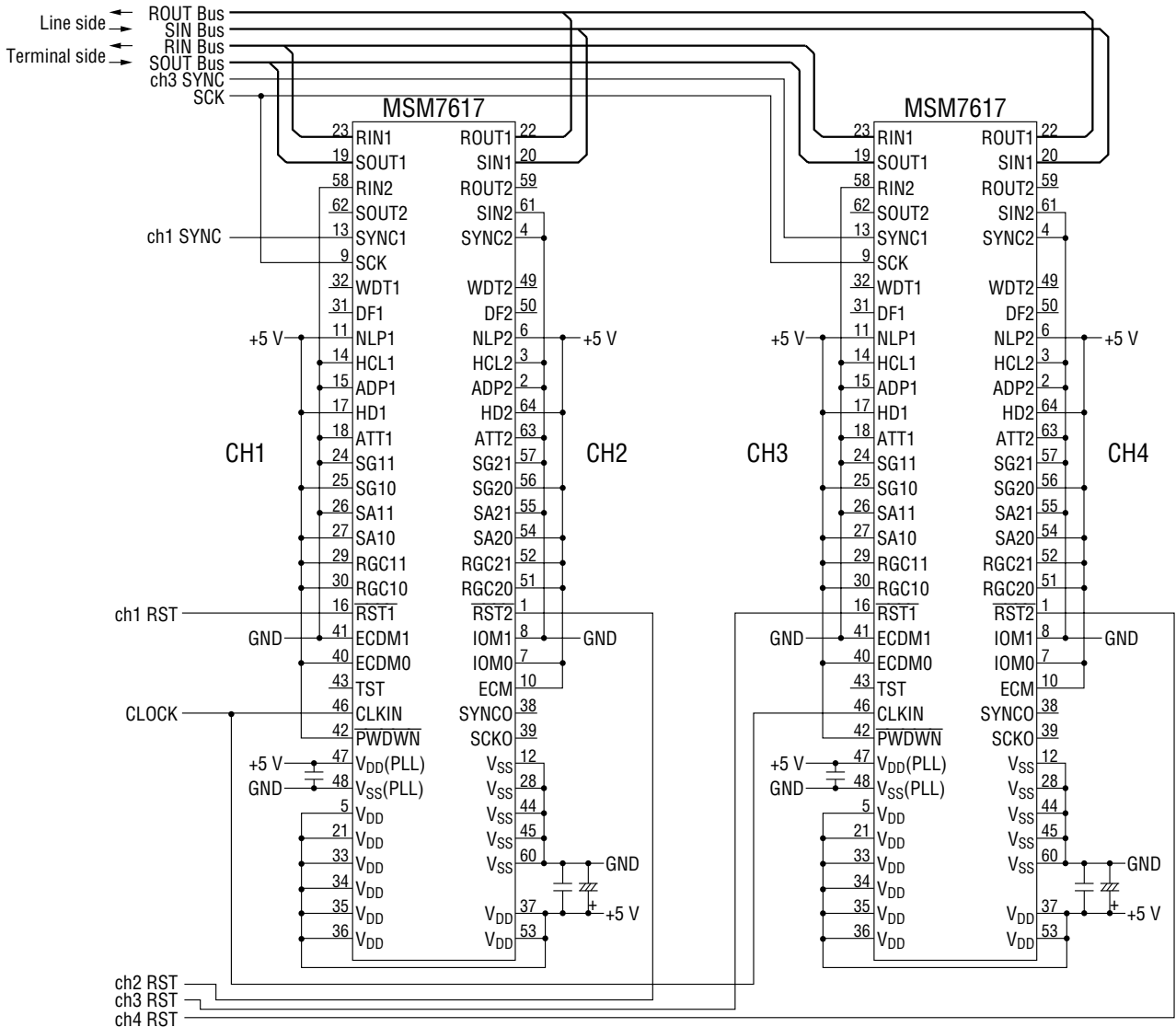
If the device is put into  $\overline{\text{PVDWN}}$  immediately after power has been applied, be sure to input 10 or more clocks of the basic clock before setting to the power down mode.

6. Always reset after power is applied or power-down is released.  
For power-on reset operation, an external oscillator may require a certain setting time after powered on. Allow 10  $\mu\text{s}$  for a reset time after the oscillator has settled.
7. When the device is used as an acoustic echo canceler, equipment noise and environment noise from the microphone amp may be amplified, and echo attenuation may be below 30 dB.

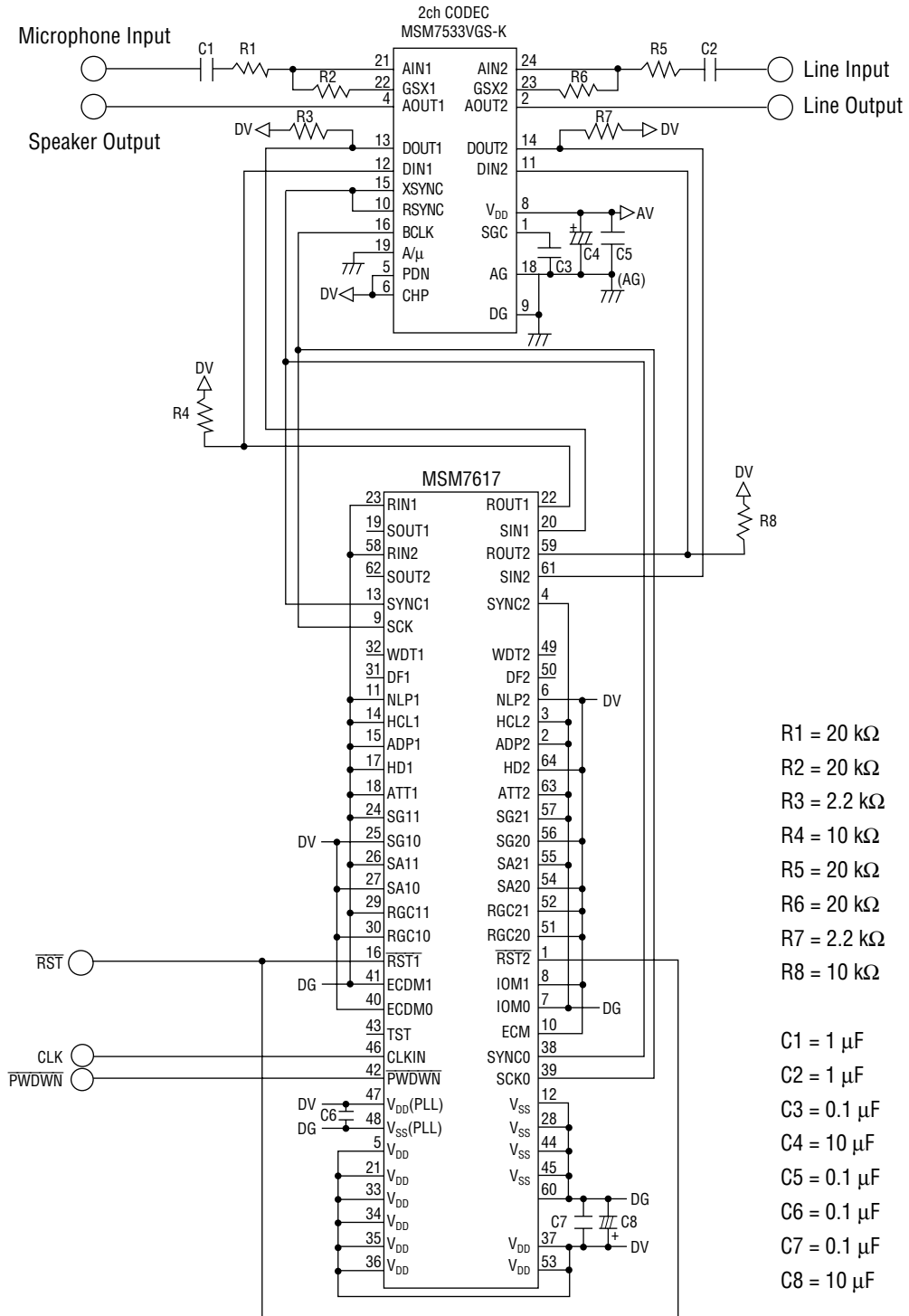
**APPLICATION CIRCUITS**

**4-Channel Serial Interface**

Line Echo Canceler Example

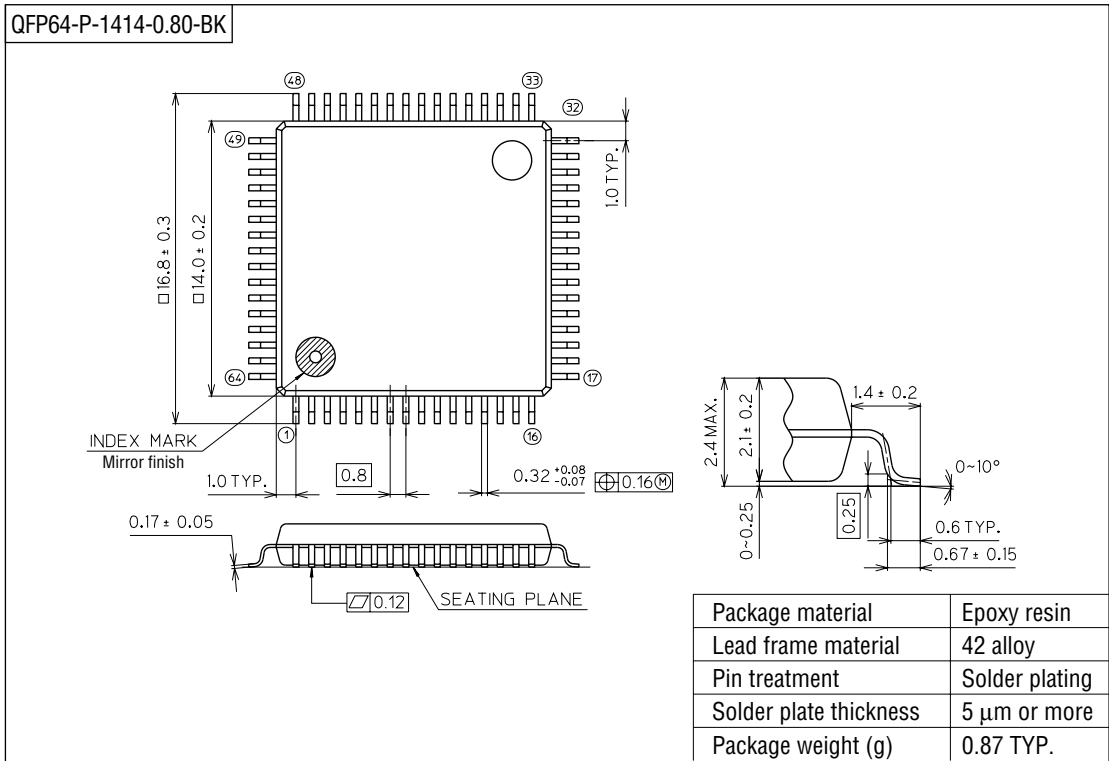


Cross-Connection Example



**PACKAGE DIMENSIONS**

(Unit : mm)



**Notes for Mounting the Surface Mount Type Package**

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
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