# MYSON TECHNOLOGY

# MTD505 (Preliminary)

## 5 Port 10M/100M Ethernet Switch

## FEATURES

- IEEE802.3 and IEEE802.3u compliant.
- Provide 4 RMII and 1 MII/RMII ports.
- Programmable 1K/8K MAC addresses filtering.
- Store and forward switching function and bad packet filtering function.
- Optional back_pressure/802.3x flow control/ flooding control/broadcast control.
- Optional EEPROM Interface for advanced switch configurations.
- 1MB/2MB SGRAM/SDRAM flexible memory interface.
- Port VLAN/trunking.
- Link/Rx activity, packet buffer utilization LED display.
- 50MHz for non-blocking for 5 ports switch operation
- Build in internal/external memory test function.
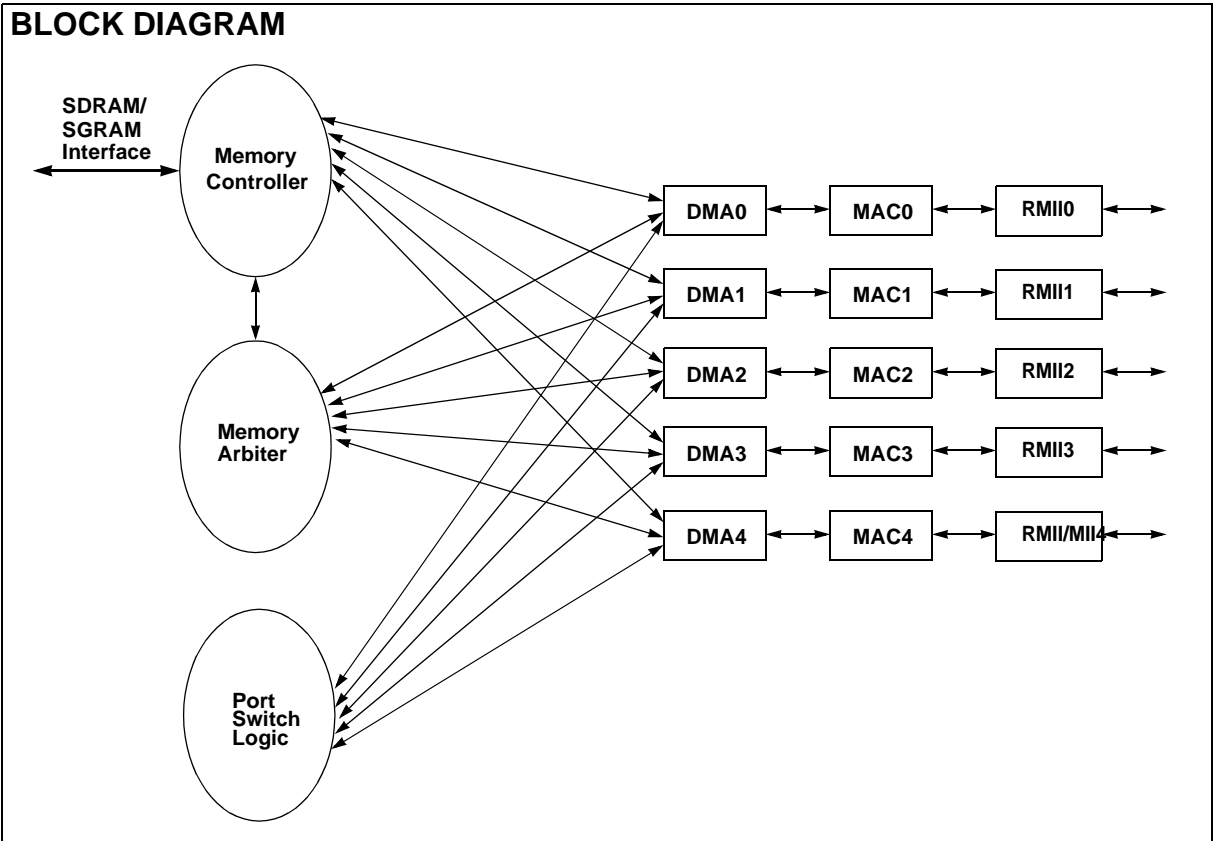- 128 pin PQFP package, 3.3V operation voltage.

## GENERAL DESCRIPTION

The MTD505 complies fully with the IEEE802.3, 802.3u and 802.3x specifications and is a non-blocking 5 port 10M/100M Ethernet switch device.

Support 4 RMII and 1 MII/RMII ports for 10M/100M operation. 1MByte/2MBytes memory interface provides maximum 1365 packet buffers for Ethernet packet buffering. Up to 8192 address entrys are provided by the MTD505, and the MTD505 use full Ethernet address compare algorithm to minimize hashing collision events.
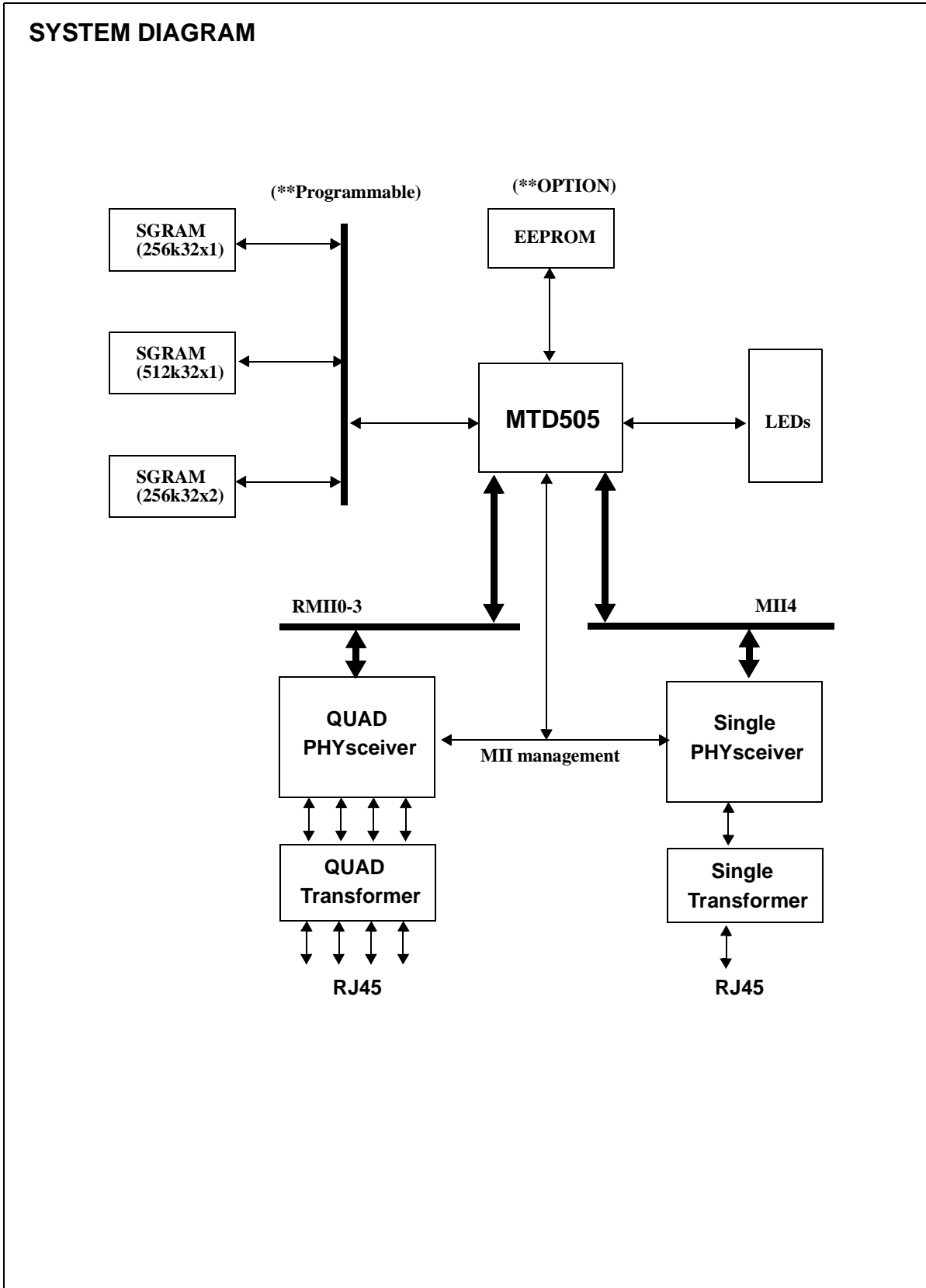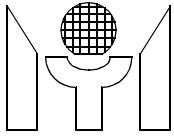
The MTD505 provides EEPROM interface to config port trunking, port VLAN, static entry, 802.3x flow control threshold, flooding port, broadcast control threshold. Each MTD505 port support 10/100M auto-negotiation by MDC/MDIO interface for connecting external PHY devices.

The MTD505 also provides 10 pins for Link/RX activity, packet buffer utilization LED display function.

## BLOCK DIAGRAM

# MYSON TECHNOLOGY

# MTD505
# (Preliminary)

## SYSTEM DIAGRAM

(**Programmable)   (**OPTION)

| SGRAM (256k32x1) | ←→ |
| SGRAM (512k32x1) | ←→ |
| SGRAM (256k32x2) | ←→ |

EEPROM

MTD505

LEDs

RMII0-3

MII4

QUAD PHYsceiver ←→ MII management ←→ Single PHYsceiver

QUAD Transformer

Single Transformer

RJ45

RJ45

## 1.0 PIN CONNECTION

Left side pins (top to bottom):

| Pin | Name |
|-----|------|
| 103 | LEDDATA4 |
| 104 | LEDDATA3 |
| 105 | LEDDATA2 |
| 106 | LEDDATA1 |
| 107 | LEDDATA0 |
| 108 | GNDI |
| 109 | CLK25M |
| 110 | VCCI |
| 111 | SDC |
| 112 | SDIO |
| 113 | EECLK |
| 114 | EEDATA |
| 115 | RESETB |
| 116 | REFCLK |
| 117 | MDIO |
| 118 | MDC |
| 119 | CRSDV0 |
| 120 | TXD0_1 |
| 121 | TXD0_0 |
| 122 | TXEN0 |
| 123 | RXD0_0 |
| 124 | RXD0_1 |
| 125 | CRSDV1 |
| 126 | TXD1_1 |
| 127 | TXD1_0 |
| 128 | TXEN1 |

Right side pins (top to bottom):

| Pin | Name |
|-----|------|
| 64 | VCCO |
| 63 | GNDO |
| 62 | AD5 |
| 61 | AD6 |
| 60 | AD7 |
| 59 | AD8 |
| 58 | VCCI |
| 57 | MEMCLK |
| 56 | GNDI |
| 55 | DQ8 |
| 54 | DQ9 |
| 53 | DQ10 |
| 52 | DQ11 |
| 51 | DQ12 |
| 50 | DQ13 |
| 49 | DQ14 |
| 48 | DQ15 |
| 47 | DQ24 |
| 46 | DQ25 |
| 45 | DQ26 |
| 44 | VCCO |
| 43 | GNDO |
| 42 | DQ27 |
| 41 | DQ28 |
| 40 | DQ29 |
| 39 | DQ30 |

Top side pins (left pin 102 to right pin 65):

| Pin | Name |
|-----|------|
| 102 | LEDDATA5 |
| 101 | LEDDATA6 |
| 100 | LEDDATA7 |
| 99 | VCCO |
| 98 | GNDO |
| 97 | LEDCLK2 |
| 96 | LEDCLK1 |
| 95 | DO0 |
| 94 | DO1 |
| 93 | DO2 |
| 92 | DO3 |
| 91 | DO4 |
| 90 | DO5 |
| 89 | DO6 |
| 88 | DO7 |
| 87 | DO16 |
| 86 | DO17 |
| 85 | DO18 |
| 84 | DO19 |
| 83 | DO20 |
| 82 | VCCO |
| 81 | GNDO |
| 80 | DO21 |
| 79 | DO22 |
| 78 | DO23 |
| 77 | WEB |
| 76 | CASB |
| 75 | RASB |
| 74 | CS0B |
| 73 | BA |
| 72 | VCCI |
| 71 | GNDI |
| 70 | CS1B |
| 69 | AD0 |
| 68 | AD1 |
| 67 | AD2 |
| 66 | AD3 |
| 65 | AD4 |

Bottom side pins (left pin 001 to right pin 38):

| Pin | Name |
|-----|------|
| 001 | RXD1_0 |
| 002 | RXD1_1 |
| 003 | CRSDV2 |
| 004 | TXD2_1 |
| 005 | TXD2_0 |
| 006 | TXEN2 |
| 007 | GNDO |
| 008 | VCCO |
| 009 | RXD2_0 |
| 010 | RXD2_1 |
| 011 | CRSDV3 |
| 012 | TXD3_1 |
| 013 | TXD3_0 |
| 014 | TXEN3 |
| 015 | RXD3_0 |
| 016 | RXD3_1 |
| 017 | CRSDV4 |
| 018 | COL4 |
| 019 | TXD4_3 |
| 020 | TXD4_2 |
| 021 | TXD4_1 |
| 022 | TXD4_0 |
| 023 | TXEN4 |
| 024 | TXC4 |
| 025 | RXC4 |
| 026 | RXDV4 |
| 027 | VCCI |
| 028 | GNDI |
| 029 | RXD4_0 |
| 030 | RXD4_1 |
| 031 | RXD4_2 |
| 032 | RXD4_3 |
| 033 | VCCI |
| 034 | GNDI |
| 035 | GNDI |
| 036 | SYSCLK |
| 037 | VCCI |
| 038 | DQ31 |

**MTD505**

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# MTD505
## (Preliminary)

## 2.0 PIN DESCRIPTIONS

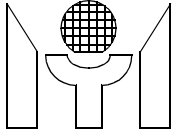| Name | Pin Number | I/O | Descriptions |
|---|---|---|---|
| RMII/MII Port Interface Pins | | | |
| CRSDV0 | 119 | I | Port0 RMII receive interface signal, CRSDV0 is asserted high when port0 media is non_idle. |
| RXD0_0 | 123 | I | Port0 RMII receive data bit_0. |
| RXD0_1 | 124 | I | Port0 RMII receive data bit_1. |
| TXEN0 | 122 | O | Port0 RMII transmit enable signal. |
| TXD0_0 | 121 | O | Port0 RMII transmit data bit_0. |
| TXD0_1 | 120 | O | Port0 RMII transmit data bit_1. |
| CRSDV1 | 125 | I | Port1 RMII receive interface signal, CRSDV1 is asserted high when port1 media is non_idle. |
| RXD1_0 | 01 | I | Port1 RMII receive data bit_0. |
| RXD1_1 | 02 | I | Port1 RMII receive data bit_1. |
| TXEN1 | 128 | O | Port1 RMII transmit enable signal. |
| TXD1_0 | 127 | O | Port1 RMII transmit data bit_0. |
| TXD1_1 | 126 | O | Port1 RMII transmit data bit_1. |
| CRSDV2 | 03 | I | Port2 RMII receive interface signal, CRSDV2 is asserted high when port2 media is non_idle. |
| RXD2_0 | 09 | I | Port2 RMII receive data bit_0. |
| RXD2_1 | 10 | I | Port2 RMII receive data bit_1. |
| TXEN2 | 06 | O | Port2 RMII transmit enable signal. |
| TXD2_0 | 05 | O | Port2 RMII transmit data bit_0. |
| TXD2_1 | 04 | O | Port2 RMII transmit data bit_1. |
| CRSDV3 | 11 | I | Port3 RMII receive interface signal, CRSDV0 is asserted high when port3 media is non_idle. |
| RXD3_0 | 15 | I | Port3 RMII receive data bit_0. |
| RXD3_1 | 16 | I | Port3 RMII receive data bit_1. |
| TXEN3 | 14 | O | Port3 RMII transmit enable signal. |
| TXD3_0 | 13 | O | Port3 RMII transmit data bit_0. |
| TXD3_1 | 12 | O | Port3 RMII transmit data bit_1. |
| CRSDV4 | 17 | I | Port4 RMII/MII receive interface signal, CRSDV4 is asserted high when port4 media is non_idle. |
| RXDV4 | 26 | I | Port4 MII receive data valid. In RMII mode, this pin don't use. |
| RXCLK4 | 25 | I | Port4 MII receive clock signal. In RMII mode, this pin is not used. |
| RXD4_3 | 32 | I | Port4 MII receive data bit_3. In RMII mode, this pin don't use. |
| RXD4_2 | 31 | I | Port4 MII receive data bit_2. In RMII mode, this pin don't use. |
| RXD4_0 | 29 | I | Port4 RMII/MII receive data bit_0. |
| RXD4_1 | 30 | I | Port4 RMII/MII receive data bit_1. |
| TXEN4 | 23 | O | Port4 RMII transmit enable signal. |
| TXCLK4 | 24 | I | Port4 RMII transmit clock signal. In RMII mode, this pin is not used. |

| RMII/MII Port Interface Pins | | | |
|---|---|---|---|
| **Name** | **Pin Number** | **I/O** | **Descriptions** |
| TXD4_3 | 19 | O | Port4 MII transmit data bit_3. In RMII mode, this pin don't use. |
| TXD4_2 | 20 | O | Port4 MII transmit data bit_2. In RMII mode, this pin don't use. |
| TXD4_0 | 22 | O | Port4 RMII/MII transmit data bit_0. |
| TXD4_1 | 21 | O | Port4 RMII/MII transmit data bit_1. |
| COL4 | 18 | I | Port4 MII collision input. In RMII mode, this pin don't use. |
| CLK25M | 109 | O | Port4 MII 25MHz clock output. |

| SGRAM/SDRAM Interface Pins | | | |
|---|---|---|---|
| **Name** | **Pin Number** | **I/O** | **Descriptions** |
| AD[8:0] | 59,60,61,62, 65,66,67,68, 69 | O | Memory row/column address bus outputs AD[7:0] are row/column address [7:0]. AD[8] : This pin should connect to SGRAM/SDRAM MSB address bit. |
| DQ[31:0] | 38~42,45~55 ,78~80, 83~95 | I/O | Memory data bus |
| RASB | 75 | O | SGRAM/SDRAM row address select |
| CASB | 76 | O | SGRAM/SDRAM column address select |
| WEB | 77 | O | SGRAM/SDRAM write enable |
| BA | 73 | O | SGRAM/SDRAM bank select |
| CS0B | 74 | O | Memory chip select 0 |
| CS1B | 70 | O | Memory chip select 1 |
| MEMCLK | 57 | O | Memory clock output. |
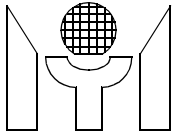
Note: SGRAM/SDRAM access time: 10 ns (max)

| LED Interface Pins | | | |
|---|---|---|---|
| **Name** | **Pin Number** | **I/O** | **Descriptions** |
| LEDDATA [7:0] | 100,101,102, 103,104,105, 106,107 | I/O | LED data output. These LED pins report Port0~7 Link/Rx activity status using LEDCLK1 strobe , and report packet buffer utilization status using LEDCLK2 strobe. |

LEDDATA   [0]   [1]   [2]   [3]   [4]   [5]   [6]   [7]

LEDCLK1  LR0 LR1 LR2 LR3 LR4 --- --- ---

LEDCLK2  Uti0 Uti1 Uti2 Uti3 Uti4 --- BFull MFail

note:

LRn: means per port's Link_RxAct status.

Uti0: 5%, Uti1: 10%, Uti2: 20%, Uti3: 35%, Uti4: 50 above .

BFull: Buffer almost full alarm signal.

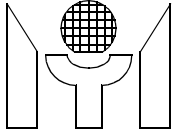Mfail: External memory poer on test failure.

| LED Interface Pins | | | |
|---|---|---|---|
| **Name** | **Pin Number** | **I/O** | **Descriptions** |
| LEDCLK1 | 96 | I/O | LED strobe 1 |
| LEDCLK2 | 97 | I/O | LED strobe 2 |

| Miscellaneous Pins | | | |
|---|---|---|---|
| **Name** | **Pin Number** | **I/O** | **Descriptions** |
| RESETB | 115 | I | System reset input, low active. |
| SYSCLK | 36 | I | Switch core system clock input, using the same clock source with REF-CLK. |
| REFCLK | 116 | I | RMII reference clock input, using 50Mhz. |
| MDC | 118 | I/O | MII management clock inout |
| MDIO | 117 | I/O | MII management data inout |
| SDC | 111 | I/O | MII register clock inout |
| SDIO | 112 | I/O | MII register data inout |
| EEDATA | 114 | I/O | EEPROM data input |
| EECLK | 113 | I/O | EEPROM clock output |
| VCC | 08,28,34,37, 44,58,64,72, 82,99,110 | PWR | Power pins |
| GND | 02,27,33,35, 43,56,63,71, 81,98,108 | GND | Ground pins |

| Jummper Configuration After Power On Reset | | | |
|---|---|---|---|
| **Name** | **Pin Number** | **I/O** | **Descriptions** |
| LEDDATA[0]<br>LEDDATA[1]<br>LEDDATA[2]<br>LEDDATA[3]<br>LEDDATA[4]<br>LEDDATA[5]<br>LEDDATA[6]<br>LEDDATA[7] | | I/O | During power on reset duration, these pins are jumper setting pins (pull_hgih = 1, pull_low = 0).<br><br>LEDDATA[0] : select SGRAM/SDRAM interface ,<br><br>"1" means 256K32 x 1 or 512K32 x 1 is selected.<br><br>"0" means 256K32 x 2 is selected, default is "1".<br><br>LEDDATA[1] : config packet buffer size,<br><br>"1" means 2 M bytes buffer size  is selected.<br><br>"0" means 1 M byte buffer size is selected, default is "0"<br><br>LEDDATA[2] :  enable memory test function,<br><br>"1" means enable.<br><br>'0" means disable, default is "1".<br><br>LEDDATA[3] : enable aging function,<br><br>"1" means enable.<br><br>"0" means disable, default is "1".<br><br>LEDDATA[4] : enable MII polling(MDC/MDIO),<br><br>"1" means enable.<br><br>"0" means disable, default is "1".<br><br>LEDDATA[5] :  enable broadcast storm control,<br><br>"1" means enable.<br><br>"0" means disable, default is "1".<br><br>LEDDATA[6] : enable backpressure function (in half mode),<br><br>"1" means enable.<br><br>"0" means disable, default is "1".<br><br>LEDDATA[7] : enable 802.3x flow control function (in full mode) ,<br><br>"1" means enable.<br><br>"0" means disable,  default is "1". |
| LEDCLK1 | | I/O | During power on reset duration, this pin is a jumper setting pin (pull_hgh =1, pull_low = 0).<br><br>LEDCLK1 : select 1K or 8K address entry table,<br><br>"1" means 8K addres entry is selected.<br><br>"0" means 1K address entry is selected,  default is "1". |
| LEDCLK2 | | I/O | During power on reset duration, this pin is a jumper setting pin (pull_hgh =1, pull_low = 0).<br><br>LEDCLK2 : enable EEPROM interface.<br><br>"1" means enable.<br><br>"0" means disable, default is "1". |

# MYSON TECHNOLOGY

# MTD505 (Preliminary)

| Jummper Configuration After Power On Reset | | | |
|---|---|---|---|
| **Name** | **Pin Number** | **I/O** | **Descriptions** |
| EEDATA | | I/O | During power on reset duration, this pin is a jumper setting pin (pull_hgh =1, pull_low = 0). <br> EEDATA : enable EEPROM auto_load configuration function while EEPROM interface is enabled, <br> "1" means enable. <br> "0" means disable, default is "1". |
| TXEN[2:0] | | I/O | During power on reset duration, this pin is a jumper setting pin (pull_hgh =1, pull_low = 0). <br> TXEN[2:0] : uplink port (flooding port) 0 ~7 selection; default is "000". |
| TXEN[3] | | I/O | During power on reset duration, this pin is a jumper setting pin (pull_hgh =1, pull_low = 0). <br> TXEN[3] : enable flooding control, <br> "1" means enable. <br> "0" means disable, default is "0". |
| TXEN[4] | | I/O | During power on reset duration, this pin is a jumper setting pin (pull_hgh =1, pull_low = 0). <br> TXEN[4] : enable VLAN tag 1522 bytes receiving, <br> "1" means enable. <br> "0" means disable, default is "0". |
| SDC | | I/O | During power on reset duration, this pin is a jumper setting pin (pull_hgh =1, pull_low = 0). <br> SDC : Port4  MII/RMII interface selection, <br> "1" means Port4 MII interface is selected. <br> "0" means Port4 RMII interface is selected, default is "0". |
| EECLK | | I/O | During power on reset duration, this pin is a jumper setting pin (pull_hgh =1, pull_low = 0). <br> EECLK : scan mode enable for debugging purpose, <br> "1" means scan mode enable. <br> "0" means scan mode disable, default is "0". |
| MDC | | I/O | During power on reset duration, this pin is a jumper setting pin (pull_hgh =1, pull_low = 0). <br> MDC : fast mode enable for testing purpose, <br> "1" means fast mode enable. <br> "0" means fast mode disable, default is "0". |
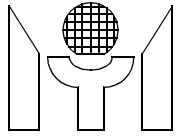
## 3.0 FUNCTIONAL DESCRIPTIONS

The MTD505 is an 5 ports 10/100 Mbps fast Ethernet switch controller. It is a low cost solution for eight ports fast Ethernet SOHO switch design. No CPU interface is required; After power on reset, MTD505 provide an auto load configuration setting function through a 2 wire serial EEPROM interface to acess external EEPROM device, and MTD505 can easily be configured to support port_trunking, port_ VLAN, static entry, 802.3X flow control threshold setting , flooding port assignment ...etc functions. The following descriptions are MTD505's major functional blocks overview.

## 3.1 Packet store and forwarding

The MTD505 use simple store and forward algorithm as packet switching method. Input packet from ports will be stored to external memory first, while packet is good for forward (CRC chech ok, 64Bytes < length < 1518Bytes, not local packets, in the same VLAN group ) , if this packet's DA hits, than forward this packet to the destination port, otherwise this packet will be broadcasted.

## 3.2 Learning and Routing

The MTD505 supports 1K or 8K MAC entries for switching. Dynamic address learning is performed by each good unicast packet is completely received. The static address learning is achieved by EEPROM configuration. On the other hand, the routing process is performed whenever the packet's DA is captured. If the DA can not get a hit result, the packet is going to switch broadcast or forward to the dedicated port according to the flooding control selction.

## 3.3 Aging

Only the dynamic address entries are scheduled in the aging machine. If one station does not transmit any packet for a period of time, the belonging MAC address will be kicked out from the address table. The aging out time can be program through the EEPROM auto load configuration. (Default value is 300 seconds)

## 3.4 Buffer Queue Management

The buffer queue manager is implemented to manage the external shared memory (use SDRAM/ SGRAM) for packet buffering. The main function of the buffer queue manager is to maintain the linked list consists of buffer IDs, which is used to show the corresponding memory address for each incoming packet. In addition, the buffer queue manager monitors the rested free spaces status of the external memory, If the packet storage achieve the predefined threshold value, the buffer queue manager will raise the alarm signal which is used to enable the flow control mechanism for avoiding transmission ID queue overflow happening. MTD505 provide 802.3x flow control in full duplex mode and back pressure control in half duplex mode.

## 3.5 Full Duplex 802.3x Flow Control

In full duplex mode, MTD505 supports the standard flow control defined in IEEE802.3x standard. It enables the stopping of remote node transmissions via a PAUSE frame information interactoin. When the "802.3x flow control enable" bit is set during power on reset (LEDDATA[7] pin is external pull_high), it enables MTD505 supporting 802.3x flow control function in full_duplex mode; When output port buffer queue's on_using value reach the initialization setting threshold value (recommended Xon_TH = 74'h when using 2Mbytes external memory; Xon_TH = 2e'h when using 1Mbytes external memory), MTD505 will send out a PAUSE packet with pause time equal to FFF to stop the remote node transmission; When the output port buffer queue's on_using value reduce to the initialization threshold value(recommended Xoff_TH = 30'h when using 2Mbytes external memory; Xoff_TH=18'h when using 1Mbytes external memory), MTD505 will also send a PAUSE packet with pause time equal to zero to inform the remote node to retransmit packet.
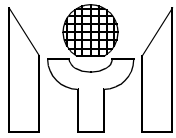
### 3.6 Half Duplex Back Pressure Control

In half duplex mode, MTD505 provide a back pressure control mechanism to avoid dropping packets during network conjection situation. When the "back pressure control enable" bit is set during power on reset (LEDDATA[6] pin is external pull_high), it enables MTD505 supporting back pressure function in half_duplex mode; When output port buffer queue's on_using value reach the initialization setting threshold value (same with the Xon_TH value), MTD505 will send a JAM pattern in the input port when it senses an incoming packet , thus force a collision to inform the remote node transmission back off and will effectively avoid dropping packets. If the "back pressure control enable" bit is not set, and there is no free buffer queue available for the incoming packets, the incoming packets will be dropped.

### 3.7 MII Polling

The MTD505 supports PHY management through the serial MDIO/MDC interface. After power on reset, the MTD505 write related abilities to the advertisement register 4 of connected PHY devices and restart the auto_negotiation prcedure via MDIO/MDC interface using the predefined PHY addresses increasingly from "01000"b to "01100"b. The MTD505 will periodically and continuously poll and update the link status and link partner's ability which include speed, duplex mode, and 802.3x flow control capable status of the connected PHY devices through MDIO/MDC serial interface.
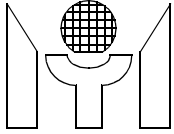
### 3.8 MAC and DMA engine

The MTD505's MAC performs all the functions in IEEE802.3 protocol, such as frame formatting, frame stripping, CRC checking, bad packet dropping, defering to line traffic, and collision handling. The MAC Rx_engine checks incoming packets and drops the bad packet which include CRC error, alignment error, short packet (less than 64 bytes), and long packet(more than 1518 bytes or 1522 bytes when the "VLAN tag 1522 bytes receive enable" bit is set during power on reset). Before transmission, The MAC Tx_engine will constantly monitor the line traffic using derfering precedure. Only if it has been idle for a 96 bits time (a minimum interpacket gap time, IPG time), actual transmmission can be started. For the half duplex mode, MAc engine will detect collision; if a collision is detected, the MAC Tx_engine will transmit a JAM pattern and then delay the re_transmission for a random time period determined by the back_off algorithm (MTD505 implements the truncated exponential back_off algorithm defined in IEEE 802.3 standard). For the full duplex mode, collision signal is ignored.

The MTD505's DMA engine performs the packets non_blocking transportation between MAC engine and external memory according to a high speed switching procedure. The switching procedure is completed by address learning/routing process and buffer queue management operation.

### 3.9 EEPROM interface

MTD505 provide an auto load configuration setting function through a 2 wire serial EEPROM interface to acess external EEPROM device(24C02) after power on reset . MTD505 can easily be configured to support port_trunking, port_ VLAN, static entry, 802.3X flow control threshold setting , flooding port assignment ...etc functions. The following table is the EEPROM contents mapping:

| Name | EEPROM Address | EEPROM Content Description | Recommended Value Under Basic Operation |
|---|---|---|---|
| EOB | 00 | Last EEPROM content address value | 8'h13 |
| AgeLow | 01 | Aging Time bit [7:0] | 8'h2c |
| AgeHigh | 02 | Aging Time bit [15:8] | 8'h01 |
| VLAN0 | 03 | Port0 VLAN register | 8'hfe |
| VLAN1 | 04 | Port1 VLAN register | 8'hfd |
| VLAN2 | 05 | Port2 VLAN register | 8'hfb |
| VLAN3 | 06 | Port3 VLAN register | 8'hf7 |
| VLAN4 | 07 | Port4 VLAN register | 8'hef |

| Name | EEPROM Address | EEPROM Content Description | Recommended Value Under Basic Operation |
|---|---|---|---|
| Reserved | 08 | reserved | 8'hdf |
| Reserved | 09 | reserved | 8'hbf |
| Reserved | 0a | reserved | 8'h7f |
| UpLink10 | 0b | bit[7:4] --- the flooding port_no of Port1 <br><br> bit[3:0] --- the flooding port_no of Port0 <br><br> *ex1: bit[7:4] = "0011"b, means that if the incomin packet of Port1 got the "un_routed" result, then this incoming packet will be flooded to Port3. <br><br> *ex2: bit[3:0] = "0111"b, means that if the incomin packet of Port0 got the "un_routed" result, then this incoming packet will be flooded to Port7. <br><br> (note: set value "4'hf", means flooding to all the other ports; set value "4'h8"~"4'he" is forbidden) | 8'h0f |
| UpLink32 | 0c | bit[7:4] --- the flooding port_no of Port3 <br><br> bit[3:0] --- the flooding port_no of Port2 <br><br> (note: set value "4'hf", means flooding to all the other ports; set value "4'h8"~"4'he" is forbidden) | 8'h00 |
| UpLink54 | 0d | bit[7:4] --- reserved <br><br> bit[3:0] --- the flooding port_no of Port4 <br><br> (note: value setting "f", means flooding to all the other ports; value setting "8" ~ "e" is forbidden) | 8'h00 |
| Reserved | 0e | reserved | 8'h00 |
| Broadcast TH | 0f | Broadcast threshold | 8'hff |
| Xon TH | 10 | Xon threshold | 8'h74 |
| Xoff TH | 11 | Xoff threshold | 8'h30 |
| DisPort | 12 | Disable Port | 8'h00 |
| System Control | 13 | System control byte : <br><br> bit[0] --- enhanced back pressure enable, <br><br> bit[7:1] --- reserved. | 8'h00 |
| Reserved | 14 ~1f | none | |
| StaticSA1 | 20 ~26 | Address 26 bit[2:0] --- means Port ID <br><br> Address 25 bit[7:0] ~ Address 20 bit[7:0] --- means static SA[47:0] | |
| StaticSA2 | 27 ~ 2d | Address 2d bit[2:0] --- means Port ID <br><br> Address 2c bit[7:0] ~ Address 27 bit[7:0] --- means static SA[47:0] | |

### 3.10  Port Based VLAN

The MTD505 supports VLAN configuration by port based methodology. One port select the certain ports to form its VLAN group by configuring the VLAN register. The packet (including broadcast packet) is not forwarding to the destination port whose VLAN group is different from the source port.
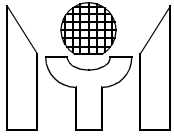
### 3.11 Port Trunking

The port trunking function can also be implemented by VLAN registers. One trunk port isolates the packet transmitting and receiving from the other trunk ports, which performs a logical trunk topology. The non-trunk port should choose only one trunk port for transmitting, which can achieve the load balancing and maintain the packet sequences.

### 3.12 Memory Interface

Two kinds of external memory interface can be selected by user -- 1M byte memory (256K32 x 1) and 2 M bytes (256K32 x 2 or 512K32 x 1). Maximum 2M byte external memory can be used for packet buffering. "-10 " speed grade of SGRAM/SDRAM device is recommanded. The following table is the SGRAM application pin connection :

| Memory Type | Memory Chip No | A[8] | CS0B | CS1B |
|---|---|---|---|---|
| 256K32 | x 1 | A8 | CS0B | NC |
| 256K32 | x 2 | A8 | CS0B | CS1B |
| 512K32 | x 1 | A9 | CS0B | A8 |

### 3.13 Internal MII Registers Acess and Control

The MTD505 support 2 serial pins (SDIO/SDC) for internal registers acess and control; The detailed registers informations are presented in Section4.0 (Internal MII Registers).

### 3.14 LED Display

The MTD505 use 10 pins to output 2 kinds of LED display -- LEDDATA[7:0], LEDCLK1, LEDCLK2. Using LEDCLK1 rising edge, LEDDATA[7:0] report   Port7~0 link/receive activity led status. Using LEDCLK2 rising edge, LEDDATA[4:0] report packet buffer utilization rating, and LEDDATA[7] report external memory test result(after power reset, MTD505 will test external SDRAM automatically), LEDDATA[6] report  the buffer almost full alarm signal .

### 4.0 Internal MII Registers

The MTD505 implements 10 MII global registers and 4 per port registers, define as following tables:

**TABLE 1. MII registers**

| GLOBAL REGISTERS | | | | | |
|---|---|---|---|---|---|
| REG NO | Bits | Name | R/W | Descriptions | Default |
| 0 | | CtlReg0 | R/W | CONTROL REGISTER 0 | |
| | 8-0 | | | bit[0] = 1 --> switch to port 0 registers<br>bit[1] = 1 --> switch to port 1 registers<br>bit[2] = 1 --> switch to port 2 registers<br>bit[3] = 1 --> switch to port 3 registers<br>bit[4] = 1 --> switch to port 4 registers<br>bit[5] = reserved<br>bit[6] = reserved<br>bit[7] = reserved<br>bit[8] = 1 --> switch to global registers | 9'h100 |
| | 12-9 | | | scan mode select 3-0 | |
| | 15-13 | | | Scan port select | |
| 1 | | CtlReg1 | R/W | CONTROL REGISTER 1 | 16'h3084 |

**TABLE 1. MII registers**

| GLOBAL REGISTERS | | | | | |
|---|---|---|---|---|---|
| **REG NO** | **Bits** | **Name** | **R/W** | **Descriptions** | **Default** |
| | 7-0 | XON | | XON threshold. | |
| | 15-8 | XOFF | | XOFF threshold. While EEPROM is enabled, this register's content will be updated by EEPROM read XON/XOFF threshold data automatically. After EEPROM read is done, this register can be read/write by management cmd. default is 16'h3084(2M memory) or 16'h1838(1M memory) | |
| **2** | | **CtlReg2** | **R/W** | **CONTROL REGISTER 2** | **16'd300** |
| | 15-0 | Aging | | bit[15:0] can specify aging time. While EEPROM is enabled, this register's content will be updated by EEPROM read Aging timer data automatically. After EEPROM read is done, this register can be read/write by management cmd. | |
| **3** | | **CtlReg3** | **R/W** | **CONTROL REGISTER 3** | **16'h000f** |
| | 15-0 | Uplink reg0 | | bit[15:12] specify port 3's uplink port ID. bit[11:8] specify port 2's uplink port ID. bit[7:4] specify port 1's uplink port ID. bit[3:0] specify port 0's uplink port ID. default is 16'h000f. P.S this register's write sequence is Jumper setting ==> EEPROM content ==> MII management command. | |
| **4** | | **CtlReg4** | **R/W** | **CONTROL REGISTER 4** | **16'h0** |
| | 15-0 | Uplink reg1 | | bit[15:12] :reserved bit[11:8] : reserved bit[7:4] : reserved bit[3:0] specify port 4's uplink port ID. default is 16'h0. P.S this register's write sequence is Jumper setting ==> EEPROM content ==> MII management command. | |
| **5** | | **CtlReg5** | **R/W** | **CONTROL REGISTER 5** | **16'hff** |
| | 7-0 | | | bit[7:0] specify broadcast threshold. | |
| | 8 | | | bit[8] enable enhance backpressure. | |
| | 15-9 | | | Reserved. P.S this register can be written by EEPROM content or MII management command too. | |
| **6** | | **StsReg0** | **RO/ RC** | **STATUS REGISTER 0** | |
| | 7-0 | | | bit[4:0] outputs port4-0 RXDMA fifofull, bit[7:5] : reserved. | |

**TABLE 1. MII registers**

| REG NO | Bits | Name | R/W | Descriptions | Default |
|---|---|---|---|---|---|
| | | | | **GLOBAL REGISTERS** | |
| | 15-8 | | | bit[12:8] outputs port4-0 TXDMA TPUR(fifoempty), bit[15:13] : reserved. | |
| 7 | | StsReg1 | RO | **STATUS REGISTER 1** | |
| | | | | 0      BufBistDone. | |
| | | | | 1      BufBistErr. | |
| | | | | 2      BufInitDone. | |
| | | | | 3      AddrTblBistDone. | |
| | | | | 4      AddrTblBistErr. | |
| | | | | 5      LthTblBistDone. | |
| | | | | 6      LthTblBistErr. | |
| | | | | 7      MemBistDone. | |
| | | | | 8      MemBistErr. | |
| | | | | 9      EEDone. | |
| | | | | 10     FreeCntIs0. | |
| | | | | 15-11   Reserved. | |
| 8 | | CtlReg7 | R/W | **CONTROL REGISTER 7** | |
| | 7-0 | | | bit[4:0] output mii polling port4-0 flow control information, bit[7:5] : reserved | |
| | 15-8 | | | bit[12:8] output mii polling port4-0 link information, bit[15:13] : reserved. "1" means flow control enable or link good. | |
| 9 | | CtlReg8 | R/W | **CONTROL REGISTER 8** | |
| | 7-0 | | | bit[4:0] output mii polling port4-0 speed information, bit[7:5] : reserved. | |
| | 15-8 | | | bit[12:8] output mii polling port4-0 full information, bit[15:13] :reserved. "1" means 100M or full duplex. | |
| | | | | **PORT REGISTERS** | |
| 1 | | StsReg1 | RO | **STATUS REGISTER 1** | |
| | 10-0 | | | bit[10:0] output Port Tx queue head value. | |
| | 15-11 | | | Reserved. | |
| 2 | | StsReg2 | RO | **STATUS REGISTER 2** | |
| | 10-0 | | | bit[10:0] output Port Tx queue tail value. | |
| | 15-11 | | | Reserved. | |
| 3 | | StsReg3 | RO | **STATUS REGISTER 3** | |
| | 10-0 | | | bit[10:0] output Port Tx queue count value. | |
| | 15-11 | | | Reserved. | |
| 4 | | CtlReg1 | R/W | **CONTROL REGISTER 1** | |
| | 7-0 | | | bit[7:0] select Port VLAN group. | |
| | 15-8 | | | Reserved. | |
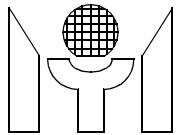
"R/W" means read/writable.

## 5.0 Electrical Characteristics

### 5.1 Absolute Maximum Ratings

| Symbol | Parameter | RATING | Unit |
|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | -0.3 to 3.6 | V |
| $V_{IN}$ | Input Voltage | -0.3 to Vcc+0.3 | V |
| $V_{OUT}$ | Output Voltage | -0.3 to Vcc+0.3 | V |
| $T_{STG}$ | Storage Temperature | -55 to 150 | $^oC$ |

### 5.2 Recommended Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply | 3.0 | 3.3 | 3.6 | V |
| $V_{IN}$ | Input Voltage | 0 | - | Vcc | V |
| $T_j$ | Commercial Junction Operating Temperature | 0 | 25 | 115 | $^oC$ |
| | Industrial Junction Operating Temperature | -40 | 25 | 125 | $^oC$ |

### 5.3 DC Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage Current | no pull-up or down | -1 | | 1 | uA |
| $I_{OZ}$ | Tri-state Leakage Current | | -1 | | 1 | uA |
| $C_{IN}$ | Input Capacitance | | | 2.8 | | pF |
| $C_{OUT}$ | Output Capacitance | | | 2.7 | 4.9 | pF |
| $C_{BID3}$ | Bi-direction buffer Capacitance | | | 2.7 | 4.9 | pF |
| $V_{IL}$ | Input Low Voltage | CMOS | | | 0.3*Vcc | V |
| $V_{IH}$ | Input High Voltage | CMOS | 0.7*Vcc | | | V |
| $V_{OH}$ | Output High Voltage | $I_{OL}$=2,4,8,12,16,24mA | | | 0.4 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OH}$=2,4,8,12,16,24mA | 2.4 | | | V |
| $R_I$ | Input Pull-up/down resistance | $V_{IL}$=0V or $V_{IH}$=$V_{CC}$ | | 75 | | KOhm |

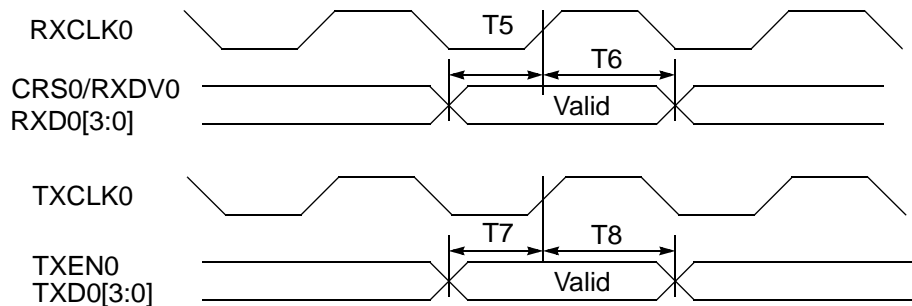(Under recommended operating conditions and Vcc = 3.0 ~ 3.6V, Tj = 0 to +115 $^oC$)
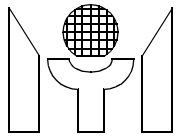
## 5.4 Electrical Characteristics

**FIGURE 1. RMII timing**
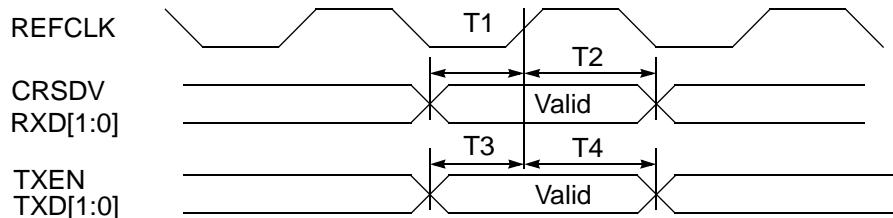


| Symbol | Parameter | Min. | Typ. | Max. | Unit | Note |
|--------|-----------|------|------|------|------|------|
| T1 | RMII input setup time | 1 | | | nS | |
| T2 | RMII input hold time | 1 | | | nS | |
| T3 | RMII output setup time | 3 | | | nS | |
| T4 | RMII output hold time | 5 | | | nS | |

**FIGURE 2. MII timing**



| Symbol | Parameter | Min. | Typ. | Max. | Unit | Note |
|--------|-----------|------|------|------|------|------|
| T5 | MII input setup time | 10 | | | nS | |
| T6 | MII input hold time | 10 | | | nS | |
| T7 | MII output setup time | 3 | | | nS | |
| T8 | MII output hold time | 5 | | | nS | |
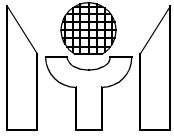
**FIGURE 3. Memory Write Timing**
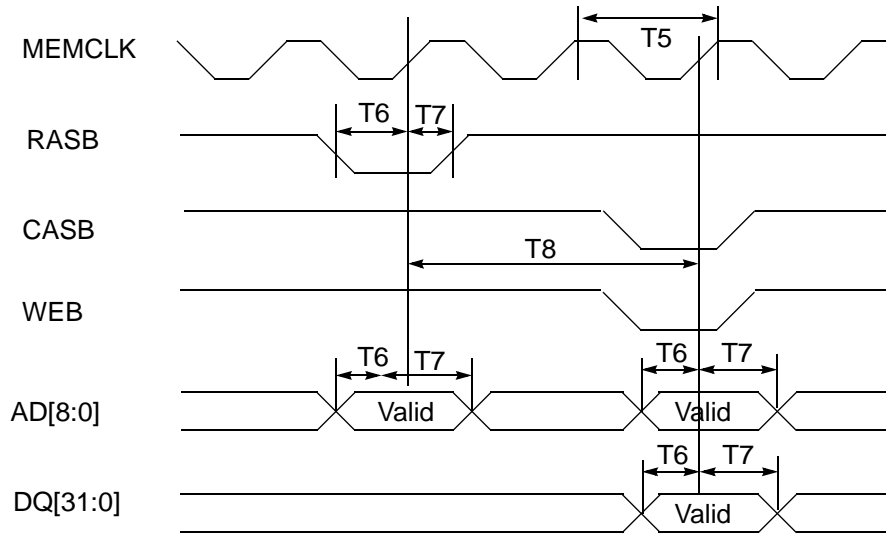


| Symbol | Parameter | Min. | Typ. | Max. | Unit | Note |
|--------|-----------|------|------|------|------|------|
| T5 | Memory clock cycle | 12 | | | nS | |
| T6 | Memory command/address/data setup time | 6 | | | nS | |
| T7 | Memory command/address/data hold time | 2 | | | nS | |
| T8 | Row active to burst write | | 2 | | CLK | |

**FIGURE 4. Memory Read Timing**
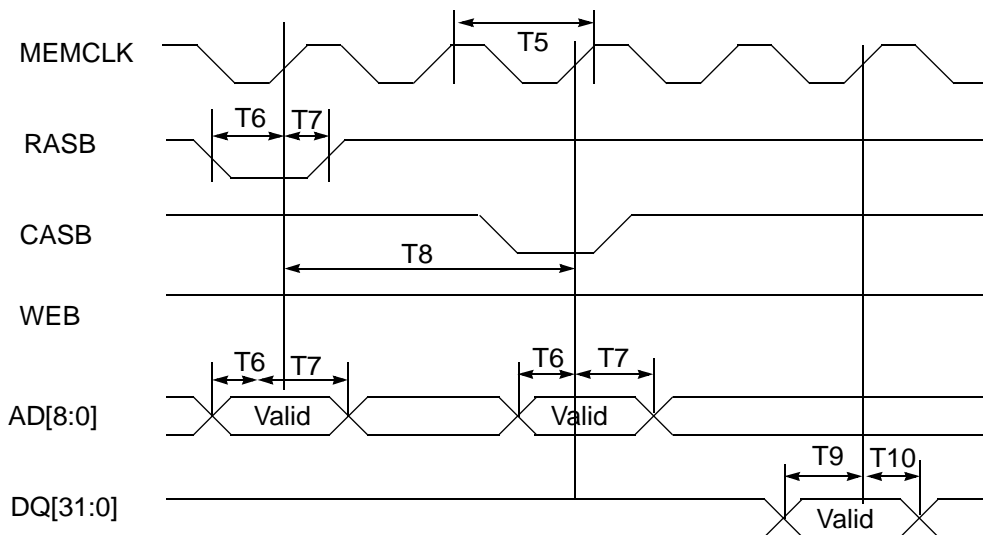
| Symbol | Parameter | Min. | Typ. | Max. | Unit | Note |
|--------|-----------|------|------|------|------|------|
| T10 | Memory read data setup time | 2 | | | nS | |
| T11 | Memory ead data hold time | 2 | | | nS | |

**FIGURE 5. EEPROM timing**
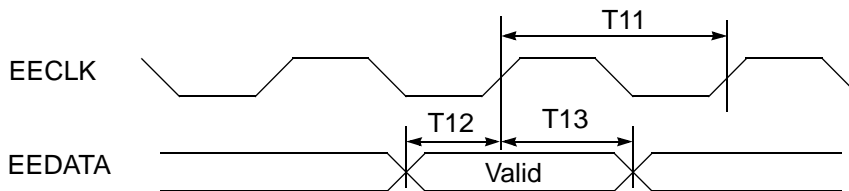


| Symbol | Parameter | Min. | Typ. | Max. | Unit | Note |
|--------|-----------|------|------|------|------|------|
| T11 | EEPROM clock cycle | | 10 | | uS | |
| T12 | EEDATA input setup time | 1 | | | nS | |
| T13 | EEDATA input hold time | 1 | | | nS | |

**FIGURE 6. LED Interface**
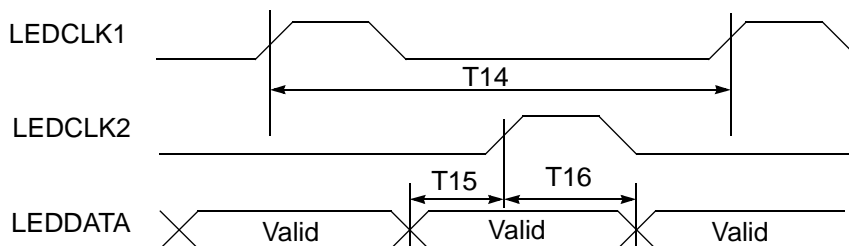


| Symbol | Parameter | Min. | Typ. | Max. | Unit | Note |
|--------|-----------|------|------|------|------|------|
| T14 | Led display strobe period | | 20 | | uS | |
| T15 | LEDCLK setup time | | 5 | | uS | |
| T16 | LEDCLK hold time | | 5 | | uS | |
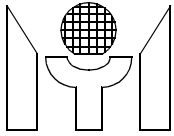
## 6.0  128 pin PQFP Package Data
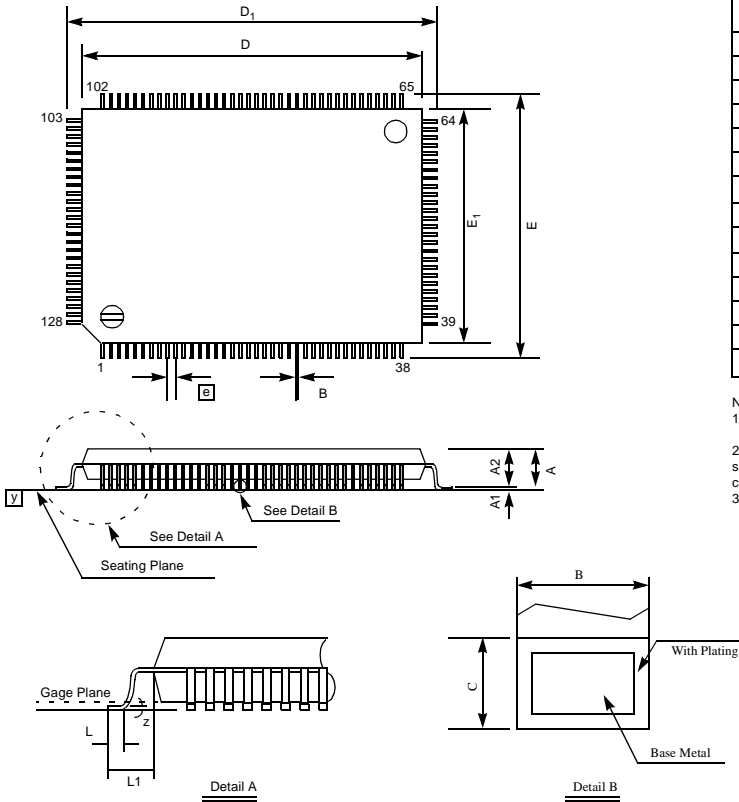


| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min | Norm | Max | Min | Norm | Max |
| A | - | - | 0.134 | - | - | 3.40 |
| A1 | 0.010 | - | - | 0.25 | - | - |
| A2 | 0.107 | 0.112 | 0.117 | 2.73 | 2.85 | 2.97 |
| B | 0.007 | 0.009 | 0.011 | 0.17 | 0.22 | 0.27 |
| C | 0.004 | - | 0.008 | 0.09 | - | 0.20 |
| D | 0.906 | 0.913 | 0.921 | 23.00 | 23.20 | 23.40 |
| D1 | 0.783 | 0.787 | 0.791 | 19.90 | 20.00 | 20.10 |
| E | 0.669 | 0.677 | 0.685 | 17.00 | 17.20 | 17.40 |
| E1 | 0.547 | 0.551 | 0.555 | 13.90 | 14.00 | 14.10 |
| e | 0.020 BSC | | | 0.50 BSC | | |
| L | 0.029 | 0.035 | 0.041 | 0.73 | 0.88 | 1.03 |
| L1 | 0.063 BSC | | | 1.60 BSC | | |
| y | - | - | 0.004 | - | - | 0.10 |
| z | 0° | - | 7° | 0° | - | 7° |

Note:
1. Dimension D1 & E1 do not include mold protrusion.
   But mold mismatch is included. Allowable protrusion is .25mm/.010" per side.
2. Dimension B does not include dambar protrusion. Allowable dambar protrusion .08mm/.003". Total in excess of the B dimemsion at maximum material condition. Dambar cannot be located on the lower radius or the foot.
3. Controlling dimension : Millimeter.