Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
TO-247 with Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

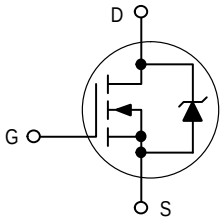
MTW8N60E

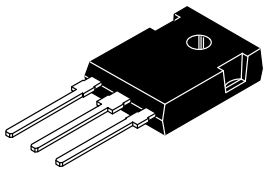
Motorola Preferred Device

TMOS POWER FET
8.0 AMPERES
600 VOLTS
$R_{DS(on)}$ = 0.55 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware





CASE 340K–01, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	600	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	8.0 6.4 24	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	180 1.43	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 24 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	864	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.70 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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Preferred devices are Motorola recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	600 —	— 695	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 7.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 4.0 Adc)		$R_{DS(on)}$	—	0.46	0.55	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 8.0 Adc) (I_D = 4.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	3.2 —	4.8 4.6	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 4.0 Adc)		g_{FS}	4.0	8.5	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	2480	3470	pF
Output Capacitance		C_{oss}	—	247	346	
Reverse Transfer Capacitance		C_{rss}	—	56	120	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 300 Vdc, I_D = 8.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	23.6	50	ns
Rise Time		t_r	—	37.6	70	
Turn–Off Delay Time		$t_{d(off)}$	—	80	170	
Fall Time		t_f	—	48	95	
Gate Charge (See Figure 8)	(V_{DS} = 300 Vdc, I_D = 8.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	67	100	nC
		Q_1	—	17	—	
		Q_2	—	26	—	
		Q_3	—	27	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 8.0 Adc, V_{GS} = 0 Vdc) (I_S = 8.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.829 0.71	1.1 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 8.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	381	—	ns
		t_a	—	225	—	
		t_b	—	156	—	
Reverse Recovery Stored Charge		Q_{RR}	—	4.61	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.