32M-BIT [4M x 8/2M x 16] SINGLE VOLTAGE 3V ONLY FLASH MEMORY

FEATURES

GENERAL FEATURES

- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- 4,194,304 x 8 / 2,097,152 x 16 switchable
- Sector structure
  - 8KB (4KW) x 8 and 64KB(32KW) x 63
- Latch-up protected to 250mA from -1V to VCC + 1V
- Low VCC write inhibit is equal to or less than 1.5V
- Compatible with JEDEC standard
  - Pin-out and software compatible to single power supply Flash

PERFORMANCE

- High Performance
  - Fast access time: 70R/90ns
  - Page read time: 25ns
  - Sector erase time: 0.5s (typ.)
  - Effective write buffer word programming time: 22us
  - 4 word/8 byte page read buffer
  - 16 word/ 32 byte write buffer: reduces programming time for multiple-word/byte updates
- Low Power Consumption
  - Active read current: 18mA(typ.)
  - Active write current: 50mA(typ.)
  - Standby current: 20uA(typ.)
- Minimum 100,000 erase/program cycle
- 20-years data retention

SOFTWARE FEATURES

- Support Common Flash Interface (CFI)
  - Flash device parameters stored on the device and provide the host system to access
- Program Suspend/Resume
  - Suspend program operation to read other sectors
- Erase Suspend/Erase Resume
  - Suspends sector erase operation to read data from or program data to another sector which is not being erased
- Status Reply
  - Data# polling & Toggle bits provide detection of program and erase operation completion

HARDWARE FEATURES

- Ready/Busy (RY/BY#) Output
  - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
  - Provides a hardware method to reset the internal state machine to read mode
- WP#/ACC input
  - Write protect (WP#) function allows protection of all sectors, regardless of sector protect status
  - ACC (high voltage) accelerates programming time for higher throughput during system

SECURITY

- Sector Protection/Chip Unprotect
  - Provides sector group protect function to prevent program or erase operation in the protected sector group
  - Provides chip unprotect function to allow code changes
- Sector Permanent Lock
  - A unique lock bit feature allows the content to be permanently locked
  (Please contact Macronix sales for specific information regarding this permanent lock feature)
- Secured Silicon Sector
  - Provides a 128-word OTP area for permanent, secure identification
  - Can be programmed and locked at factory or by customer

PACKAGE

- 48-pin TSOP (for MX29LA320MT/B)
- 48-ball CSP (for MX29LA320MT/B)
- 56-pin TSOP (for MX29LA321MT/B)
- 64-ball CSP (for MX29LA321MT/B)
- **All Pb-free devices are RoHS Compliant**

GENERAL DESCRIPTION

The MX29LA32xMT/B is a 32-mega bit Flash memory organized as 4M bytes of 8 bits or 2M words of 16 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29LA32xMT/B is packaged in 48-pin TSOP, 48-ball CSP, 56-pin TSOP and 64-ball CSP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29LA32xMT/B offers access time as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LA32xMT/B has separate chip enable (CE#) and output enable (OE#) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29LA32xMT/B uses a command register to manage this functionality.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29LA32xMT/B uses a 2.7V to 3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamperes on address and data pin from -1V to VCC + 1V.

AUTOMATIC PROGRAMMING

The MX29LA32xMT/B is byte/word/page programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed. The typical chip programming time at room temperature of the MX29LA32xMT/B is less than 31.5 seconds.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm require the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to DATA# polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 50 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than 32 seconds. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC SECTOR ERASE

The MX29LA32xMT/B is sector(s) erasable using MXIC's Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

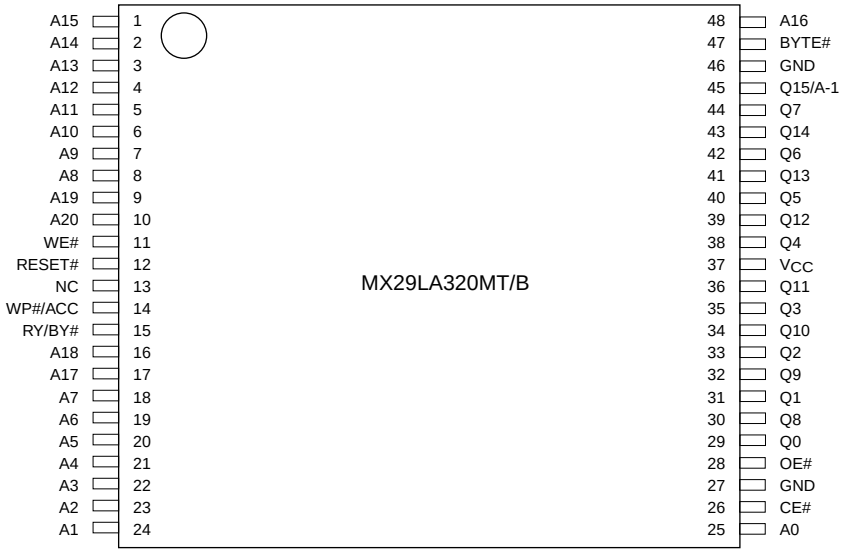
Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of WE# .

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29LA32xMT/B electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

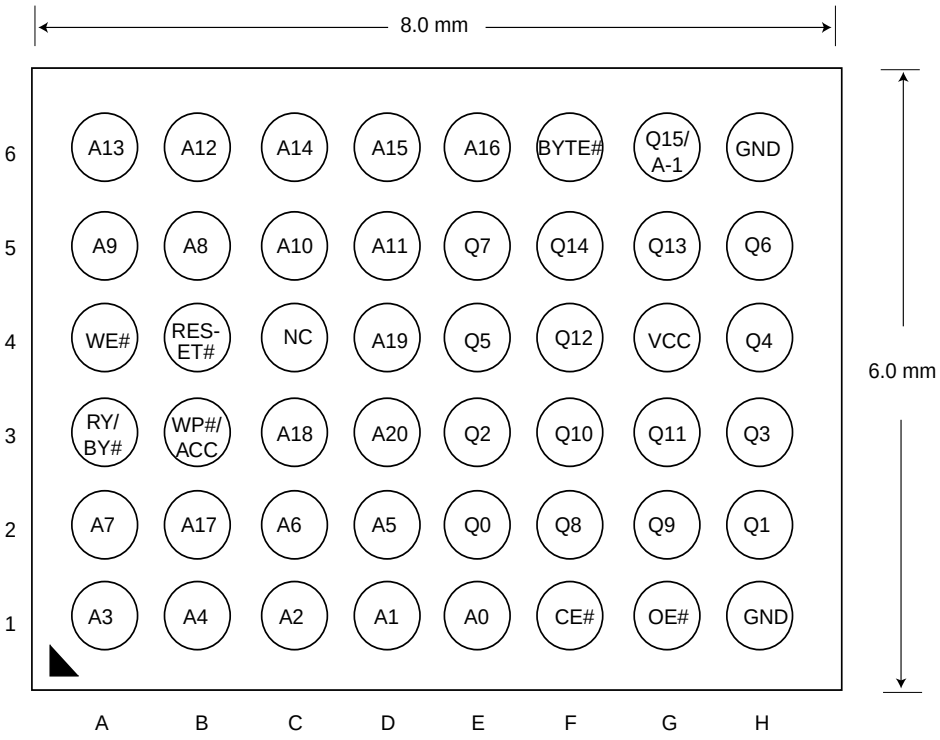
During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

PIN CONFIGURATION

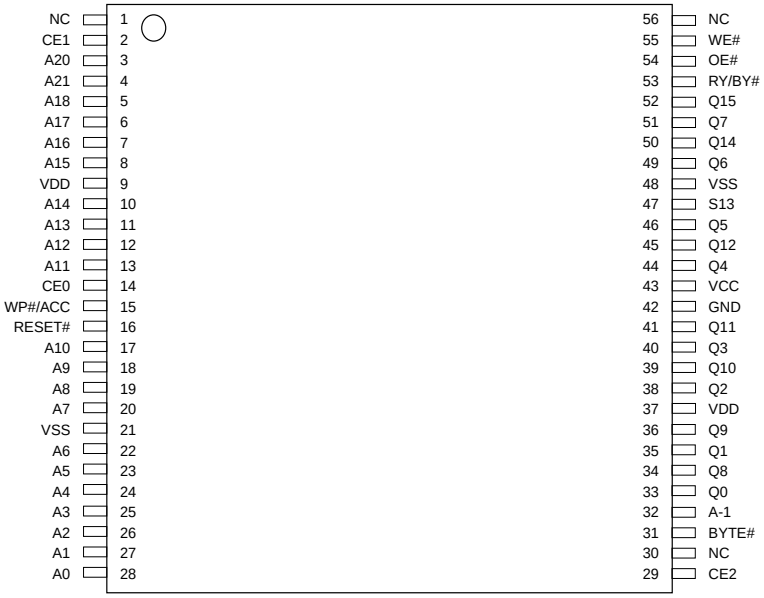
48 TSOP (for MX29LA320MT/B)



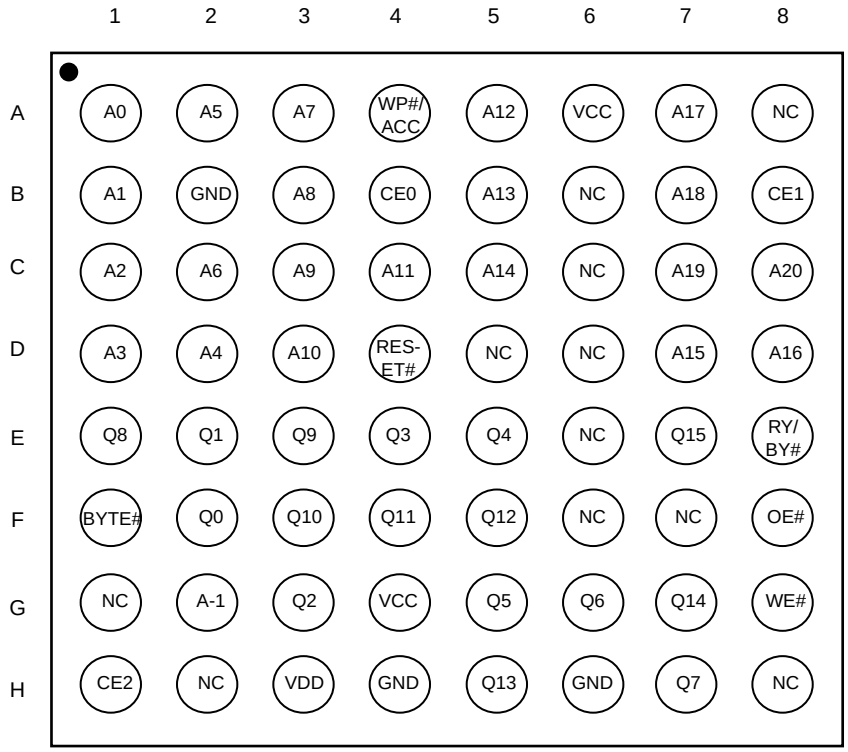
48 Ball CSP (Top View, Ball Down) (for MX29LA320MT/B)



56 TSOP (for MX29LA321MT/B)



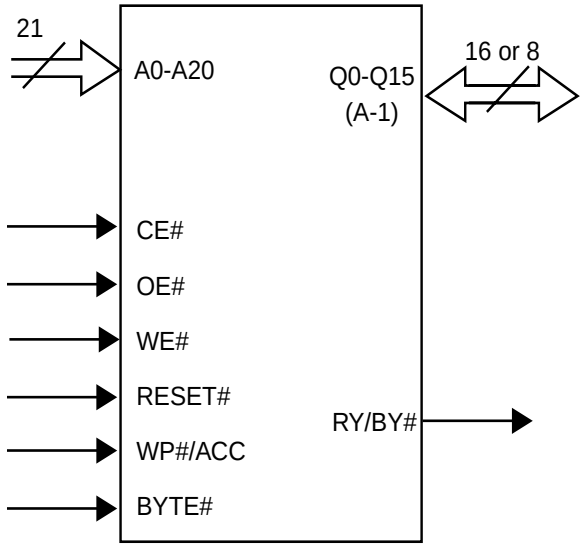
64 CSP (for MX29LA321MT/B)



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A20	Address Input
Q0~Q14	Data Inputs/Outputs
Q15/A-1	Q15(Word Mode)/LSB addr(Byte Mode)
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
RESET#	Hardware Reset Pin, Active Low
WP#/ACC	Hardware Write Protect/Programming Acceleration input
RY/BY#	Read/Busy Output
BYTE#	Selects 8 bit or 16 bit mode
VCC	+3.0V single power supply
GND	Device Ground
NC	Pin Not Connected Internally

LOGIC SYMBOL



Chip Enable Truth Table (for MX29LA321MT/B Only)

CE2	CE1	CE0	DEVICE
VIL	VIL	VIL	Enabled
VIL	VIL	VIH	Disabled
VIL	VIH	VIL	Disabled
VIL	VIH	VIH	Disabled
VIH	VIL	VIL	Enabled
VIH	VIL	VIH	Enabled
VIH	VIH	VIL	Enabled
VIH	VIH	VIH	Disabled

Note: For Single-chip applications, CE2 and CE1 can be strapped to GND.

BLOCK DIAGRAM

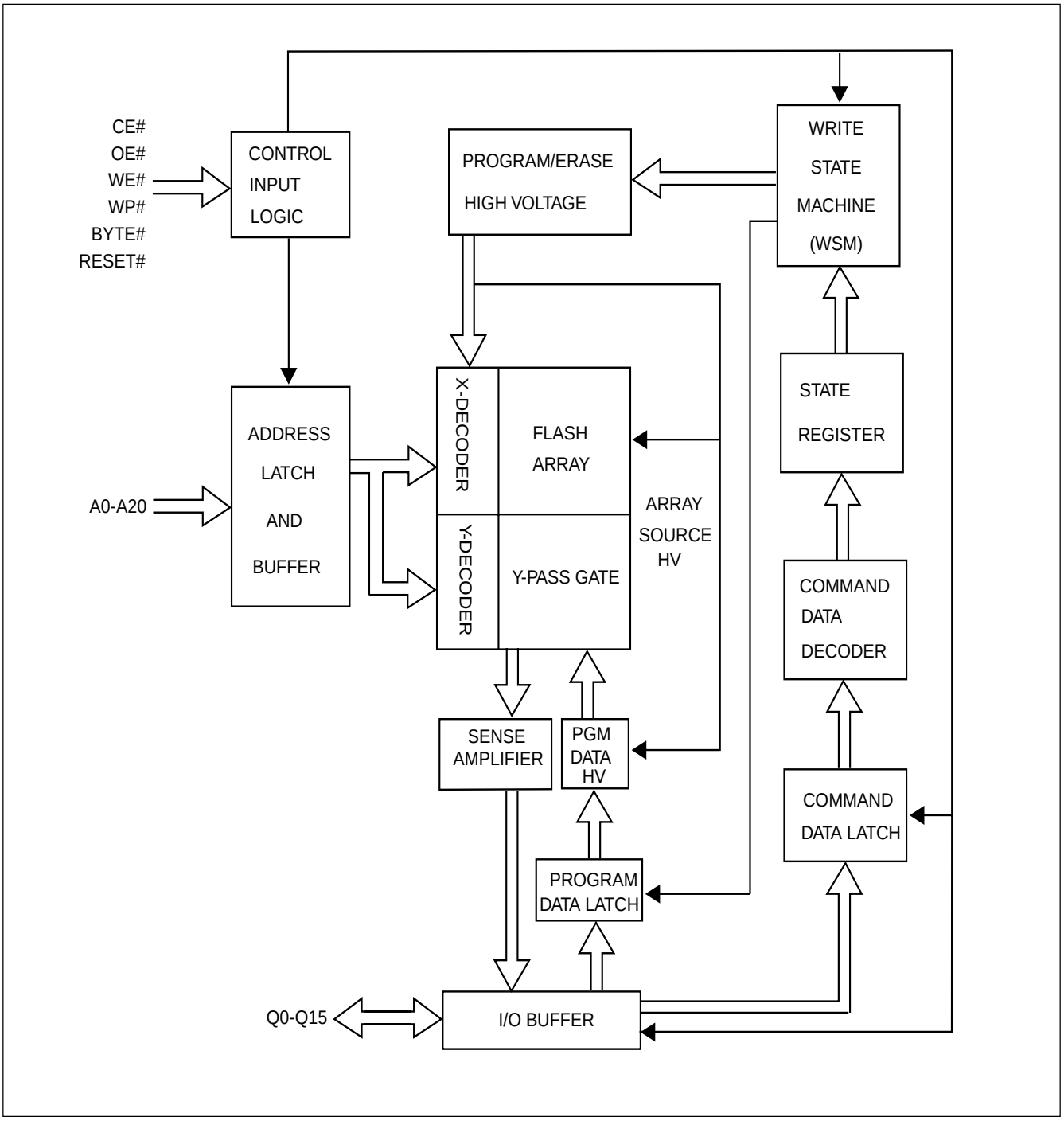


Table 1.a: MX29LA32xMT SECTOR GROUP ARCHITECTURE

Sector Group	Sector	Sector Address A20-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
1	SA0	000000xxx	64/32	000000h-00FFFFh	000000h-07FFFh
1	SA1	000001xxx	64/32	010000h-01FFFFh	008000h-0FFFFh
1	SA2	000010xxx	64/32	020000h-02FFFFh	010000h-17FFFh
1	SA3	000011xxx	64/32	030000h-03FFFFh	018000h-01FFFFh
2	SA4	000100xxx	64/32	040000h-04FFFFh	020000h-027FFFh
2	SA5	000101xxx	64/32	050000h-05FFFFh	028000h-02FFFFh
2	SA6	000110xxx	64/32	060000h-06FFFFh	030000h-037FFFh
2	SA7	000111xxx	64/32	070000h-07FFFFh	038000h-03FFFFh
3	SA8	001000xxx	64/32	080000h-08FFFFh	040000h-047FFFh
3	SA9	001001xxx	64/32	090000h-09FFFFh	048000h-04FFFFh
3	SA10	001010xxx	64/32	0A0000h-0AFFFFh	050000h-057FFFh
3	SA11	001011xxx	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
4	SA12	001100xxx	64/32	0C0000h-0CFFFFh	060000h-067FFFh
4	SA13	001101xxx	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
4	SA14	001110xxx	64/32	0E0000h-0EFFFFh	070000h-077FFFh
4	SA15	001111xxx	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
5	SA16	010000xxx	64/32	100000h-10FFFFh	080000h-087FFFh
5	SA17	010001xxx	64/32	110000h-11FFFFh	088000h-08FFFFh
5	SA18	010010xxx	64/32	120000h-12FFFFh	090000h-097FFFh
5	SA19	010011xxx	64/32	130000h-13FFFFh	098000h-09FFFFh
6	SA20	010100xxx	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
6	SA21	010101xxx	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
6	SA22	010110xxx	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
6	SA23	010111xxx	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
7	SA24	011000xxx	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
7	SA25	011001xxx	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
7	SA26	011010xxx	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
7	SA27	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
8	SA28	011100xxx	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
8	SA29	011101xxx	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
8	SA30	011110xxx	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
8	SA31	011111xxx	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh
9	SA32	100000xxx	64/32	200000h-20FFFFh	100000h-107FFFh
9	SA33	100001xxx	64/32	210000h-21FFFFh	108000h-10FFFFh
9	SA34	100010xxx	64/32	220000h-22FFFFh	110000h-117FFFh
9	SA35	100011xxx	64/32	230000h-23FFFFh	118000h-11FFFFh
10	SA36	100100xxx	64/32	240000h-24FFFFh	120000h-127FFFh
10	SA37	100101xxx	64/32	250000h-25FFFFh	128000h-12FFFFh
10	SA38	100110xxx	64/32	260000h-26FFFFh	130000h-137FFFh
10	SA39	100111xxx	64/32	270000h-27FFFFh	138000h-13FFFFh

Sector Group	Sector	Sector Address A20-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
11	SA40	101000xxx	64/32	280000h-28FFFFh	140000h-147FFFh
11	SA41	101001xxx	64/32	290000h-29FFFFh	148000h-14FFFFh
11	SA42	101010xxx	64/32	2A0000h-2AFFFFh	150000h-157FFFh
11	SA43	101011xxx	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
12	SA44	101100xxx	64/32	2C0000h-2CFFFFh	160000h-147FFFh
12	SA45	101101xxx	64/32	2D0000h-2DFFFFh	168000h-14FFFFh
12	SA46	101110xxx	64/32	2E0000h-2EFFFFh	170000h-177FFFh
12	SA47	101111xxx	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
13	SA48	110000xxx	64/32	300000h-30FFFFh	180000h-187FFFh
13	SA49	110001xxx	64/32	310000h-31FFFFh	188000h-18FFFFh
13	SA50	110010xxx	64/32	320000h-32FFFFh	190000h-197FFFh
13	SA51	110011xxx	64/32	330000h-33FFFFh	198000h-19FFFFh
14	SA52	110100xxx	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
14	SA53	110101xxx	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
14	SA54	110110xxx	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
14	SA55	110111xxx	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
15	SA56	111000xxx	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
15	SA57	111001xxx	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
15	SA58	111010xxx	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
15	SA59	111011xxx	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
16	SA60	111100xxx	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
16	SA61	111101xxx	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
16	SA62	111110xxx	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
17	SA63	111111000	8/4	3F0000h-3F1FFFh	1F8000h-1F8FFFh
18	SA64	111111001	8/4	3F2000h-3F3FFFh	1F9000h-1F9FFFh
19	SA65	111111010	8/4	3F4000h-3F5FFFh	1FA000h-1FAFFFh
20	SA66	111111011	8/4	3F6000h-3F7FFFh	1FB000h-1FBFFFh
21	SA67	111111100	8/4	3F8000h-3F9FFFh	1FC000h-1FCFFFh
22	SA68	111111101	8/4	3FA000h-3FBFFFh	1FD000h-1FDFFFh
23	SA69	111111110	8/4	3FC000h-3FDFFFh	1FE000h-1FEFFFh
24	SA70	111111111	8/4	3FE000h-3FFFFFh	1FF000h-1FFFFFh

Note:The address range is A20:A-1 in byte mode (BYTE#=VIL) or A20:A0 in word mode (BYTE#=VIH)

Table 1.b: MX29LA32xMB SECTOR GROUP ARCHITECTURE

Sector Group	Sector	Sector Address A20-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
1	SA0	000000000	8/4	000000h-001FFFh	000000h-000FFFh
2	SA1	000000001	8/4	002000h-003FFFh	001000h-001FFFh
3	SA2	000000010	8/4	004000h-005FFFh	002000h-002FFFh
4	SA3	000000011	8/4	006000h-007FFFh	003000h-003FFFh
5	SA4	000000100	8/4	008000h-009FFFh	004000h-004FFFh
6	SA5	000000101	8/4	00A000h-00BFFFh	005000h-005FFFh
7	SA6	000000110	8/4	00C000h-00DFFFh	006000h-006FFFh
8	SA7	000000111	8/4	00E000h-00FFFFh	007000h-007FFFh
9	SA8	000001xxx	64/32	010000h-01FFFFh	008000h-00FFFFh
9	SA9	000010xxx	64/32	020000h-02FFFFh	010000h-017FFFh
9	SA10	000011xxx	64/32	030000h-03FFFFh	018000h-01FFFFh
10	SA11	000100xxx	64/32	040000h-04FFFFh	020000h-027FFFh
10	SA12	000101xxx	64/32	050000h-05FFFFh	028000h-02FFFFh
10	SA13	000110xxx	64/32	060000h-06FFFFh	030000h-037FFFh
10	SA14	000111xxx	64/32	070000h-07FFFFh	038000h-03FFFFh
11	SA15	001000xxx	64/32	080000h-08FFFFh	040000h-047FFFh
11	SA16	001001xxx	64/32	090000h-09FFFFh	048000h-04FFFFh
11	SA17	001010xxx	64/32	0A0000h-0AFFFFh	050000h-057FFFh
11	SA18	001011xxx	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
12	SA19	001100xxx	64/32	0C0000h-0CFFFFh	060000h-067FFFh
12	SA20	001101xxx	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
12	SA21	001110xxx	64/32	0E0000h-0EFFFFh	070000h-077FFFh
12	SA22	001111xxx	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
13	SA23	010000xxx	64/32	100000h-10FFFFh	080000h-087FFFh
13	SA24	010001xxx	64/32	110000h-11FFFFh	088000h-08FFFFh
13	SA25	010010xxx	64/32	120000h-12FFFFh	090000h-097FFFh
13	SA26	010011xxx	64/32	130000h-13FFFFh	098000h-09FFFFh
14	SA27	010100xxx	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
14	SA28	010101xxx	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
14	SA29	010110xxx	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
14	SA30	010111xxx	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
15	SA31	011000xxx	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
15	SA32	011001xxx	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
15	SA33	011010xxx	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
15	SA34	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
16	SA35	011100xxx	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
16	SA36	011101xxx	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
16	SA37	011110xxx	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
16	SA38	011111xxx	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh

Sector Group	Sector	Sector Address A20-A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
17	SA39	100000xxx	64/32	200000h-20FFFFh	100000h-107FFFh
17	SA40	100001xxx	64/32	210000h-21FFFFh	108000h-10FFFFh
17	SA41	100010xxx	64/32	220000h-22FFFFh	110000h-117FFFh
17	SA42	100011xxx	64/32	230000h-23FFFFh	118000h-11FFFFh
18	SA43	100100xxx	64/32	240000h-24FFFFh	120000h-127FFFh
18	SA44	100101xxx	64/32	250000h-25FFFFh	128000h-12FFFFh
18	SA45	100110xxx	64/32	260000h-26FFFFh	130000h-137FFFh
18	SA46	100111xxx	64/32	270000h-27FFFFh	138000h-13FFFFh
19	SA47	101000xxx	64/32	280000h-28FFFFh	140000h-147FFFh
19	SA48	101001xxx	64/32	290000h-29FFFFh	148000h-14FFFFh
19	SA49	101010xxx	64/32	2A0000h-2AFFFFh	150000h-157FFFh
19	SA50	101011xxx	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
20	SA51	101100xxx	64/32	2C0000h-2CFFFFh	160000h-167FFFh
20	SA52	101101xxx	64/32	2D0000h-2DFFFFh	168000h-16FFFFh
20	SA53	101110xxx	64/32	2E0000h-2EFFFFh	170000h-177FFFh
20	SA54	101111xxx	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
21	SA55	110000xxx	64/32	300000h-30FFFFh	180000h-187FFFh
21	SA56	110001xxx	64/32	310000h-31FFFFh	188000h-18FFFFh
21	SA57	110010xxx	64/32	320000h-32FFFFh	190000h-197FFFh
21	SA58	110011xxx	64/32	330000h-33FFFFh	198000h-19FFFFh
22	SA59	110100xxx	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
22	SA60	110101xxx	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
22	SA61	110110xxx	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
22	SA62	110111xxx	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
23	SA63	111000xxx	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
23	SA64	111001xxx	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
23	SA65	111010xxx	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
23	SA66	111011xxx	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
24	SA67	111100xxx	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
24	SA68	111101xxx	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
24	SA69	111110xxx	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
24	SA70	111111xxx	64/32	3F0000h-3FFFFFh	1F8000h-1FFFFFh

Note:The address range is A20:A-1 in byte mode (BYTE#=VIL) or A20:A0 in word mode (BYTE#=VIH)

Table 1. BUS OPERATION (1)

Operation	CE#	OE#	WE#	RE-SET#	WP#	ACC	Address	Q0~Q7	Q8~Q15	
									BYTE# =VIH	BYTE# =VIL
Read	L	L	H	H	X	X	A_{IN}	D_{OUT}	D_{OUT}	Q8-Q14= High Z Q15=A-1
Write (Program/Erase)	L	H	L	H	(Note 3)	X	A_{IN}	(Note 4)	(Note 4)	Q8-Q14= High Z Q15=A-1
Accelerated Program	L	H	L	H	(Note 3)	V_{HH}	A_{IN}	(Note 4)	(Note 4)	Q8-Q14= High Z Q15=A-1
Standby	VCC± 0.3V	X	X	VCC± 0.3V	X	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	X	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	X	X	High-Z	High-Z	High-Z
Sector Group Protect (Note 2)	L	H	L	V_{ID}	H	X	Sector Addresses, A6=L,A3=L, A2=L, A1=H,A0=L	(Note 4)	X	X
Chip unprotect (Note 2)	L	H	L	V_{ID}	H	X	Sector Addresses, A6=H, A3=L, A2=L, A1=H, A0=L	(Note 4)	X	X

Legend:
L=Logic LOW=V_{IL}, H=Logic High=V_{IH}, V_{ID}=12.0±0.5V, V_{HH}=12.0±0.5V, X=Don't Care, A_{IN}=Address IN, D_{IN}=Data IN, D_{OUT}=Data OUT

Notes:
1. Addresses are Amax:A0 in word mode; Amax:A-1 in byte mode. Sector address are Amax:A15 in both modes.
2. The sector group protect and chip unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Chip Unprotect" section.
3. If WP#=VIL, all the sectors remain protected. If WP#=VIH, all sector's protection depends on whether they were last protected or unprotect using the method described in "Sector/ Sector Block Protection and Unprotect".
4. D_{IN} or D_{OUT} as required by command sequence, Data# polling or sector protect algorithm (see Figure 15).

Table 2. AUTOSELECT CODES (High Voltage Method)

Description		CE#	OE#	WE#	A20 to A15	A14 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	Q8 to Q15		Q7 to Q0
														BYTE# =VIH	BYTE# =VIL	
Manufacturer ID		L	L	H	X	X	VID	X	L	X	L	L	L	00	X	C2h
Device ID	Cycle 1	L	L	H	X	X	VID	X	L	X	L	L	H	22	X	7Eh
	Cycle 2										H	H	L	22	X	1Ah
	Cycle 3										H	H	H	22	X	00(bottom boot) 01h(top boot)
Sector Protection Verification		L	L	H	SA	X	VID	X	L	X	L	H	L	X	X	01h (protected), 00h (unprotected)
Secured Silicon Sector Indicator Bit (Q7), WP# protects top two address sector		L	L	H	X	X	VID	X	L	X	L	H	H	X	X	98h (factory locked), 18h (not factory locked)
Secured Silicon Sector Indicator Bit (Q7), WP# protects bottom two address sector		L	L	H	X	X	VID	X	L	X	L	H	H	X	X	88h (factory locked), 08h (not factory locked)

Legend: L = Logic Low = VIL, H = Logic High = VIH, SA = Sector Address, X = Don't care.

REQUIREMENTS FOR READING ARRAY DATA

To read array data from the outputs, the system must drive the CE# and OE# pins to VIL. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at VIH.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid address on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

PAGE MODE READ

The MX29LA32xMT/B offers "fast page mode read" function. This mode provides faster read access speed for random locations within a page. The page size of the device is 4 words/8 bytes. The appropriate page is selected by the higher address bits A0~A1(Word Mode)/A-1~A1(Byte Mode) This is an asynchronous operation; the microprocessor supplies the specific word location.

The system performance could be enhanced by initiating 1 normal read and 3 fast page read (for word mode A0-A1) or 7 fast page read (for byte mode A-1~A1). When CE# is deasserted and reasserted for a subsequent access, the access time is tACC or tCE. Fast page mode accesses are obtained by keeping the "read-page addresses" constant and changing the "intra-read page" addresses.

WRITING COMMANDS/COMMAND SEQUENCES

To program data to the device or erase sectors of memory, the system must drive WE# and CE# to VIL, and OE# to VIH.

An erase operation can erase one sector, multiple sectors, or the entire device. Table indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Writing specific address and data commands or sequences into the command register initiates device operations. Table 1 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data. Section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the Automatic Select command sequence, the device enters the Automatic Select mode. The system can then read Automatic Select codes from the internal register (which is separate from the memory array) on Q7-Q0. Standard read cycle timings apply in this mode. Refer to the Automatic Select Mode and Automatic Select Command Sequence section for more information.

ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

WRITE BUFFER

Write Buffer Programming allows the system to write a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. See "Write Buffer" for more information.

ACCELERATED PROGRAM OPERATION

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts VHH on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing VHH from the ACC pin must not be at VHH for operations other than accelerated programming, or device damage may result.

STANDBY MODE

When using both pins of CE# and RESET#, the device enter CMOS Standby with both pins held at VCC ±0.3V. If CE# and RESET# are held at VIH, but not within the range of VCC ±0.3V, the device will still be in the standby mode, but the standby current will be larger. During Auto Algorithm operation, VCC active current (ICC2) is required even CE# = "H" until the operation is completed. The device can be read with standard access time (tCE) from either of these standby modes, before it is ready to read data.

AUTOMATIC SLEEP MODE

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when address remain stable for tACC+30ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. ICC4 in the DC Characteristics table represents the automatic sleep mode current specification.

OUTPUT DISABLE

With the OE# input at a logic high level (VIH), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

RESET# OPERATION

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of tRP, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity

Current is reduced for the duration of the RESET# pulse. When RESET# is held at VSS±0.3V, the device draws CMOS standby current (ICC4). If RESET# is held at VIL but not within VSS±0.3V, the standby current will be greater.

The RESET# pin may be tied to system reset circuitry. A system reset would that also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of tREADY (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is completed within a time of tREADY (not during Embedded Algorithms). The system can read data tRH after the RESET# pin returns to VIH.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 3 for the timing diagram.

SECTOR GROUP PROTECT OPERATION

The MX29LA32xMT/B features hardware sector group protection. This feature will disable both program and erase operations for these sector group protected. In this device, a sector group consists of four adjacent sectors which are protected or unprotected at the same time. To activate this mode, the programming equipment must force VID on address pin A9 and control pin OE#, (suggest VID = 12V) A6 = VIL and CE# = VIL. (see Table 2) Programming of the protection circuitry begins on the falling edge of the WE# pulse and is terminated on the rising edge. Please refer to sector group protect algorithm and waveform.

MX29LA32xMT/B also provides another method. Which requires VID on the RESET# only. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 (with CE# and OE# at VIL and WE# at VIH). When A1=1, it will produce a logical "1" code at device output Q0 for a protected sector. Otherwise the device will produce 00H for the unprotected sector. In this mode, the addresses, except for A1, are don't care. Address locations with A1 = VIL are reserved to read manufacturer and device codes. (Read Silicon ID)

It is also possible to determine if the group is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected sector.

CHIP UNPROTECT OPERATION

The MX29LA32xMT/B also features the chip unprotect mode, so that all sectors are unprotected after chip unprotect is completed to incorporate any changes in the code. It is recommended to protect all sectors before activating chip unprotect mode.

To activate this mode, the programming equipment must force VID on control pin OE# and address pin A9. The CE# pins must be set at VIL. Pins A6 must be set to VIH. (see Table 2) Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotect mechanism begins on the falling edge of the WE# pulse and is terminated on the rising edge.

MX29LA32xMT/B also provides another method. Which requires VID on the RESET# only. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing.

It is also possible to determine if the chip is unprotect in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs (Q0-Q7) for an unprotect sector. It is noted that all sectors are unprotected after the chip unprotect algorithm is completed.

WRITE PROTECT (WP#)

The write protect function provides a hardware method to protect all sectors without using V_{ID}.

If the system asserts VIL on the WP# pin, the device disables program and erase functions in all sectors independently of whether those sectors were protected or unprotect using the method described in Sector "Sector Group Protection and Chip Unprotect".

If the system asserts VIH on the WP# pin, the device reverts to whether sectors were last set to be protected or unprotect. That is, sector protection or unprotection for the sectors depends on whether they were last protected or unprotect using the method described in "Sector/Sector Group Protection and Chip Unprotect".

Note that the WP# pin must not be left floating or unconnected; inconsistent behavior of the device may result.

SILICON ID READ OPERATION

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

MX29LA32xMT/B provides hardware method to access the silicon ID read operation. Which method requires VID on A9 pin, VIL on CE#, OE#, A6, and A1 pins. Which apply VIL on A0 pin, the device will output MXIC's manufacture code.. Which apply VIH on A0 pin, the device will output MX29LA32xMT/B device code.

VERIFY SECTOR GROUP PROTECT STATUS OPERATION

MX29LA32xMT/B provides hardware method for sector group protect status verify. Which method requires VID on A9 pin, VIH on WE# and A1 pins, VIL on CE#, OE#, A6, and A0 pins, and sector address on A16 to A20 pins. Which the identified sector is protected, the device will output 01H. Which the identified sector is not protect, the device will output 00H.

DATA PROTECTION

The MX29LA32xMT/B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

SECURED SILICON SECTOR

The MX29LA32xMT/B features a OTP memory region where the system may access through a command sequence to create a permanent part identification as so called Electronic Serial Number (ESN) in the device. Once this region is programmed, any further modification on the region is impossible. The secured silicon sector is a 128 words in length, and uses a Secured Silicon Sector Indicator Bit (Q7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevent duplication of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The MX29LA32xMT/B offers the device with Secured Silicon Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory , and has the Secured Silicon Sector Indicator Bit permanently set to a "1". The customer-lockable version is shipped with the Secured Silicon Sector unprotected, allowing customers to utilize that sector in any form they prefer. The customer-lockable version has the secured sector Indicator Bit permanently set to a "0". Therefore, the Secured Silicon Sector Indicator Bit prevents customer, lockable device from being used to replace devices that are factory locked.

The system access the Secured Silicon Sector through a command sequence (refer to "Enter Secured Silicon/ Exit Secured Silicon Sector command Sequence). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the address normally occupied by the first sector SA0. Once entry the Secured Silicon Sector the operation of boot sectors is disabled but the operation of main sectors is as normally. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending command to sector SA0.

Secured Silicon Sector address range	ESN factory locked	Customer lockable
000000h-000007h	ESN	Determined by Customer
000008h-00007Fh	Unavailable	

FACTORY LOCKED:Secured Silicon Sector Programmed and Protected At the Factory

In device with an ESN, the Secured Silicon Sector is protected when the device is shipped from the factory. The Secured Silicon Sector cannot be modified in any way. A factory locked device has an 8-word random ESN at address 000000h-000007h.

CUSTOMER LOCKABLE:Secured Silicon Sector NOT Programmed or Protected At the Factory

As an alternative to the factory-locked version, the device may be ordered such that the customer may program and protect the 128-word Secured Silicon Sector. Programming and protecting the Secured Silicon Sector must be used with caution since, once protected, there is no procedure available for unprotected the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

The Secured Silicon Sector area can be protected using one of the following procedures:

Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 15, except that RESET# may be at either VIH or VID. This allows in-system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that method is only applicable to the Secured Silicon Sector.

Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then alternate method of sector protection described in the :Sector Group Protection and Unprotect" section.

Once the Secured Silicon Sector is programmed, locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing the remainder of the array.

LOW VCC WRITE INHIBIT

When VCC is less than VLKO the device does not accept any write cycles. This protects data during VCC power-up and power-down. The command register and all

internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until VCC is greater than VLKO. The system must provide the proper signals to the control pins to prevent unintentional write when VCC is greater than VLKO.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns (typical) on CE# or WE# will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of OE# = VIL, CE# = VIH or WE# = VIH. To initiate a write cycle CE# and WE# must be a logical zero while OE# is a logical one.

POWER-UP SEQUENCE

The MX29LA32xMT/B powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

POWER-UP WRITE INHIBIT

If WE#=CE#=VIL and OE#=VIH during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

POWER SUPPLY DE COUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

SOFTWARE COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 3 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device (when applicable).

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data are latched on rising edge of WE# or CE#, whichever happens first.

TABLE 3. MX29LA32xMT/B COMMAND DEFINITIONS

Command		Bus	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Cycles	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Automatic Select (Note 7)														
Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	C2H				
	Byte	4	AAA	AA	555	55	AAA	90	X00	C2H				
Device ID (Note 8)	Word	4	555	AA	2AA	55	555	90	X01	227EH	X0E	221A	X0F	2200/2201
	Byte	4	AAA	AA	555	55	AAA	90	X02	7E	X1C	1A	X1E	00/01
Secured Sector Factory Protect (Note 9)	Word	4	555	AA	2AA	55	555	90	X03	see Note 9				
	Byte	4	AAA	AA	555	55	AAA	90	X06					
Sector Group Protect Verify (Note 10)	Word	4	555	AA	2AA	55	555	90	(SA)X02	XX00/XX01				
	Byte	4	AAA	AA	555	55	AAA	90	(SA)X04					
Enter Secured Silicon Sector	Word	3	555	AA	2AA	55	555	88						
	Byte	3	AAA	AA	555	55	AAA	88						
Exit Secured Silicon Sector	Word	4	555	AA	2AA	55	555	90	XXX	00				
	Byte	4	AAA	AA	555	55	AAA	90	XXX	00				
Program	Word	4	555	AA	2AA	55	555	A0	PA	PD				
	Byte	4	AAA	AA	555	55	AAA	A0	PA	PD				
Write to Buffer (Note 11)	Word	6	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
	Byte	6	AAA	AA	555	55	SA	25	SA	BC	PA	PD	WBL	PD
Program Buffer to Flash	Word	1	SA	29										
	Byte	1	SA	29										
Write to Buffer Abort Reset (Note 12)	Word	3	555	AA	2AA	55	555	F0						
	Byte	3	AAA	AA	555	55	AAA	F0						
Chip Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Byte	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Byte	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Program/Erase Suspend (Note 13)		1	XXX	B0										
Program/Erase Resume (Note 14)		1	XXX	30										
CFI Query (Note 15)	Word	1	55	98										
	Byte	1	AA	98										

Legend:
X=Don't care
RA=Address of the memory location to be read.
RD=Data read from location RA during read operation.
PA=Address of the memory location to be programmed.
Addresses are latched on the falling edge of the WE# or CE# pulse, whichever happen later.
DDI=Data of device identifier
C2H for manufacture code

PD=Data to be programmed at location PA. Data is latched on the rising edge of WE# or CE# pulse.
SA=Address of the sector to be erase or verified (in autoselect mode).
Address bits A20-A12 uniquely select any sector.
WBL=Write Buffer Location. Address must be within the same write buffer page as PA.
WC=Word Count. Number of write buffer locations to load minus 1.
BC=Byte Count. Number of write buffer locations to load minus 1.

Notes:
1. See Table 1 for descriptions of bus operations.
2. All values are in hexadecimal.
3. Except when reading array or automatic select data, all bus cycles are write operation.
4. Address bits are don't care for unlock and command cycles, except when PA or SA is required.
5. No unlock or command cycles required when device is in read mode.
6. The Reset command is required to return to the read mode when the device is in the automatic select mode or if Q5 goes high.
7. The fourth cycle of the automatic select command sequence is a read cycle.
8. The device ID must be read in three cycles. The data is 01h for top boot and 00h for bottom boot.
9. If WP# protects the top two address sectors, the data is 98h for factory locked and 18h for not factory locked. If WP# protects the bottom two address sectors, the data is 88h for factory locked and 08h for not factor locked.
10. The data is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block.
11. The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 21(Word Mode) / 37(Byte Mode).
12. Command sequence resets device for next command after aborted write-to-buffer operation.
13. The system may read and program functions in non-erasing sectors, or enter the automatic select mode, when in the erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
14. The Erase Resume command is valid only during the Erase Suspend mode.
15. Command is valid when device is ready to read array data or when device is in automatic select mode.

READING ARRAY DATA

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Automatic Program or Automatic Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Erase Suspend/Erase Resume Commands for more information on this mode. The system must issue the reset command to re-enable the device for reading array data if Q5 goes high, or while in the automatic select mode. See the "Reset Command" section, next.

RESET COMMAND

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an SILICON ID READ command sequence. Once in the SILICON ID READ mode, the reset command must be written to return to reading array data (also applies to SILICON ID READ during Erase Suspend).

If Q5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

SILICON ID READ COMMAND SEQUENCE

The SILICON ID READ command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table 2 shows the address and data requirements. This method is an alternative to that shown in Table 1, which is intended for PROM programmers and requires VID on address bit A9.

The SILICON ID READ command sequence is initiated by writing two unlock cycles, followed by the SILICON ID READ command. The device then enters the SILICON ID READ mode, and the system may read at any address any number of times, without initiating another command sequence. A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table for valid sector addresses.

The system must write the reset command to exit the automatic select mode and return to reading array data.

BYTE/WORD PROGRAM COMMAND SEQUENCE

The command sequence requires four bus cycles, and is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 3 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using Q7, Q6, or RY/BY#. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hard-

ware reset immediately terminates the programming operation. The Byte/Word Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a "0" back to a "1". Attempting to do so may halt the operation and set Q5 to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming will occur. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system will program 6 unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits A_{MAX}-4. All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages. This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation will abort.

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter will be decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Note also that if an address location is loaded more than once into the buffer, the final data loaded for that address will be programmed.

Once the specified number of write buffer locations have been loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. Q7, Q6, Q5, and Q1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

The abort condition is indicated by Q1 = 1, Q7 = DATA# (for the last address location loaded), Q6 = toggle, and Q5=0. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer

programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15us maximum (5 us typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. See Write Operation Status for more information.

SETUP AUTOMATIC CHIP/SECTOR ERASE

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H, or the sector erase command 30H.

The MX29LA32xMT/B contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL,A0=VIL retrieves the manufacturer code of C2H.

AUTOMATIC CHIP/SECTOR ERASE COMMAND

The device does not require the system to preprogram prior to erase. The Automatic Erase algorithm automatically pre-program and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 3 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Automatic Erase algorithm are ignored. Note that a hardware reset during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using Q7, Q6, Q2, or RY/BY#. See "Write Operation Status" for information on these status bits. When the Automatic Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 10 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to Figure 9 for timing diagrams.

SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system is not required to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verify begin. The erase and verify operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of WE# or CE#, whichever happens later , while the command (data) is latched on the rising edge of WE# or CE#, whichever happens first. Sector addresses selected are loaded into internal register on the sixth falling edge of WE# or CE#, whichever happens later. Each successive sector load cycle started by the falling edge of WE# or CE#, whichever happens later must begin within 50us from the rising edge of the preceding WE# or CE#, whichever happens first. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase(30H) or Erase Suspend(B0H) during the time-out period resets the device to read mode.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. When the Erase Suspend command is issued during the sector erase operation, the device requires a maximum 20us to suspend the sector erase operation. However, When the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Erase Resume, program data to, or read data from any sector not selected for erasure.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended blocks.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions. Another Erase Suspend command can be written after the chip has resumed erasing.

QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LA32xMT/B is capable of operating in the CFI mode. This mode all the host system to determine the manufacturer of the device such as operating parameters and configuration. Two commands are required in CFI mode. Query command of CFI mode is placed first, then the Reset command exits CFI mode. These are described in Table 4.

The single cycle Query command is valid only when the device is in the Read mode, including Erase Suspend, Standby mode, and Read ID mode; however, it is ignored otherwise.

The Reset command exits from the CFI mode to the Read mode, or Erase Suspend mode, or read ID mode. The command is valid only when the device is in the CFI mode.

Table 4-1. CFI mode: Identification Data Values
(All values in these tables are in hexadecimal)

Description	Address h (x16)	Address h (x8)	Data h
Query-unique ASCII string "QRY"	10	20	0051
	11	22	0052
	12	24	0059
Primary vendor command set and control interface ID code	13	26	0002
	14	28	0000
Address for primary algorithm extended query table	15	2A	0040
	16	2C	0000
Alternate vendor command set and control interface ID code (none)	17	2E	0000
	18	30	0000
Address for secondary algorithm extended query table (none)	19	32	0000
	1A	34	0000

Table 4-2. CFI Mode: System Interface Data Values

Description	Address h (x16)	Address h (x8)	Data h
VCC supply, minimum (2.7V)	1B	36	0027
VCC supply, maximum (3.6V)	1C	38	0036
VPP supply, minimum (none)	1D	3A	0000
VPP supply, maximum (none)	1E	3C	0000
Typical timeout for single word/byte write (2^N us)	1F	3E	0007
Typical timeout for maximum size buffer write (2^N us)	20	40	0007
Typical timeout for individual block erase (2^N ms)	21	42	000A
Typical timeout for full chip erase (2^N ms)	22	44	0000
Maximum timeout for single word/byte write times (2^N X Typ)	23	46	0001
Maximum timeout for maximum size buffer write times (2^N X Typ)	24	48	0005
Maximum timeout for individual block erase times (2^N X Typ)	25	4A	0004
Maximum timeout for full chip erase times (not supported)	26	4C	0000

Table 4-3. CFI Mode: Device Geometry Data Values

Description	Address h (x16)	Address h (x8)	Data h
Device size (2^n bytes)	27	4E	0016
Flash device interface code (02=asynchronous x8/x16)	28	50	0002
	29	52	0000
Maximum number of bytes in multi-byte write = 2^n	2A	54	0005
	2B	56	0000
Number of erase block regions	2C	58	0002
Erase block region 1 information	2D	5A	0007
[2E,2D] = # of blocks in region -1	2E	5C	0000
[30, 2F] = size in multiples of 256-bytes	2F	5E	0020
	30	60	0000
	31	62	003E
Erase Block Region 2 Information (refer to CFI publication 100)	32	64	0000
	33	66	0000
	34	68	0001
	35	6A	0000
Erase Block Region 3 Information (refer to CFI publication 100)	36	6C	0000
	37	6E	0000
	38	70	0000
	39	72	0000
Erase Block Region 4 Information (refer to CFI publication 100)	3A	74	0000
	3B	76	0000
	3C	78	0000

Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address h (x16)	Address h (x8)	Data h
Query-unique ASCII string "PRI"	40	80	0050
	41	82	0052
	42	84	0049
Major version number, ASCII	43	86	0031
Minor version number, ASCII	44	88	0033
Address sensitive unlock (0=required, 1= not required)	45	8A	0000
Erase suspend (2= to read and write)	46	8C	0002
Sector protect (N= # of sectors/group)	47	8E	0001
Temporary sector unprotect (1=supported)	48	90	0000
Sector protect/unprotect scheme	49	92	0004
Simultaneous R/W operation (0=not supported)	4A	94	0000
Burst mode type (0=not supported)	4B	96	0000
Page mode type (1= 4 word page)	4C	98	0001
ACC (Acceleration) Supply Minimum 00h=Not Supported, D7-D4: Volt, D3-D0:100mV	4D	9A	00B5
ACC (Acceleration) Supply Maximum 00h=Not Supported, D7-D4: Volt, D3-D0:100mV	4E	9C	00C5
Top/Bottom Boot Sector Flag 02h=Bottom Boot Device, 03h=Top Boot Device	4F	9E	0002/ 0003
Program Suspend 00h=Not Supported, 01h=Supported	50	A0	0001

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: Q2, Q3, Q5, Q6, Q7, and RY/BY#. Table 5 and the following subsections describe the functions of these bits. Q7, RY/BY#, and Q6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

Table 5. Write Operation Status

Status		Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Byte/Word Program in Auto Program Algorithm		Q7#	Toggle	0	N/A	No Toggle	0	0
Auto Erase Algorithm		0	Toggle	0	1	Toggle	N/A	0
Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle	N/A	1
	Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data	Data	1
	Erase Suspend Program	Q7#	Toggle	0	N/A	N/A	N/A	0
Program Suspend	Program-Suspended Read (Program-Suspended Sector)	Invalid (not allowed)						1
	Program-Suspended Read (Non-Program-Suspended Sector)	Data						1
Write-to-Buffer	Busy	Q7#	Toggle	0	N/A	N/A	0	0
	Abort	Q7#	Toggle	0	N/A	N/A	1	0

Notes:
1. Q5 switches to "1" when an Word/Byte Program, Erase, or Write-to-Buffer operation has exceeded the maximum timing limits. Refer to the section on Q5 for more information.
2. Q7 and Q2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
3. The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.
4. Q1 switches to "1" when the device has aborted the write-to-buffer operation.

Q7: Data# Polling

The Data# Polling bit, Q7, indicates to the host system whether an Automatic Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Automatic Program algorithm, the device outputs on Q7 the complement of the datum programmed to Q7. This Q7 status also applies to programming during Erase Suspend. When the Automatic Program algorithm is complete, the device outputs the datum programmed to Q7. The system must provide the program address to read valid status information on Q7. If a program address falls within a protected sector, Data# Polling on Q7 is active for approximately 1 us, then the device returns to reading array data.

During the Automatic Erase algorithm, Data# Polling produces a "0" on Q7. When the Automatic Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on Q7. This is analogous to the complement/true datum output described for the Automatic Program algorithm: the erase function changes all the bits in a sector to "1" prior to this, the device outputs the "complement," or "0". The system must provide an address within any of the sectors selected for erasure to read valid status information on Q7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on Q7 is active for approximately 100 us, then the device returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects Q7 has changed from the complement to true data, it can read valid data at Q7-Q0 on the following read cycles. This is because Q7 may change asynchronously with Q0-Q6 while Output Enable (OE#) is asserted low.

Q6:Toggle BIT I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# or CE#, whichever happens first pulse in the command sequence (prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles for 100us and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected sector, Q6 toggles for approximately 2us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 5 shows the outputs for Toggle Bit I on Q6.

Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively erasing (that is, the Automatic Erase algorithm is in process), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# or CE#, whichever happens first pulse in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by com-

parison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 5 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

Q5:Program/Erase Timing

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data# Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte/word programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

The Q5 failure condition may appear if the system tries to program a to a "1" location that is previously programmed to "0". Only an erase operation can change a "0" back to a "1". Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, Q5 produces a "1".

Q3:Sector Erase Timer

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data# Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data# Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data# Polling or

Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

If the time between additional erase commands from the system can be less than 50us, the system need not to monitor Q3.

Q1: Write-to-Buffer Abort

Q1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions Q1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See Write Buffer section for more details.

RY/BY#:READY/BUSY OUTPUT

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to VCC .

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature

Plastic Packages . . . . -65°C to +150°C

Ambient Temperature

with Power Applied. . . . . -65°C to +125°C

Voltage with Respect to Ground

VCC (Note 1) . . . . . -0.5 V to +4.0 V

A9, OE#, and

RESET# (Note 2) . . . .-0.5 V to +12.5 V

All other pins (Note 1) . . . . . -0.5 V to VCC +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may overshoot VSS to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is VCC +0.5 V. During voltage transitions, input or I/O pins may overshoot to VCC +2.0 V for periods up to 20ns.
2. Minimum DC input voltage on pins A9, OE#, and RESET# is -0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot VSS to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RATINGS

Commercial (C) Devices

Ambient Temperature (T_A). . . . . 0° C to +70° C

Industrial (I) Devices

Ambient Temperature (T_A). . . . . -40° C to +85° C

VCC Supply Voltages

VCC for full voltage range. . . . . +2.7 V to 3.6 V

VCC for regulated voltage range. . . . . +3.0 V to 3.6 V

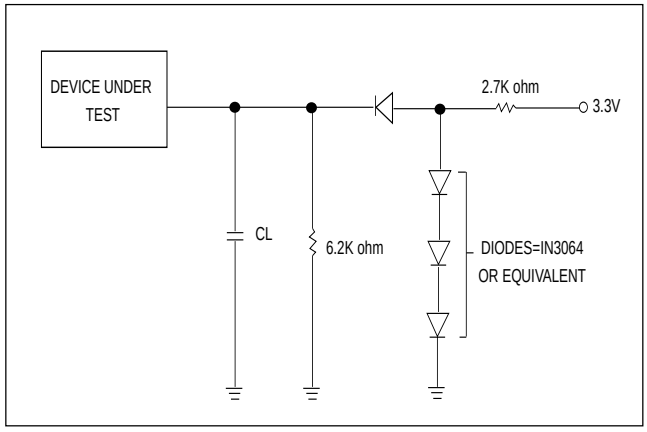
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS TA=-40° C to 85° C, VCC=2.7V~3.6V (TA=0° C to 70° C, VCC=3.0V~3.6V for 70R)

Para-meter	Description	Test Conditions		Min.	Typ.	Max.	Unit
I LI	Input Load Current (Note 1)	VIN = VSS to VCC , VCC = VCC max				±1.0	uA
I LIT	A9 Input Leakage Current	VCC=VCC max; A9 = 12.5V				35	uA
I LO	Output Leakage Current	VOUT = VSS to VCC , VCC= VCC max				±1.0	uA
ICC1	VCC Initial Read Current (Notes 2,3)	CE#= VIL, OE# = VIH	10 MHz		35	50	mA
			5 MHz		18	25	mA
			1 MHz		5	20	mA
ICC2	VCC Intra-Page Read Current (Notes 2,3)	CE#= VIL , OE# = VIH	10 MHz		5	20	mA
			40 MHz		10	40	mA
ICC3	VCC Active Write Current (Notes 2,4,6)	CE#= VIL , OE# = VIH WE#=VIL			50	60	mA
ICC4	VCC Standby Current (Note 2)	CE#,RESET#=VCC±0.3V WP#=VIH			20	50	uA
ICC5	VCC Reset Current (Note 2)	RESET#=VSS±0.3V WP#=VIH			20	50	uA
ICC6	Automatic Sleep Mode (Notes 2,5)	VIL = V SS ± 0.3 V, VIH = VCC ± 0.3 V, WP#=VIH			20	50	uA
VIL	Input Low Voltage			-0.5		0.8	V
VIH	Input High Voltage			0.7xVCC		VCC+0.5	V
VHH	Voltage for ACC Program Acceleration	VCC = 2.7V ~ 3.6V		11.5	12.0	12.5	V
VID	Voltage for Autoselect	VCC = 3.0 V ±10%		11.5	12.0	12.5	V
VOL	Output Low Voltage	IOL= 4.0mA,VCC=VCC min				0.45	V
VOH1	Output High Voltage	IOH=-2.0mA,VCC=VCC min		0.85VCC			V
VOH2		IOH=-100uA,VCC=VCC min		VCC-0.4			V
VLKO	Low VCC Lock-Out Voltage (Note 4)			2.3		2.5	V

Notes:
1. On the WP#/ACC pin only, the maximum input load current when WP# = VIL is ±5.0uA.
2. Maximum ICC specifications are tested with VCC = VCC max.
3. The ICC current listed is typically is less than 2 mA/MHz, with OE# at VIH. Typical specifications are for VCC = 3.0V.
4. ICC active while Embedded Erase or Embedded Program is in progress.
5. Automatic sleep mode enables the low power mode when addresses remain stable for t ACC + 30 ns.
6. Not 100% tested.
7. A9=12.5V when TA=0° C to 85° C, A9=12V when when TA=-40° C to 0° C.

SWITCHING TEST CIRCUITS



TEST SPECIFICATIONS

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, CL (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0-3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State(High Z)

SWITCHING TEST WAVEFORMS

AC CHARACTERISTICS

Read-Only Operations TA=-40° C to 85° C, VCC=2.7V~3.6V (TA=0° C to 70° C, VCC=3.0V~3.6V for 70R)

Parameter Std.	Description		Test Setup		Speed Options		Unit
					70R	90	
tRC	Read Cycle Time (Note 1)			Min	70	90	ns
tACC	Address to Output Delay		CE#, OE#=VIL	Max	70	90	ns
tCE	Chip Enable to Output Delay		OE#=VIL	Max	70	90	ns
tPACC	Page Access Time			Max	25	25	ns
tOE	Output Enable to Output Delay			Max	35	35	ns
tDF	Chip Enable to Output High Z (Note 1)			Max	16		ns
tDF	Output Enable to Output High Z (Note 1)			Max	16		ns
tOH	Output Hold Time From Address, CE# or OE#, whichever Occurs First			Min	0		ns
tOEH	Output Enable Hold Time (Note 1)	Read		Min	35		ns
		Toggle and Data# Polling		Min	10		ns

Notes:
1. Not 100% tested.
2. See SWITCHING TEST CIRCUITS and TEST SPECIFICATIONS TABLE for test specifications.

Figure 1. READ TIMING WAVEFORMS

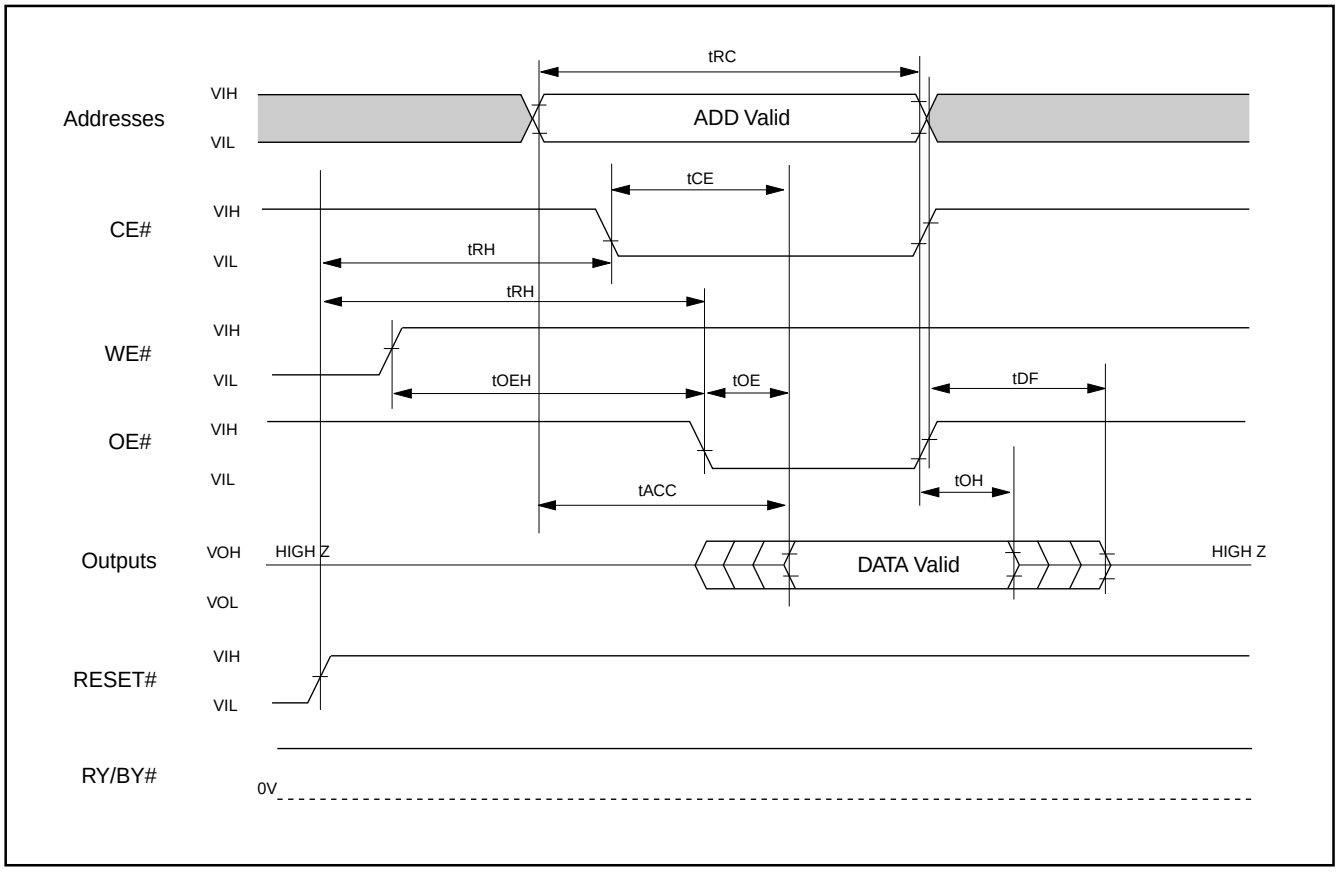
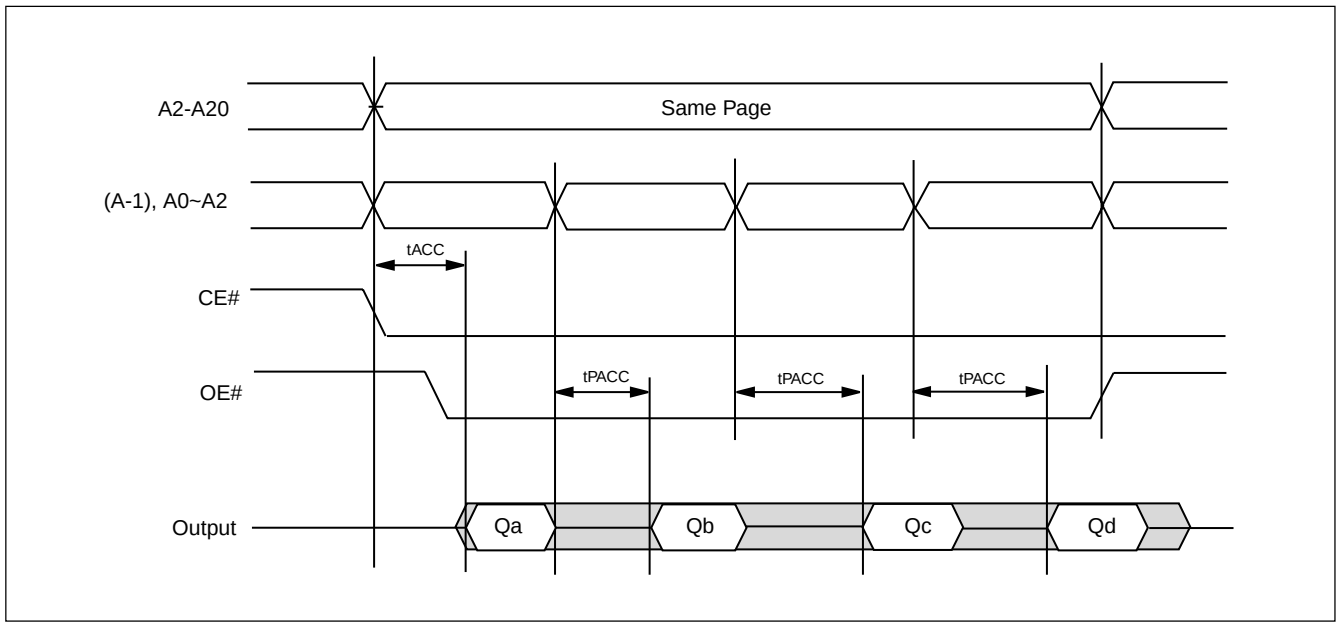


Figure 2. PAGE READ TIMING WAVEFORMS

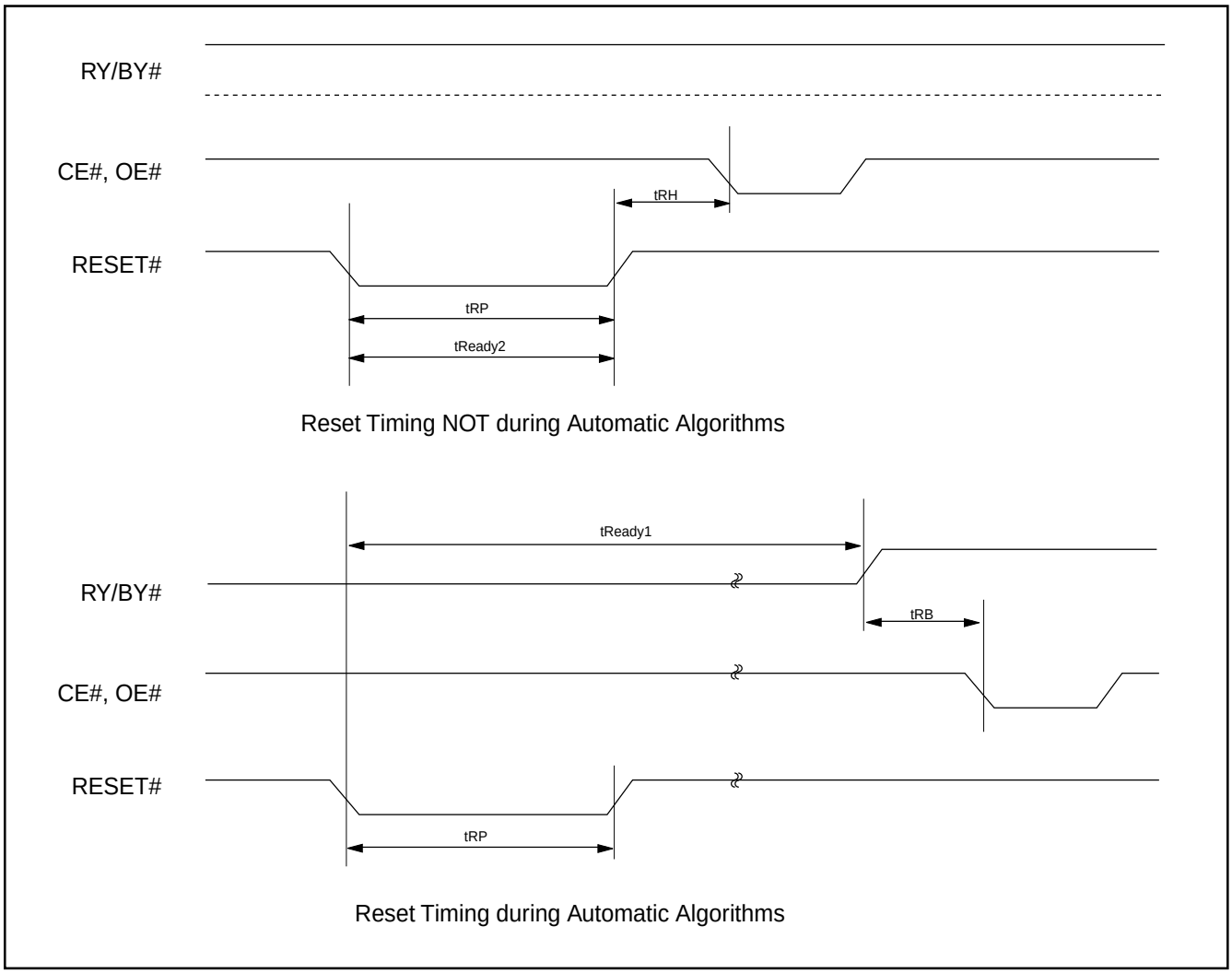


AC CHARACTERISTICS

Parameter	Description	Test Setup	All Speed Options	Unit
tREADY1	RESET# PIN Low (During Automatic Algorithms) to Read or Write (See Note)	MAX	20	us
tREADY2	RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write (See Note)	MAX	500	ns
tRP	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
tRH	RESET# High Time Before Read (See Note)	MIN	50	ns
tRB	RY/BY# Recovery Time(to CE#, OE# go low)	MIN	0	ns
tRPD	RESET# Low to Standby Mode	MIN	20	us

Note:Not 100% tested

Figure 3. RESET# TIMING WAVEFORM



AC CHARACTERISTICS

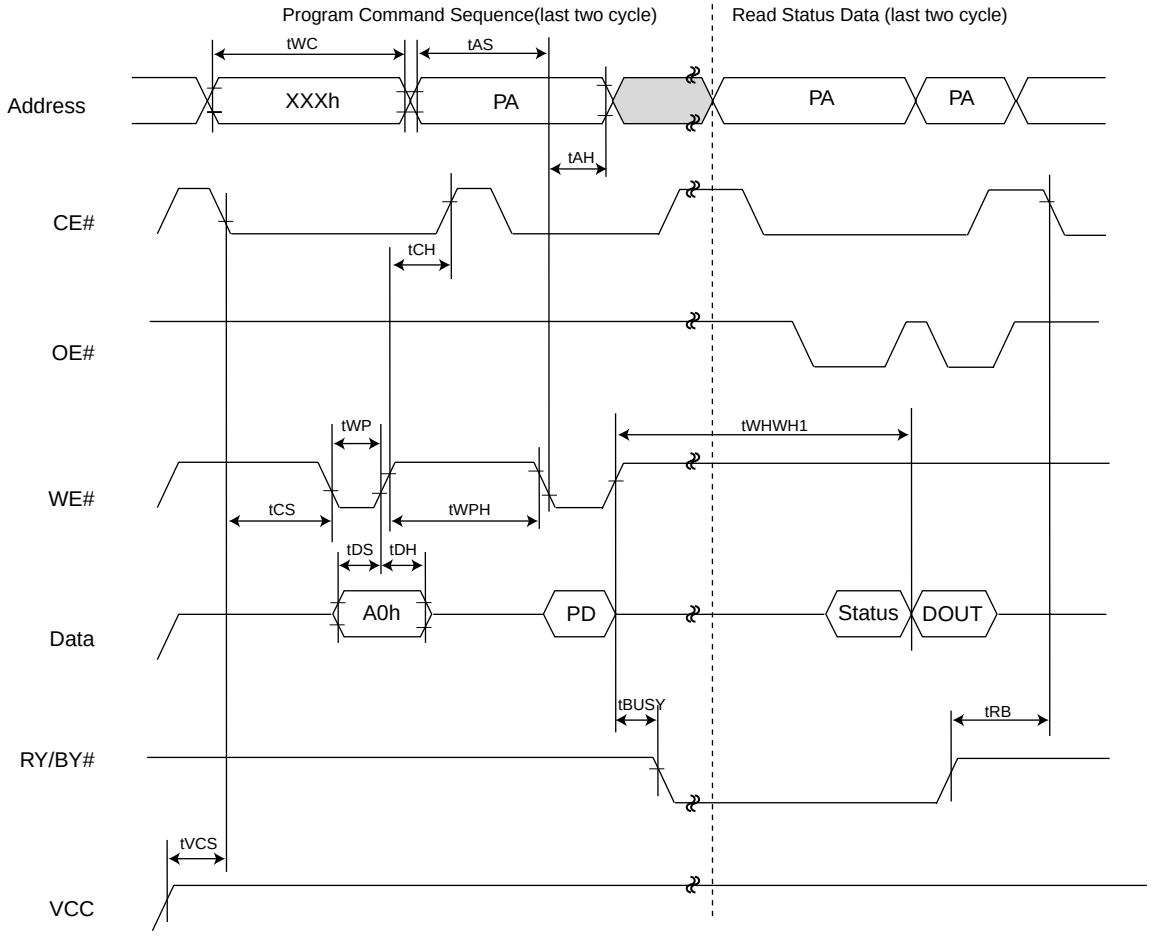
Erase and Program Operations TA=-40°C to 85°C, VCC=2.7V~3.6V (TA=0°C to 70°C, VCC= 3.0V~3.6V for 70R)

Parameter Std.	Description			Speed Options 70R	Speed Options 90	Unit
tWC	Write Cycle Time (Note 1)		Min	70	90	ns
tAS	Address Setup Time		Min	0		ns
tASO	Address Setup Time to OE# low during toggle bit polling		Min	15		ns
tAH	Address Hold Time		Min	45		ns
tAHT	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0		ns
tDS	Data Setup Time		Min	35		ns
tDH	Data Hold Time		Min	0		ns
tCEPH	CE# High During Toggle Bit Polling		Min	20		ns
tOEPH	Output Enable High during toggle bit polling		Min	20		ns
tGHWL	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
tGHEL	Read Recovery Time Before Write		Min	0		ns
tCS	CE# Setup Time		Min	0		ns
tCH	CE# Hold Time		Min	0		ns
tWP	Write Pulse Width		Min	35		ns
tWPH	Write Pulse Width High		Min	30		ns
tWHWH1	Write Buffer Program Operation (Notes 2,3)		Typ	240		us
	Single Word/Byte Program Operation (Notes 2,5)	Byte	Typ	60		us
		Word	Typ	60		us
	Accelerated Single Word/Byte Programming Operation (Notes 2,5)	Byte	Typ	54		us
		Word	Typ	54		us
tWHWH2	Sector Erase Operation (Note 2)		Typ	0.5		sec
tVCS	VCC Setup Time (Note 1)		Min	50		us
tRB	Write Recovery Time from RY/BY#		Min	0		ns
tBUSY	Program/Erase Valid to RY/BY# Delay		Min	70	90	ns
tVHH	VHH Rise and Fall Time (Note 1)		Min	250		ns
tPOLL	Program Valid Before Status Polling (Note 6)		Max	4		us

Notes:
1. Not 100% tested.
2. See the "Erase And Programming Performance" section for more information.
3. For 1-16 words/1-32 bytes programmed.
4. Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.
5. Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.
6. When using the program suspend/resume feature, if the suspend command is issued within tPOLL, tPOLL must be fully re-applied upon resuming the programming operation. If the suspend command is issued after tPOLL, tPOLL is not required again prior to reading the status bits upon resuming.

ERASE/PROGRAM OPERATION

Figure 4. AUTOMATIC PROGRAM TIMING WAVEFORMS



Note :
1.PA=Program Address, PD=Program Data, DOUT is the true data the program address

Figure 5. ACCELERATED PROGRAM TIMING DIAGRAM

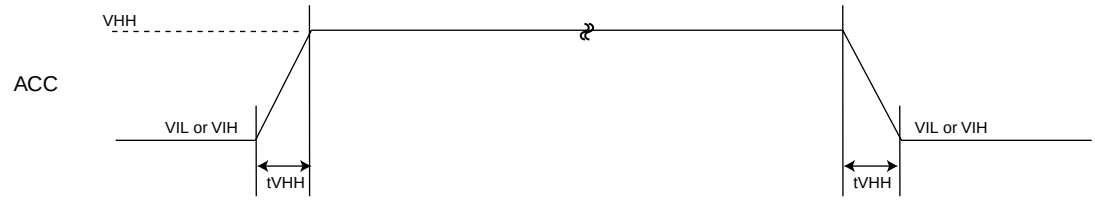


Figure 6. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART

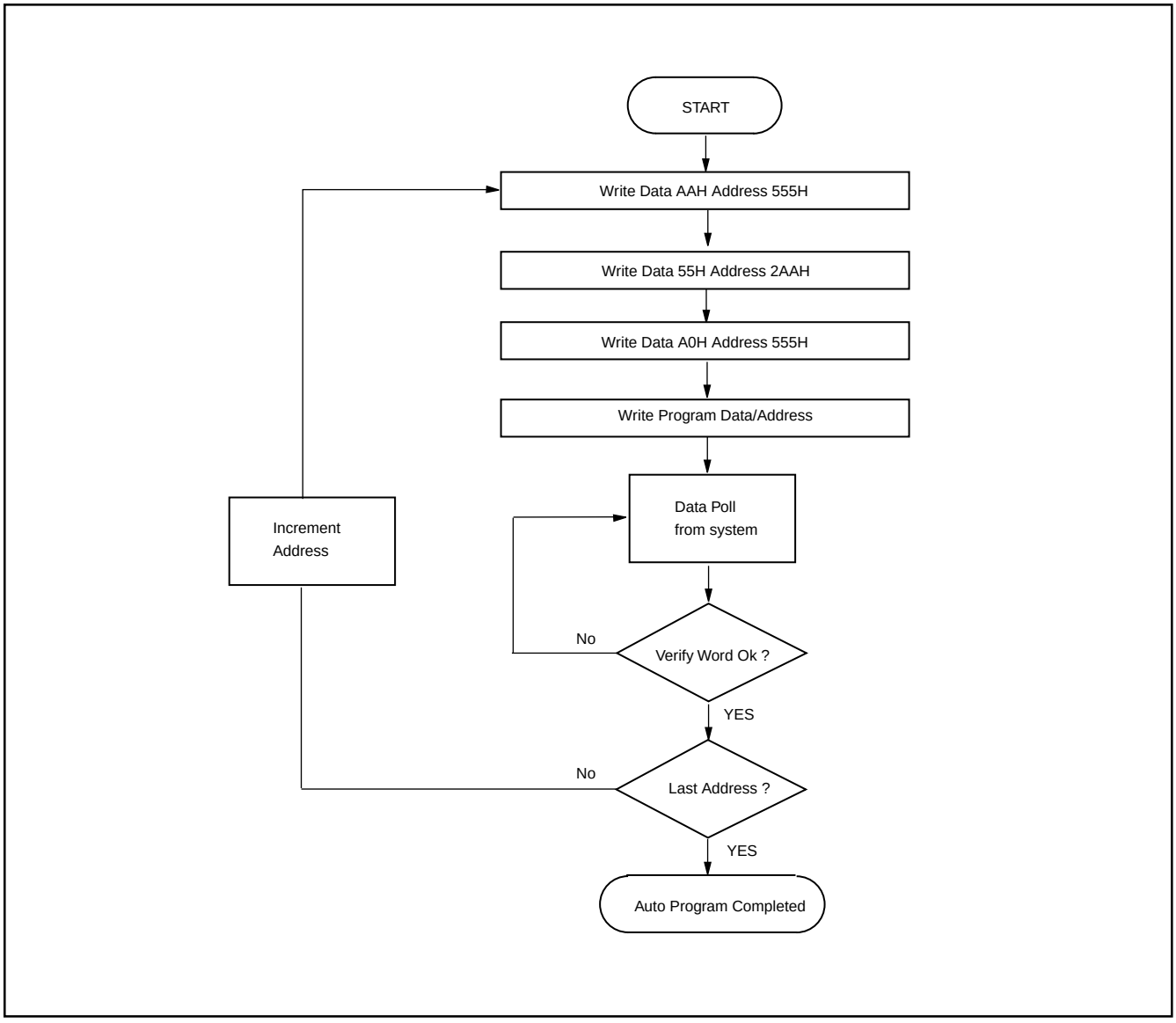
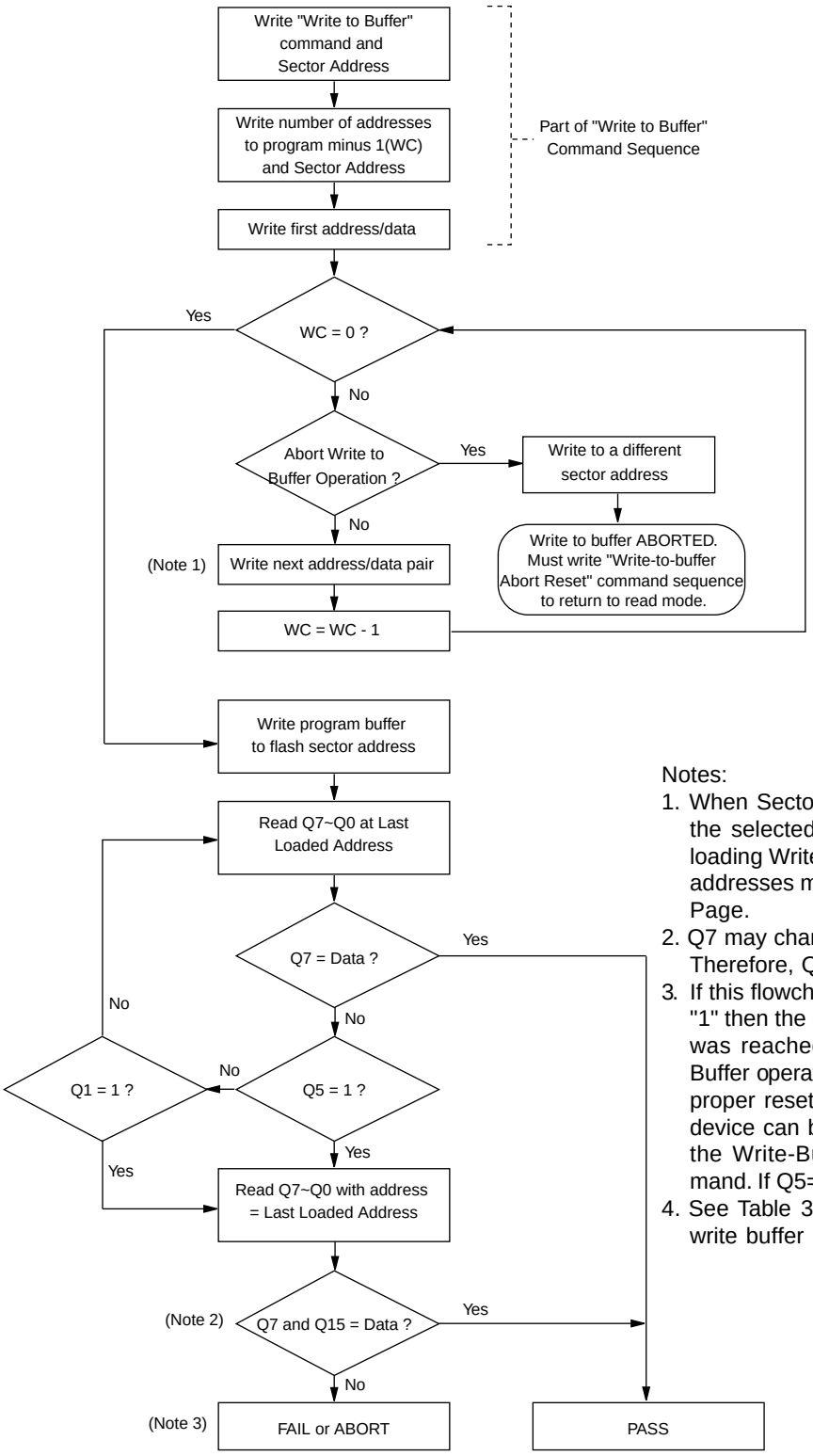


Figure 7. WRITE BUFFER PROGRAMMING ALGORITHM FLOWCHART



Notes:

1. When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.
2. Q7 may change simultaneously with Q5. Therefore, Q7 should be verified.
3. If this flowchart location was reached because Q5= "1" then the device FAILED. If this flowchart location was reached because Q1="1", then the Write to Buffer operation was ABORTED. In either case, the proper reset command must be written before the device can begin another operation. If Q1=1, write the Write-Buffer-Programming-Abort-Reset command. If Q5=1, write the Reset command.
4. See Table 3 for command sequences required for write buffer programming.

Figure 8. PROGRAM SUSPEND/RESUME FLOWCHART

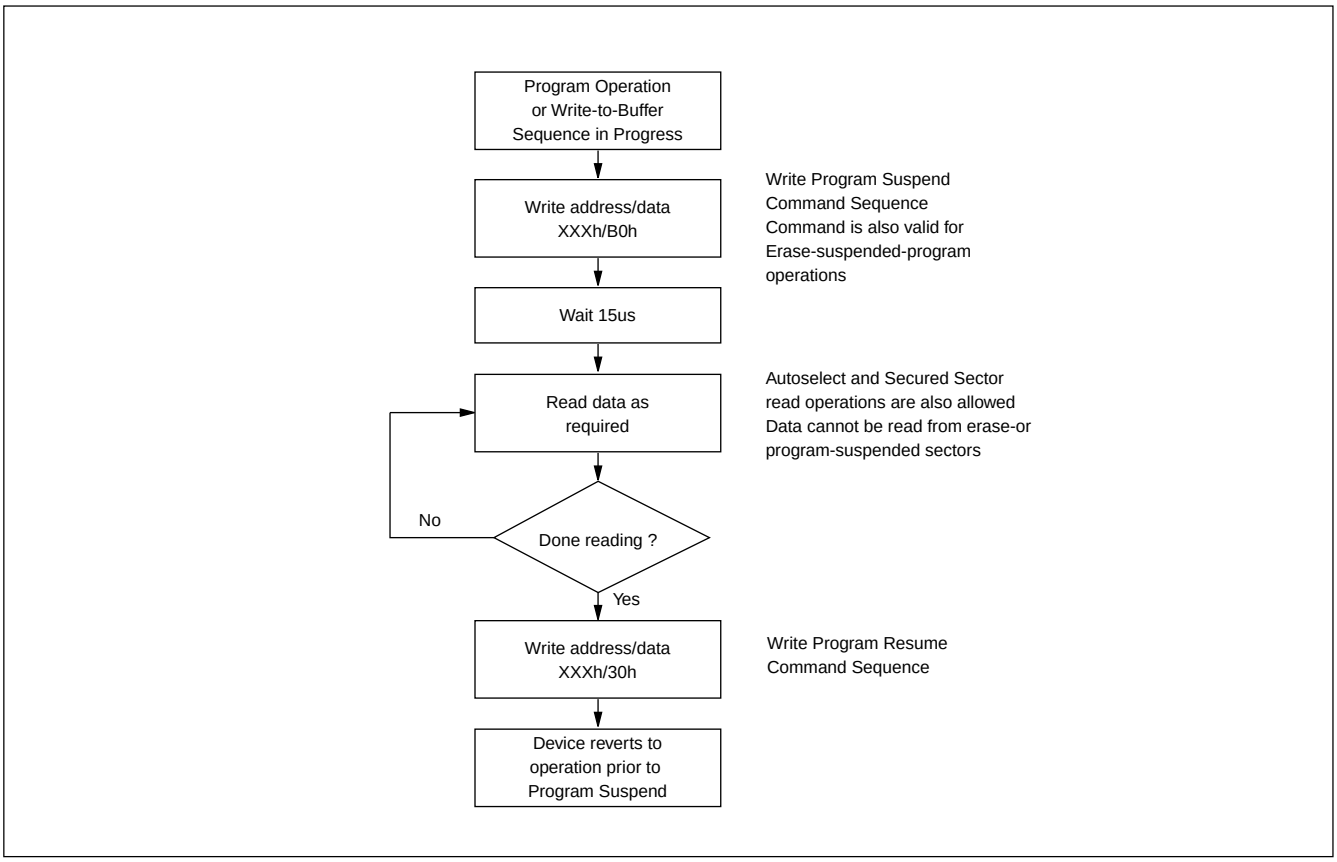
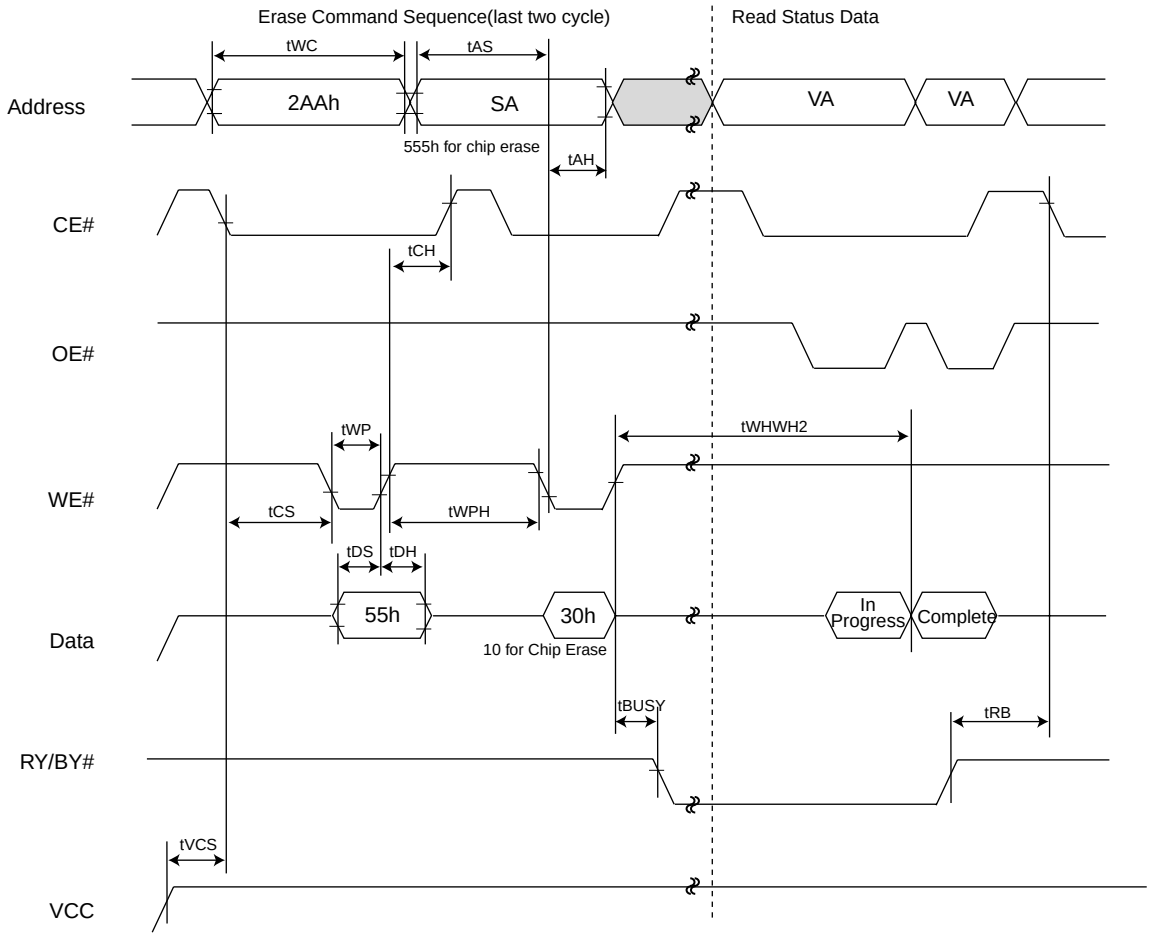


Figure 9. AUTOMATIC CHIP/SECTOR ERASE TIMING WAVEFORM



Note :

1. SA=sector address(for Sector Erase), VA=Valid Address for reading status data(see "Write Operation Status").

Figure 10. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

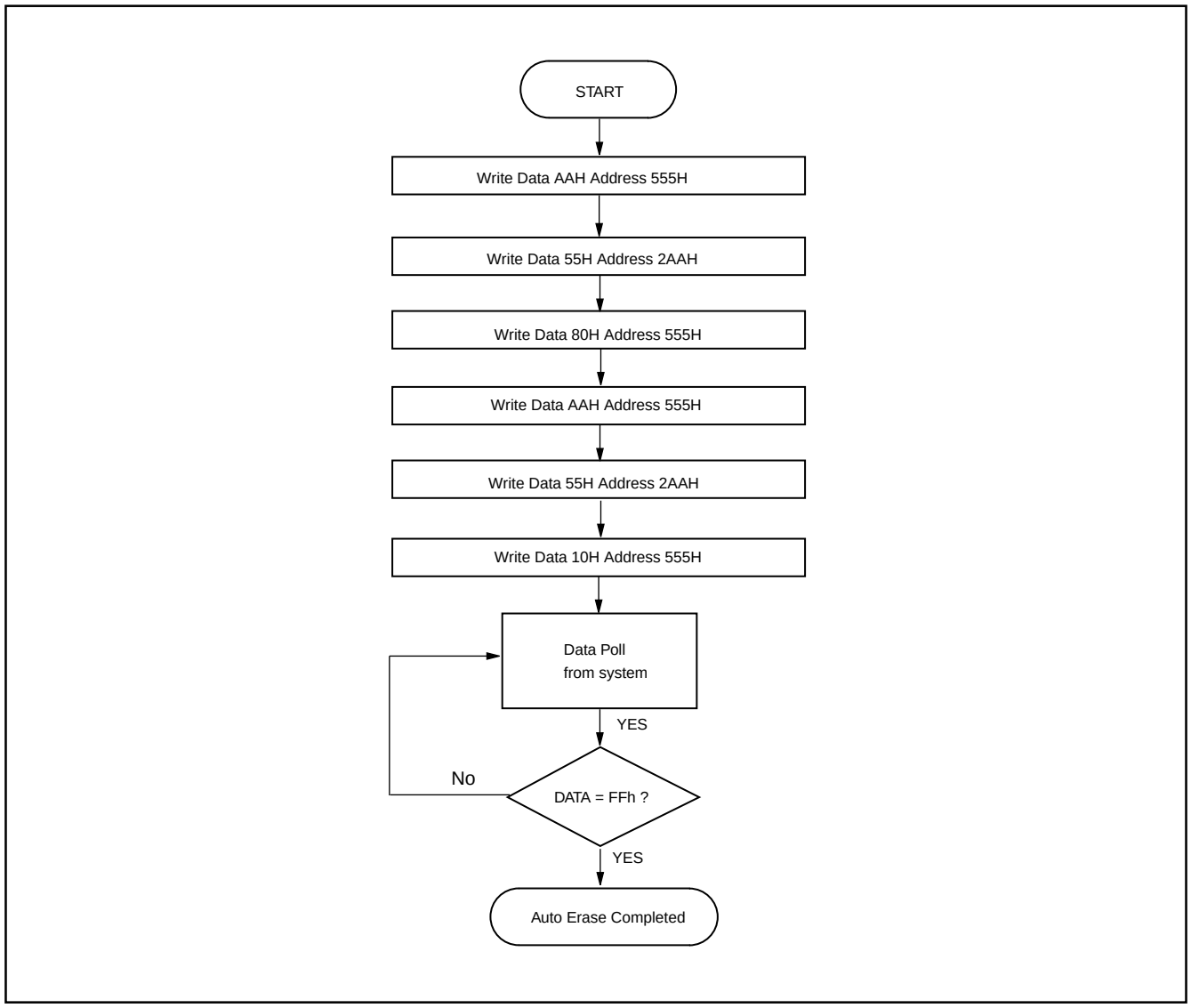


Figure 11. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART

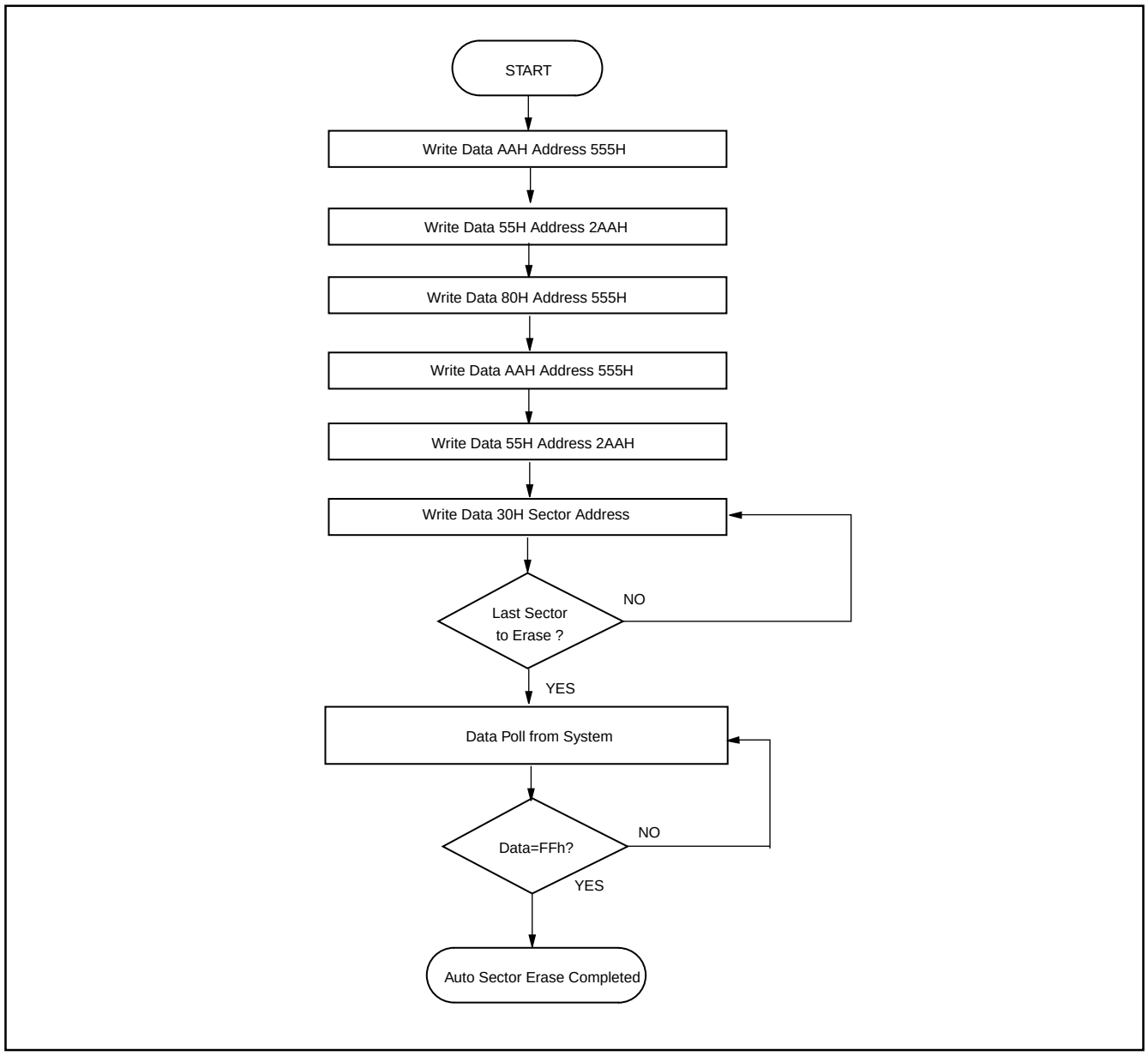
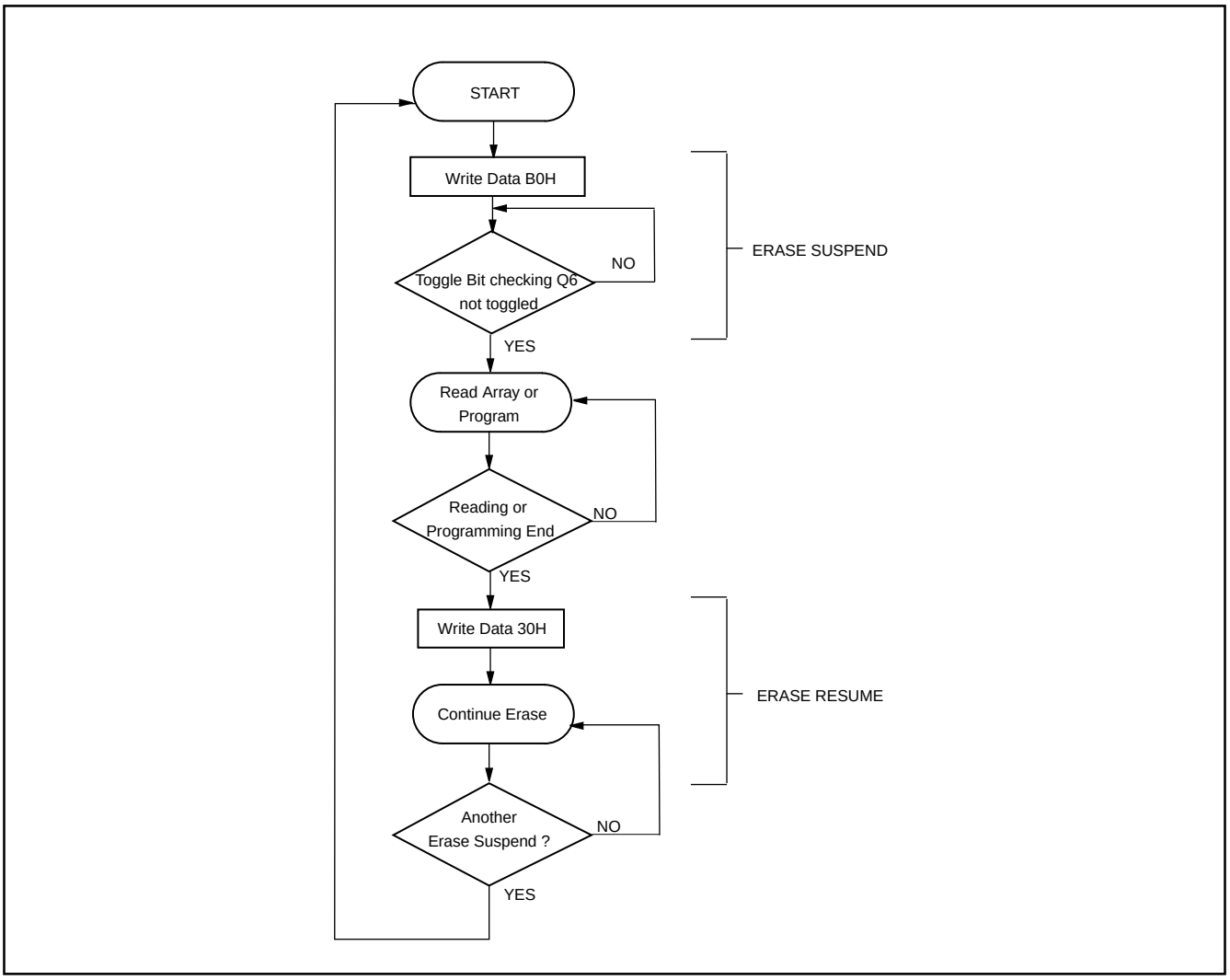


Figure 12. ERASE SUSPEND/RESUME FLOWCHART



AC CHARACTERISTICS

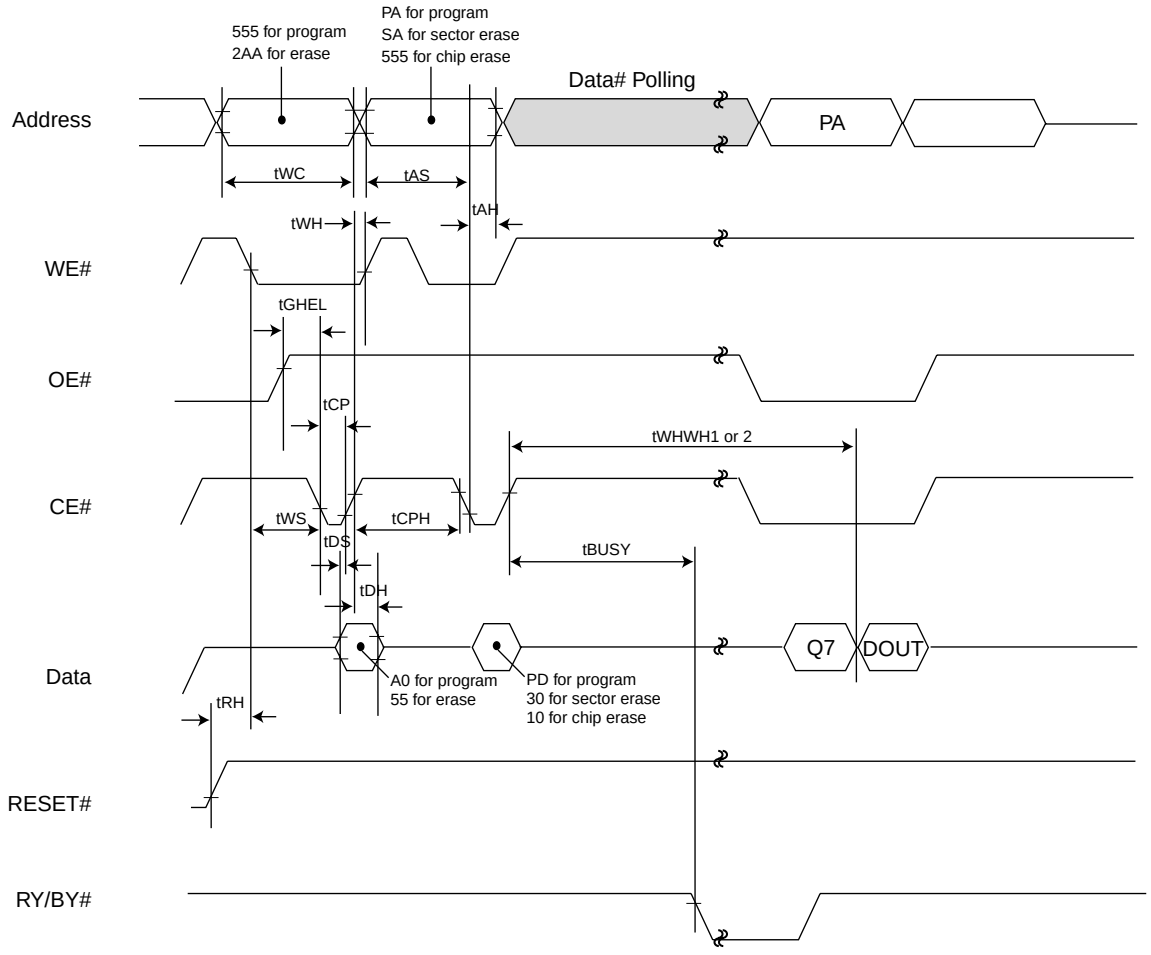
Alternate CE# Controlled Erase and Program Operations

TA=-40° C to 85° C, VCC=2.7V~3.6V (TA=0° C to 70° C, VCC=3.0V~3.6V for 70R)

Parameter Std.	Description			Speed Options 70R	Speed Options 90	Unit
tWC	Write Cycle Time (Note 1)		Min	70	90	ns
tAS	Address Setup Time		Min	0		ns
tAH	Address Hold Time		Min	45		ns
tDS	Data Setup Time		Min	35		ns
tDH	Data Hold Time		Min	0		ns
tGHEL	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
tWS	WE# Setup Time		Min	0		ns
tWH	WE# Hold Time		Min	0		ns
tCP	CE# Pulse Width		Min	35		ns
tCPH	CE# Pulse Width High		Min	25		ns
tWHWH1	Write Buffer Program Operation (Notes 2,3)		Typ	240		us
	Single Word/Byte Program Operation (Notes 2,5)	Byte	Typ	60		us
		Word	Typ	60		us
	Accelerated Single Word/Byte Programming Operation (Notes 2,5)	Byte	Typ	54		us
		Word	Typ	54		us
tWHWH2	Sector Erase Operation (Note 2)		Typ	0.5		sec
tRH	RESET HIGH Time Before Write (Note 1)		Min	50		ns
tPOLL	Program Valid Before Status Polling (Note 6)		Max	4		us

Notes:
1. Not 100% tested.
2. See the "Erase And Programming Performance" section for more information.
3. For 1-16 words/1-32 bytes programmed.
4. Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.
5. Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.
6. When using the program suspend/resume feature, if the suspend command is issued within tPOLL, tPOLL must be fully re-applied upon resuming the programming operation. If the suspend command is issued after tPOLL, tPOLL is not required again prior to reading the status bits upon resuming.

Figure 13. CE# CONTROLLED PROGRAM TIMING WAVEFORM

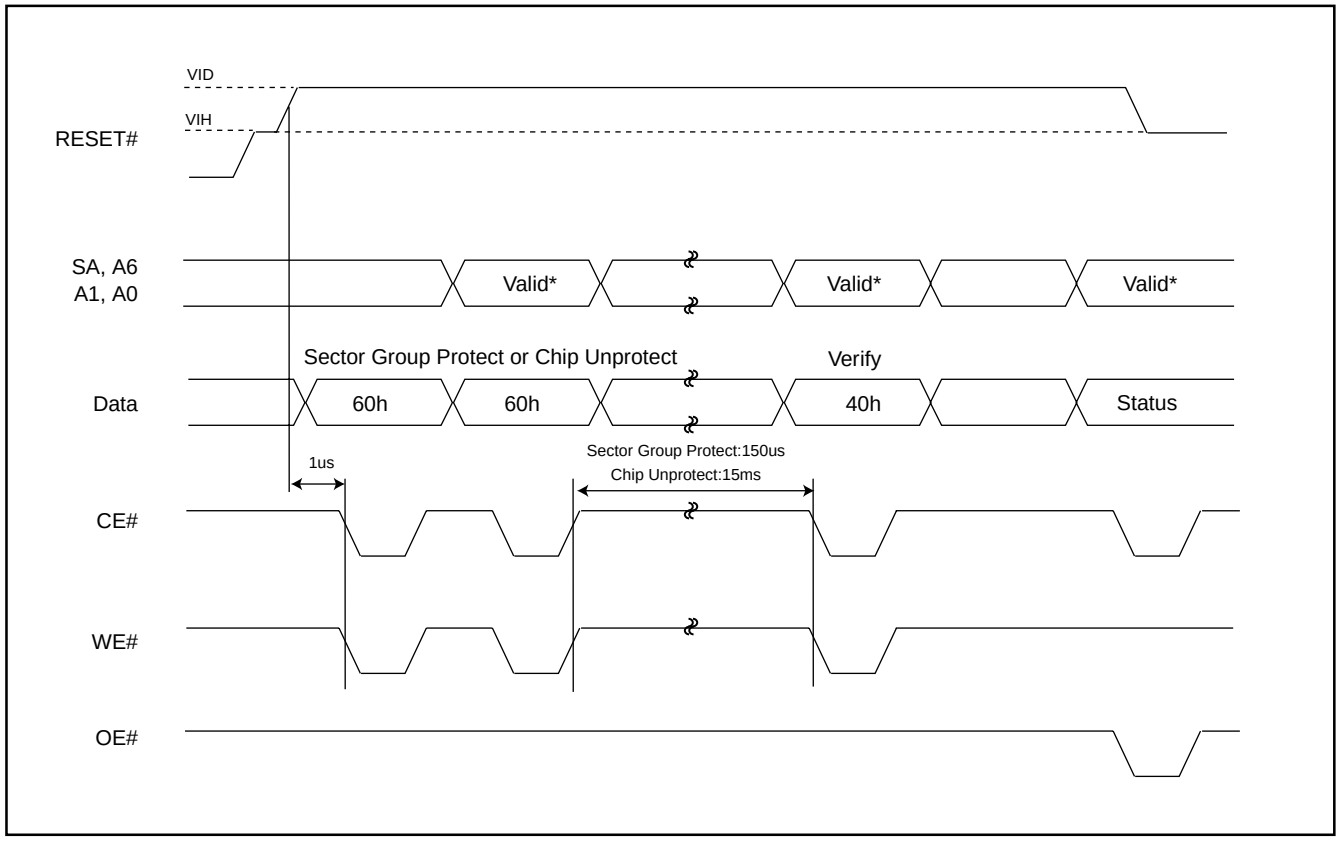


Notes :

1. PA=Program Address, PD=Program Data, DOUT=Data Out, Q7=complement of data written to device.
2. Figure indicates the last two bus cycles of the command sequence.

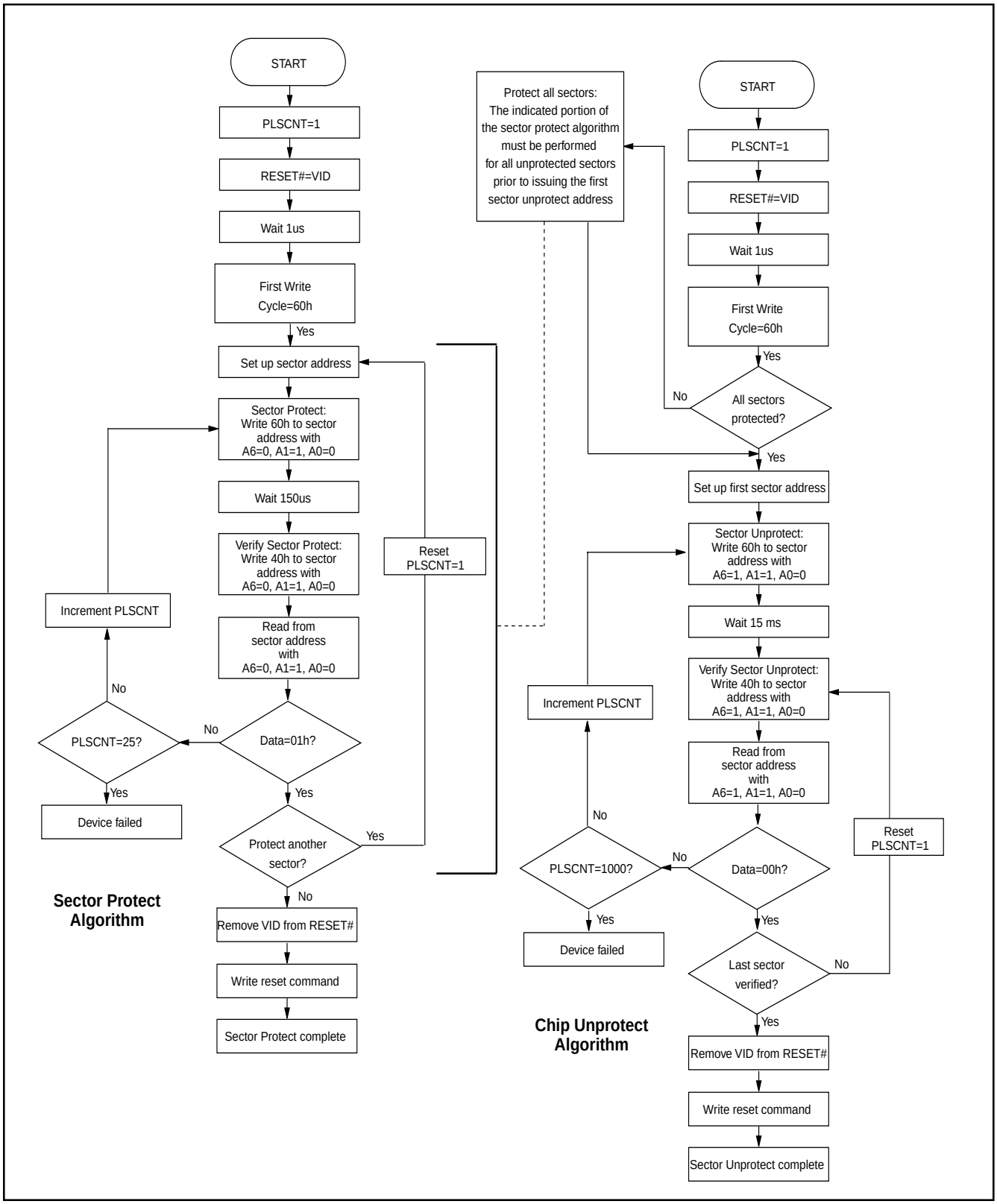
SECTOR GROUP PROTECT/CHIP UNPROTECT

Figure 14. Sector Group Protect / Chip Unprotect Waveform (RESET# Control)



Note: For sector group protect A6=0, A1=1, A0=0. For chip unprotect A6=1, A1=1, A0=0

Figure 15. IN-SYSTEM SECTOR GROUP PROTECT/CHIP UNPROTECT ALGORITHMS WITH RESET#=VID



AC CHARACTERISTICS

Parameter	Description	Test Setup	All Speed Options	Unit
tVLHT	Voltage transition time	Min.	4	us
tWPP1	Write pulse width for sector group protect	Min.	100	ns
tOESP	OE# setup time to WE# active	Min.	4	us

Figure 16. SECTOR GROUP PROTECT TIMING WAVEFORM (A9, OE# Control)

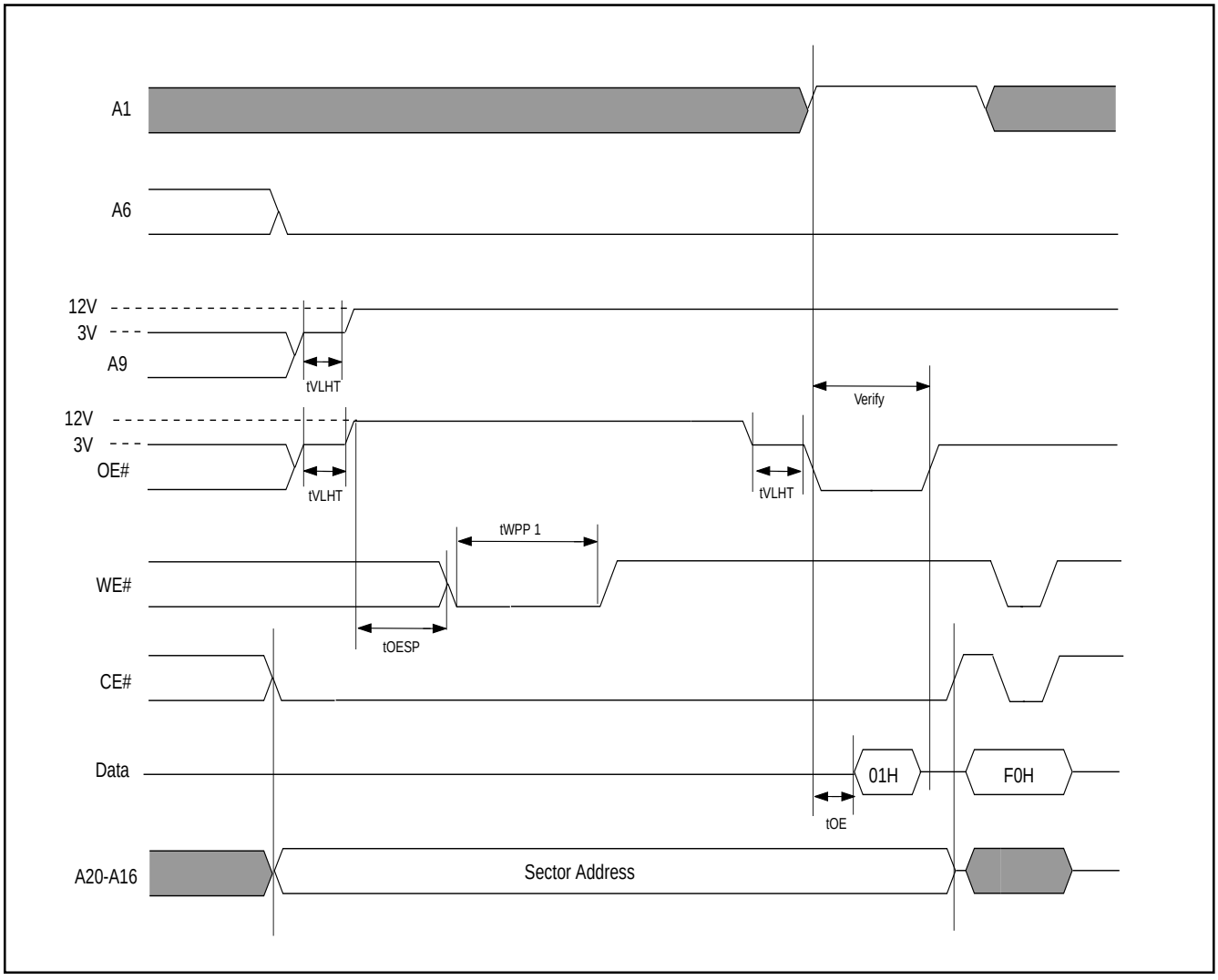


Figure 17. SECTOR GROUP PROTECTION ALGORITHM (A9, OE# Control)

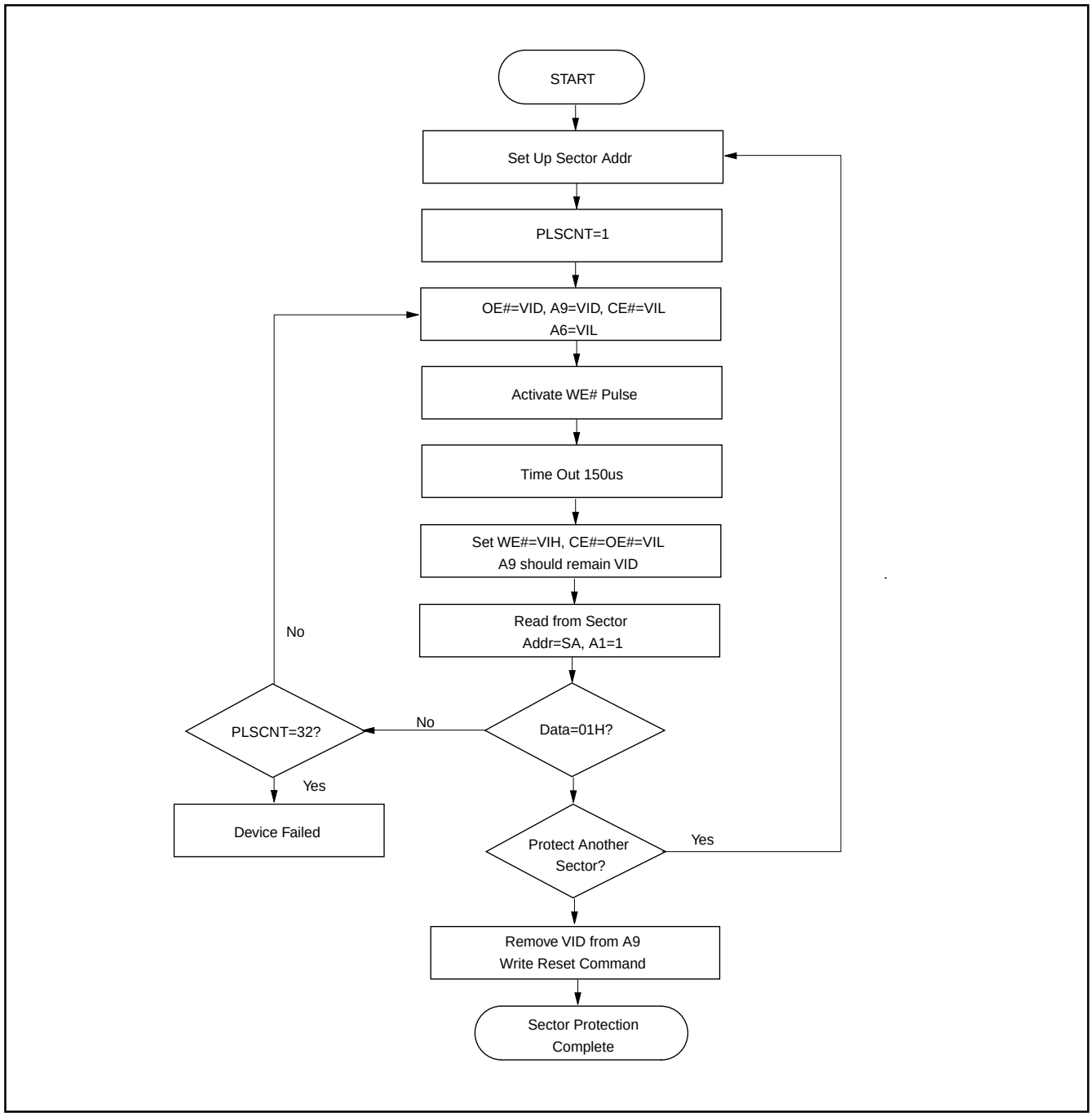


Figure 18. CHIP UNPROTECT TIMING WAVEFORM (A9, OE# Control)

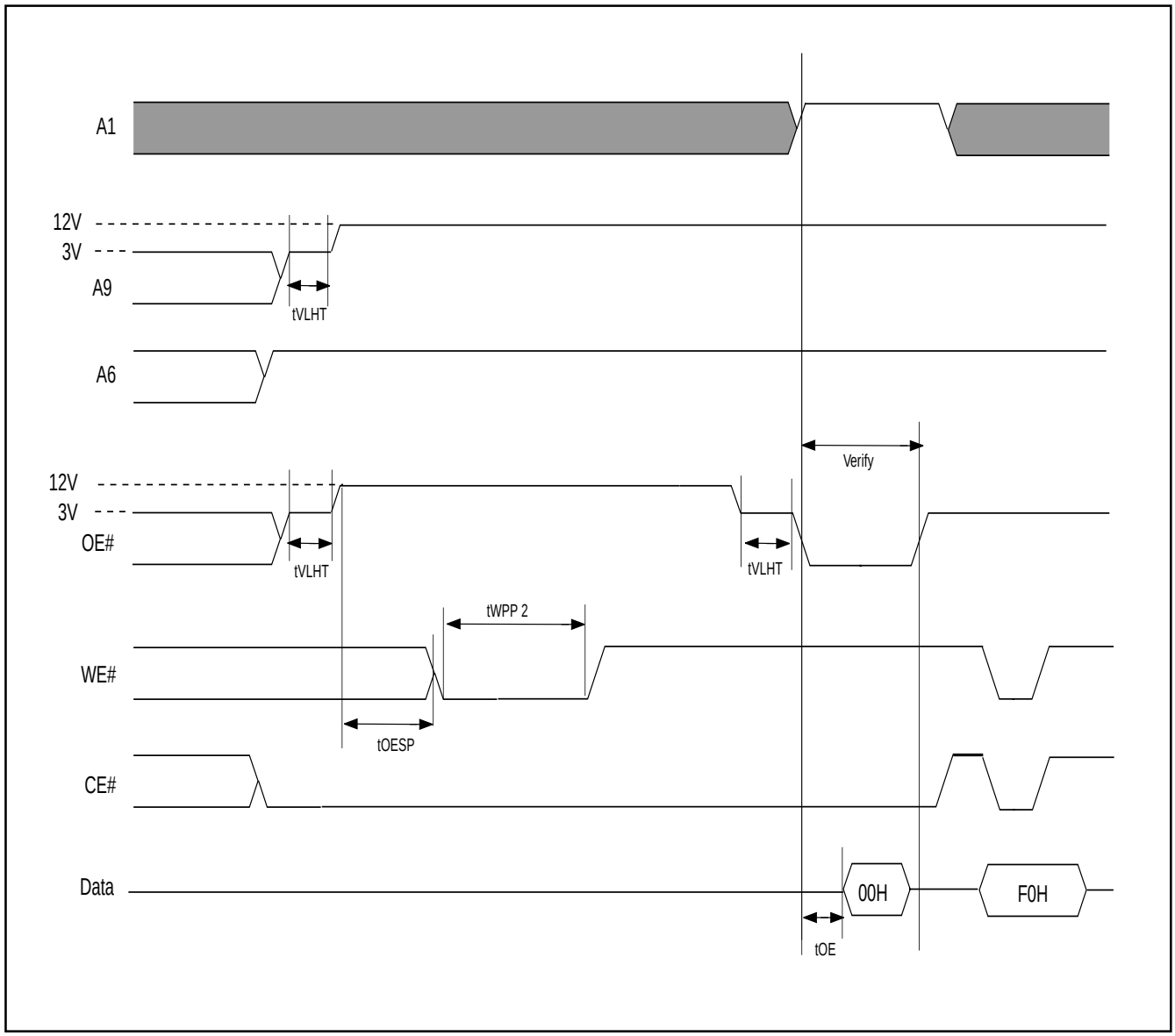
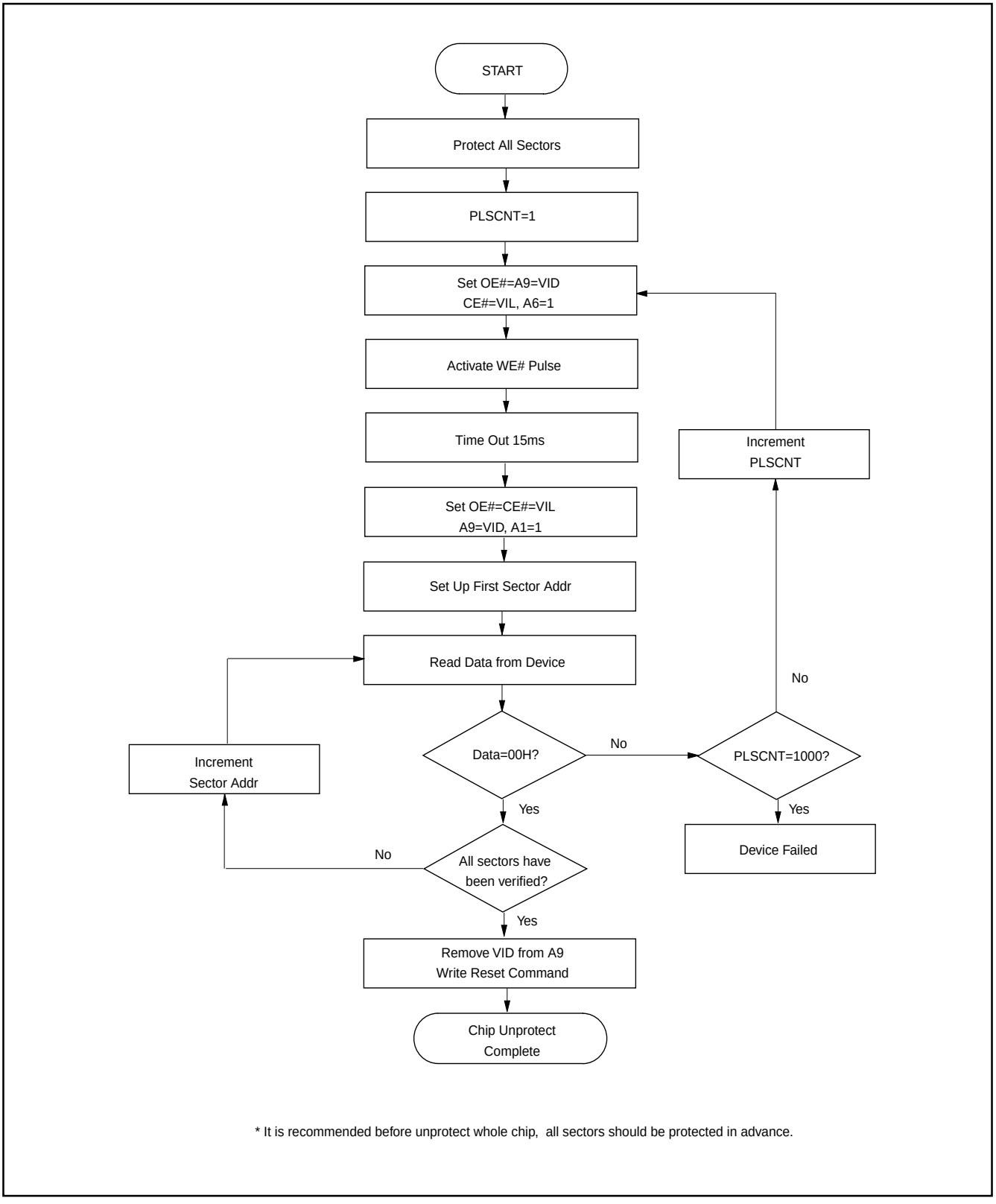


Figure 19. CHIP UNPROTECT FLOWCHART (A9, OE# Control)



* It is recommended before unprotect whole chip, all sectors should be protected in advance.

Figure 20. SECURED SILICON SECTOR PROTECTED ALGORITHMS FLOWCHART

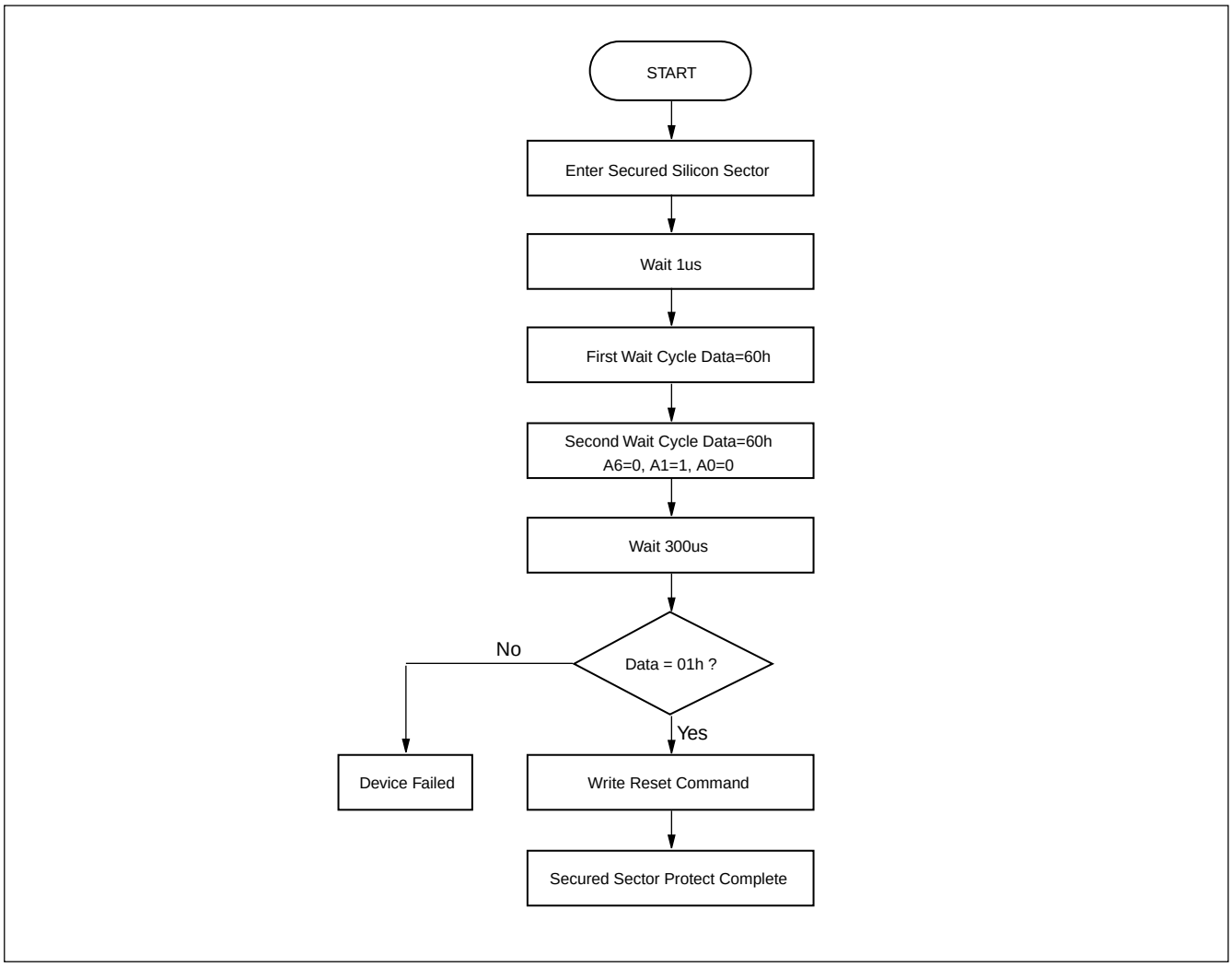
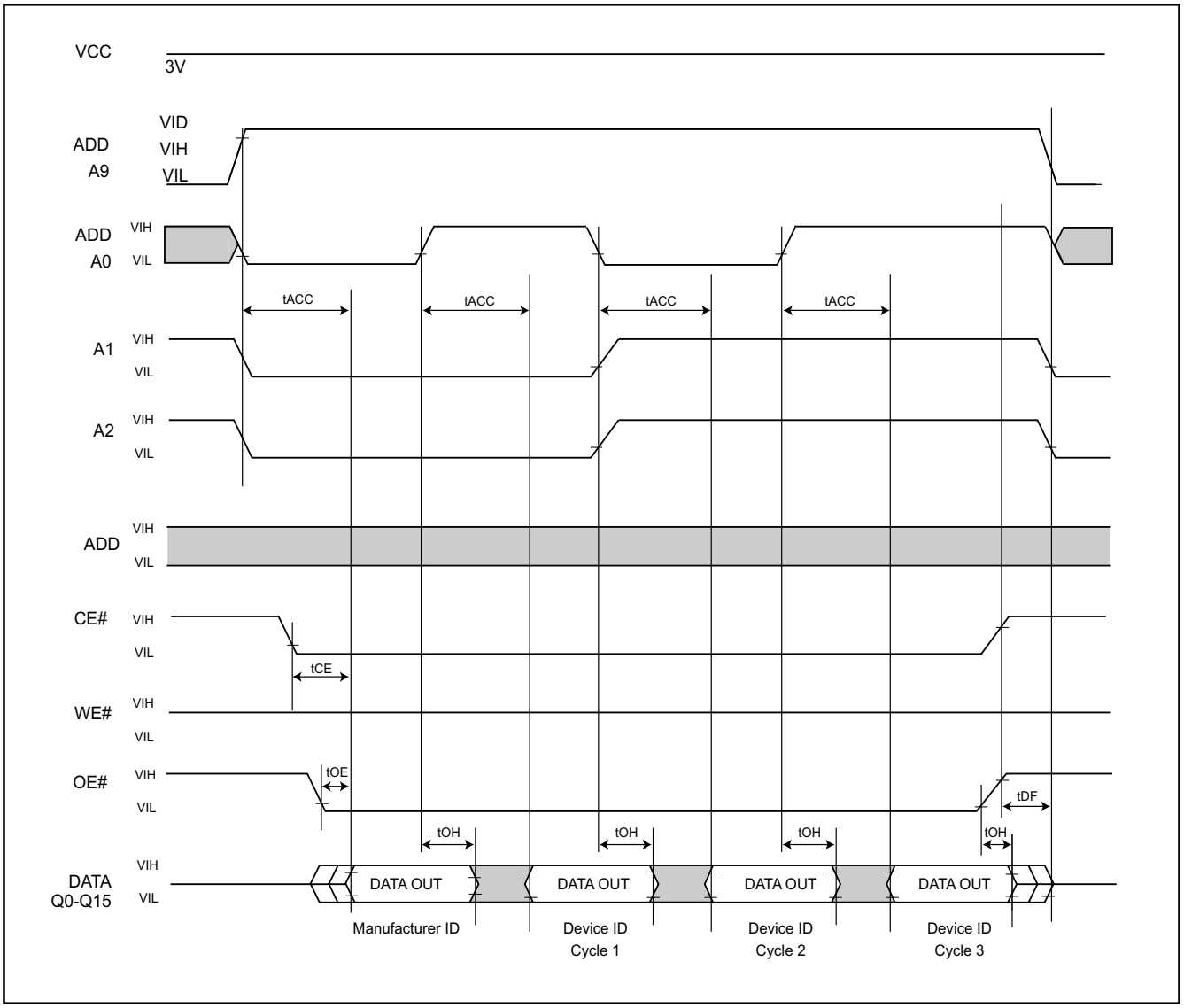
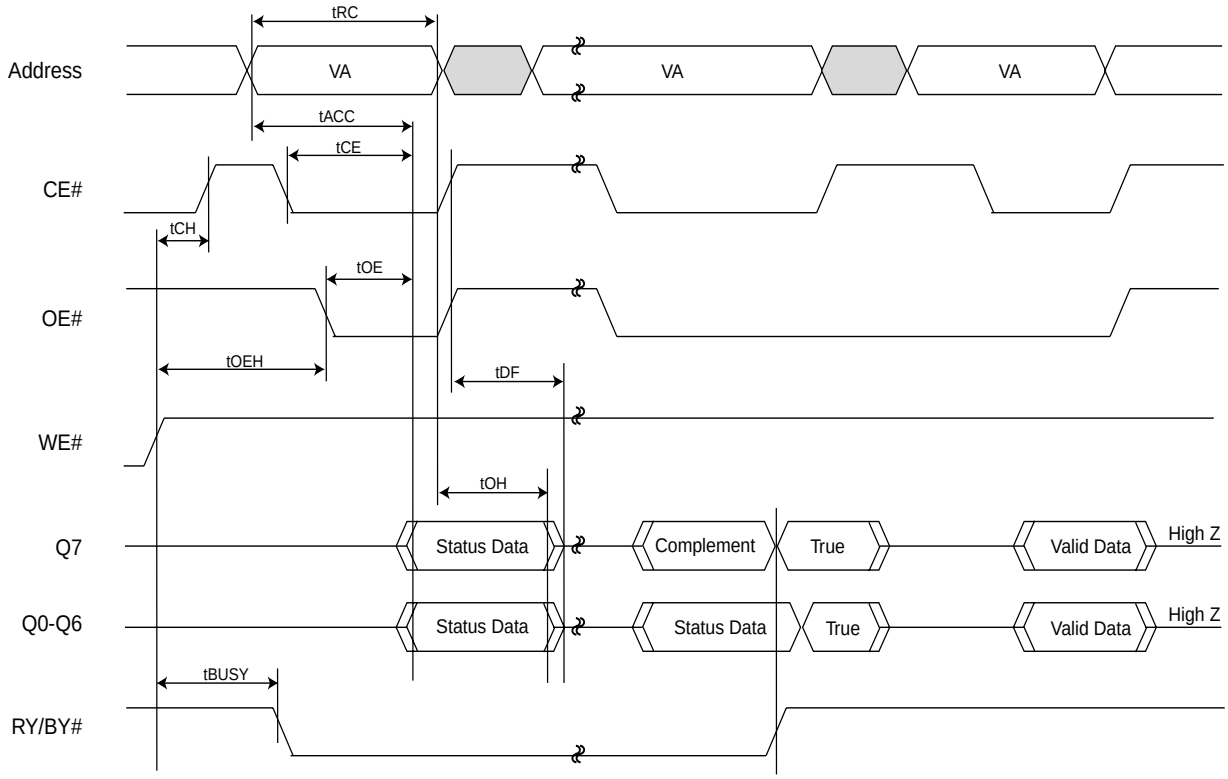


Figure 21. SILICON ID READ TIMING WAVEFORM



WRITE OPERATION STATUS

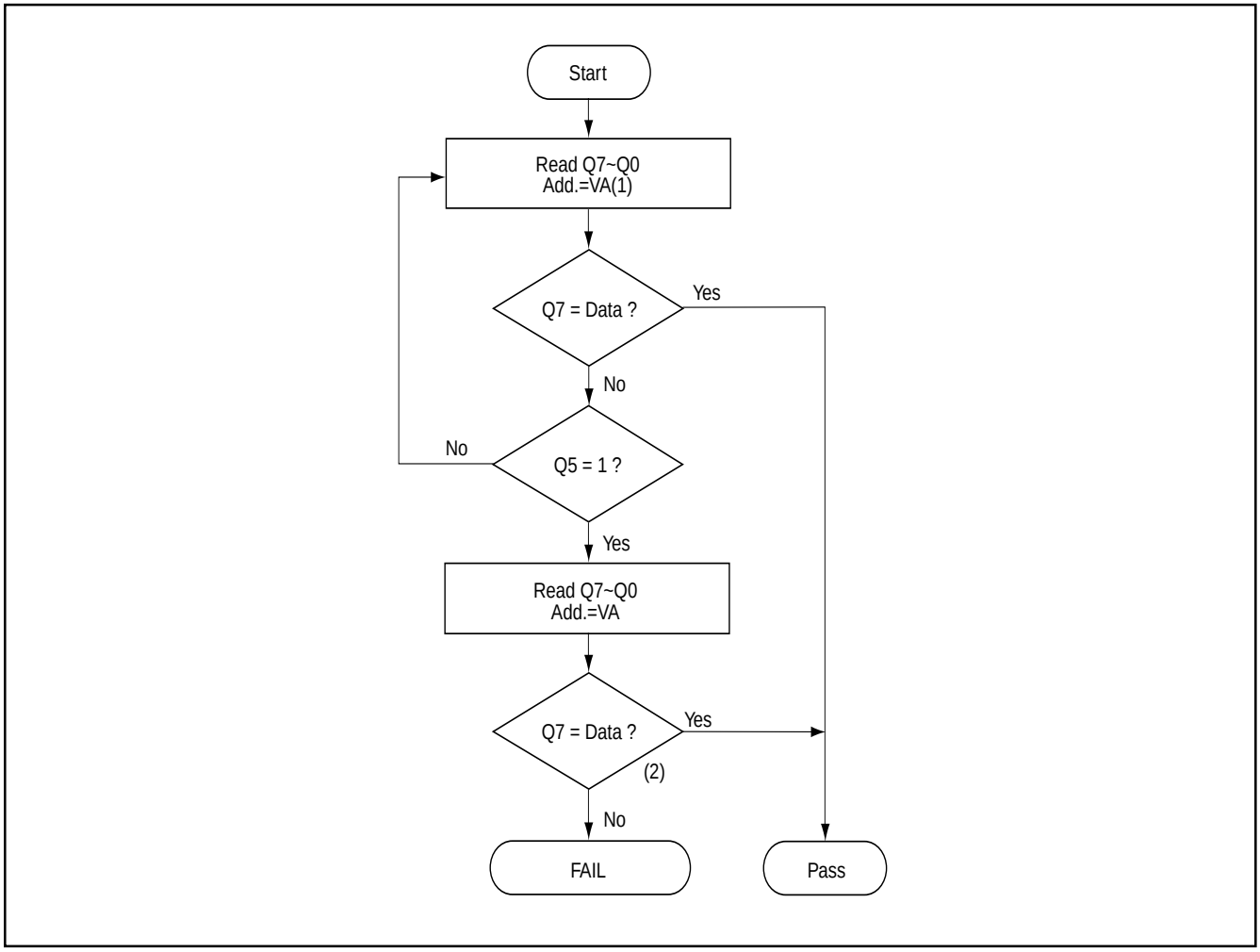
Figure 22. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)



Note :

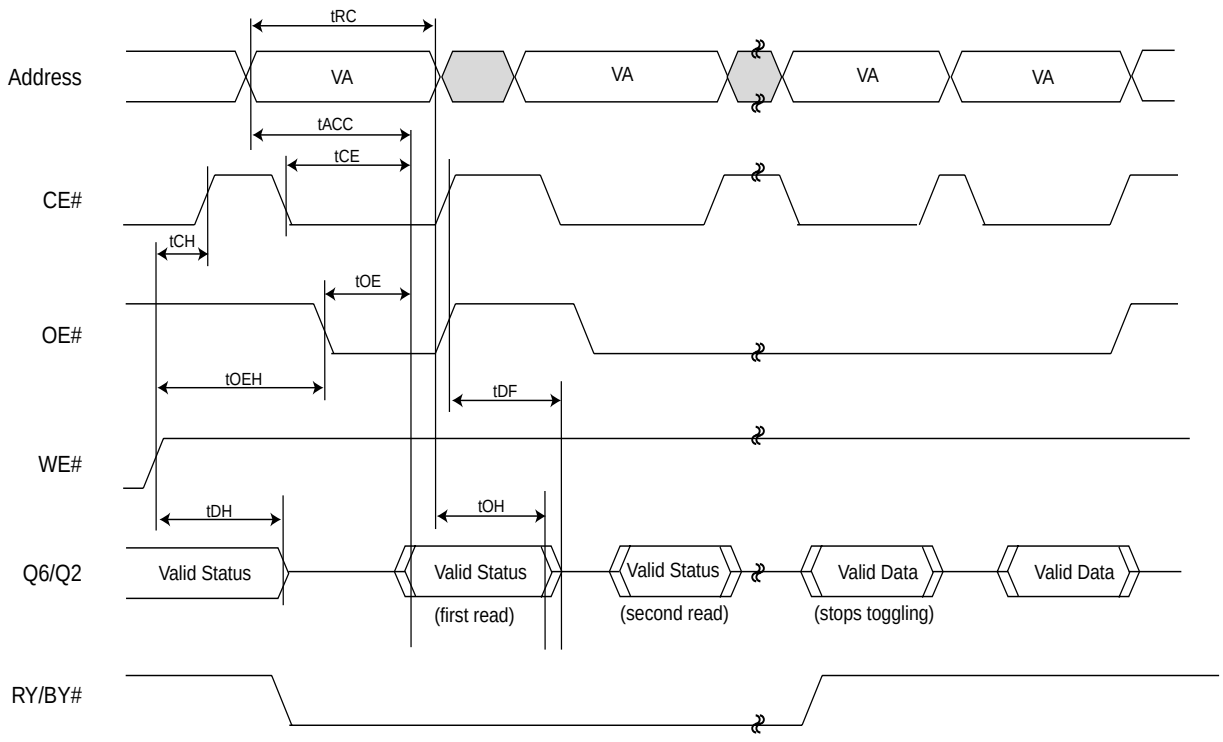
VA=Valid address. Figure shows are first status cycle after command sequence, last status read cycle, and array data raed cycle.

Figure 23. DATA# POLLING ALGORITHM



Notes :
1.VA=valid address for programming.
2.Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

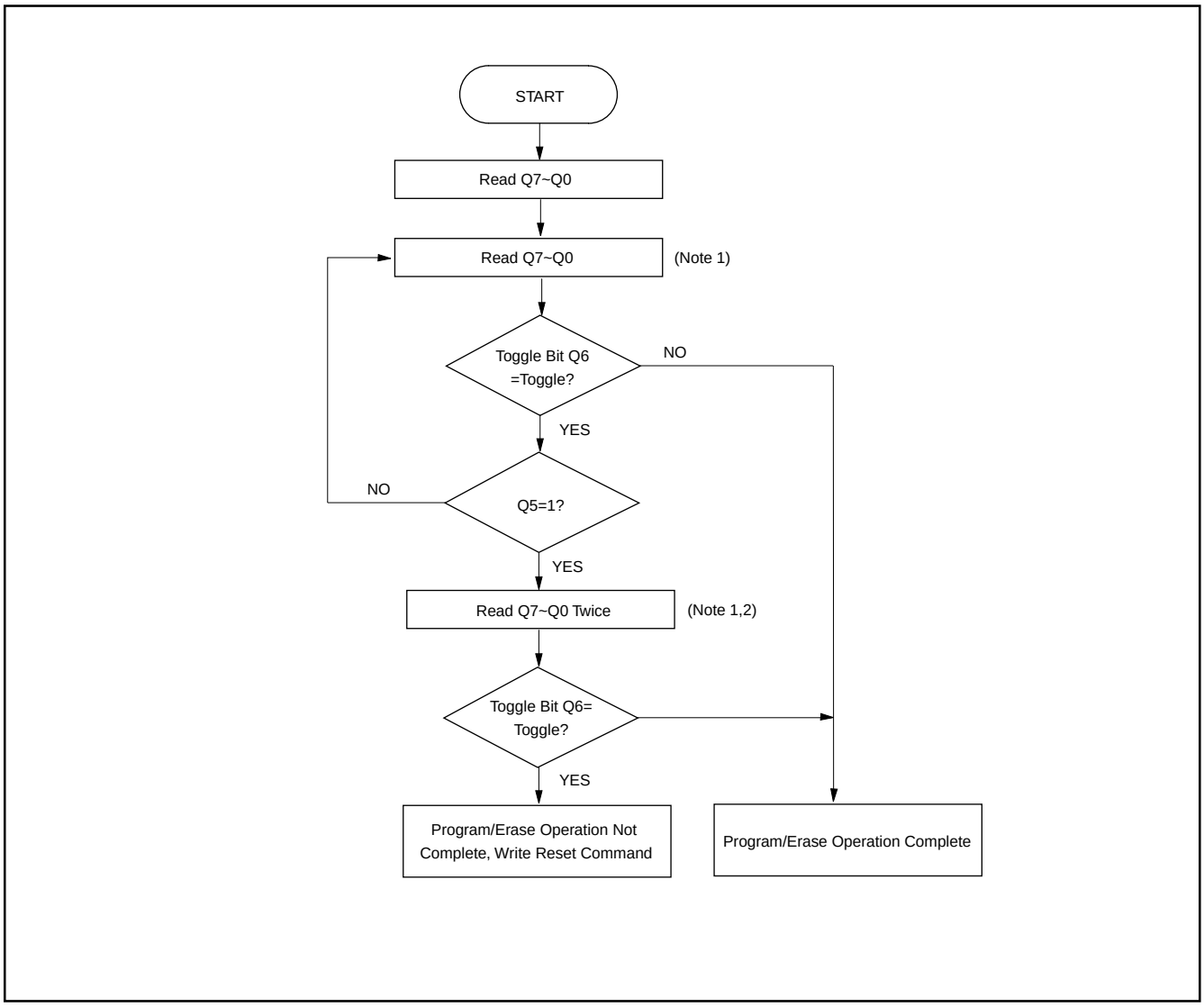
Figure 24. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)



Note :

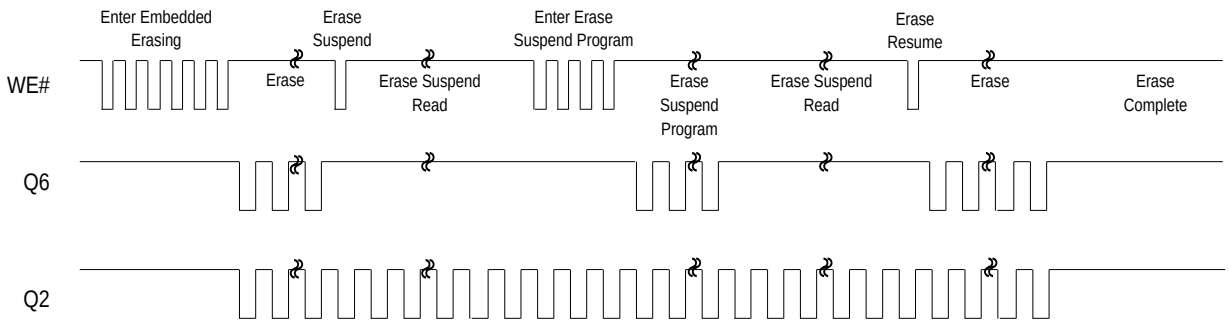
VA=Valid address; not required for Q6. Figure shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 25. TOGGLE BIT ALGORITHM



Notes :
1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

Figure 26. Q6 versus Q2



Note :

The system can use OE# or CE# to toggle Q2/Q6, Q2 toggles only when read at an address within an erase-suspended

RECOMMENDED OPERATING CONDITIONS

At Device Power-Up

AC timing illustrated in Figure A is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

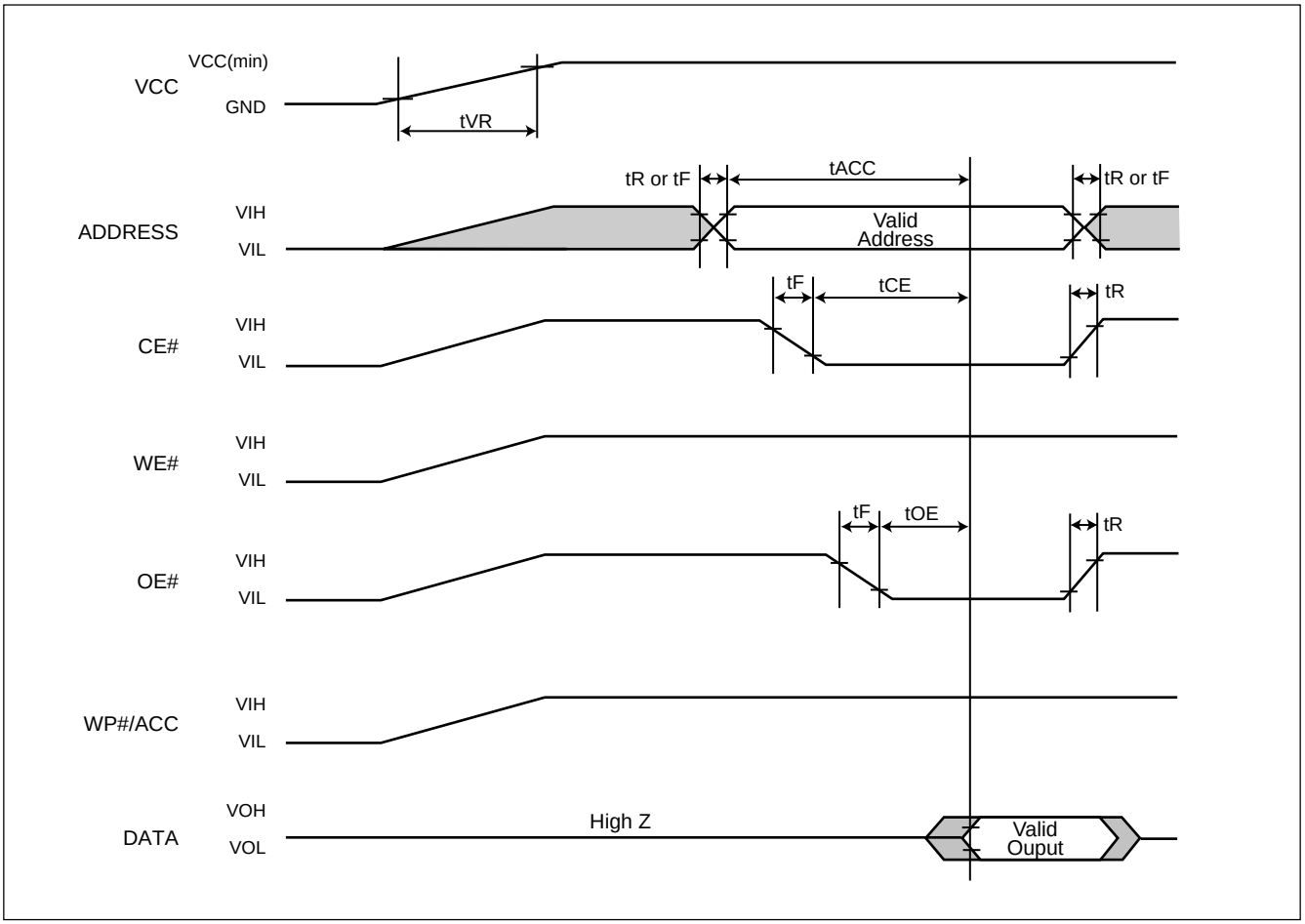


Figure A. AC Timing at Device Power-Up

Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V
tR	Input Signal Rise Time	1,2		20	us/V
tF	Input Signal Fall Time	1,2		20	us/V

Notes :
1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

ERASE AND PROGRAMMING PERFORMANCE (1)

PARAMETER	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	0.5	3.5	sec	Excludes 00h programming prior to erasure Note 6
Chip Erase Time	32		sec	
Total Write Buffer Program Time (Note 4)	240		us	Excludes system level overhead Note 7
Total Accelerated Effective Write Buffer Program Time (Note 4)	200		us	
Chip Program Time	31.5		sec	

Notes:
1. Typical program and erase times assume the following conditions: 25° C, 3.0 V VCC. Programming specifications assume that all bits are programmed to 00h.
2. Maximum values are measured at VCC = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
3. Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.
4. For 1-16 words or 1-32 bytes programmed in a single write buffer programming operation.
5. Effective write buffer specification is calculated on a per-word/per-byte basis for a 16-word/32-byte write buffer operation.
6. In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.
7. System-level overhead is the time required to execute the command sequence(s) for the program command. See Tables 3 for further information on command definitions.
8. The device has a minimum erase and program cycle endurance of 100,000 cycles.

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

DATA RETENTION

Parameter	Min	Unit
Minimum Pattern Data Retention Time	20	Years

TSOP PIN AND CSP PACKAGE CAPACITANCE

Parameter Symbol	Parameter Description	Test Set		TYP	MAX	UNIT
CIN	Input Capacitance	VIN=0	TSOP	6	7.5	pF
			CSP	4.2	5.0	pF
COUT	Output Capacitance	VOUT=0	TSOP	8.5	12	pF
			CSP	5.4	6.5	pF
CIN2	Control Pin Capacitance	VIN=0	TSOP	7.5	9	pF
			CSP	3.9	4.7	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions TA=25° C, f=1.0MHz

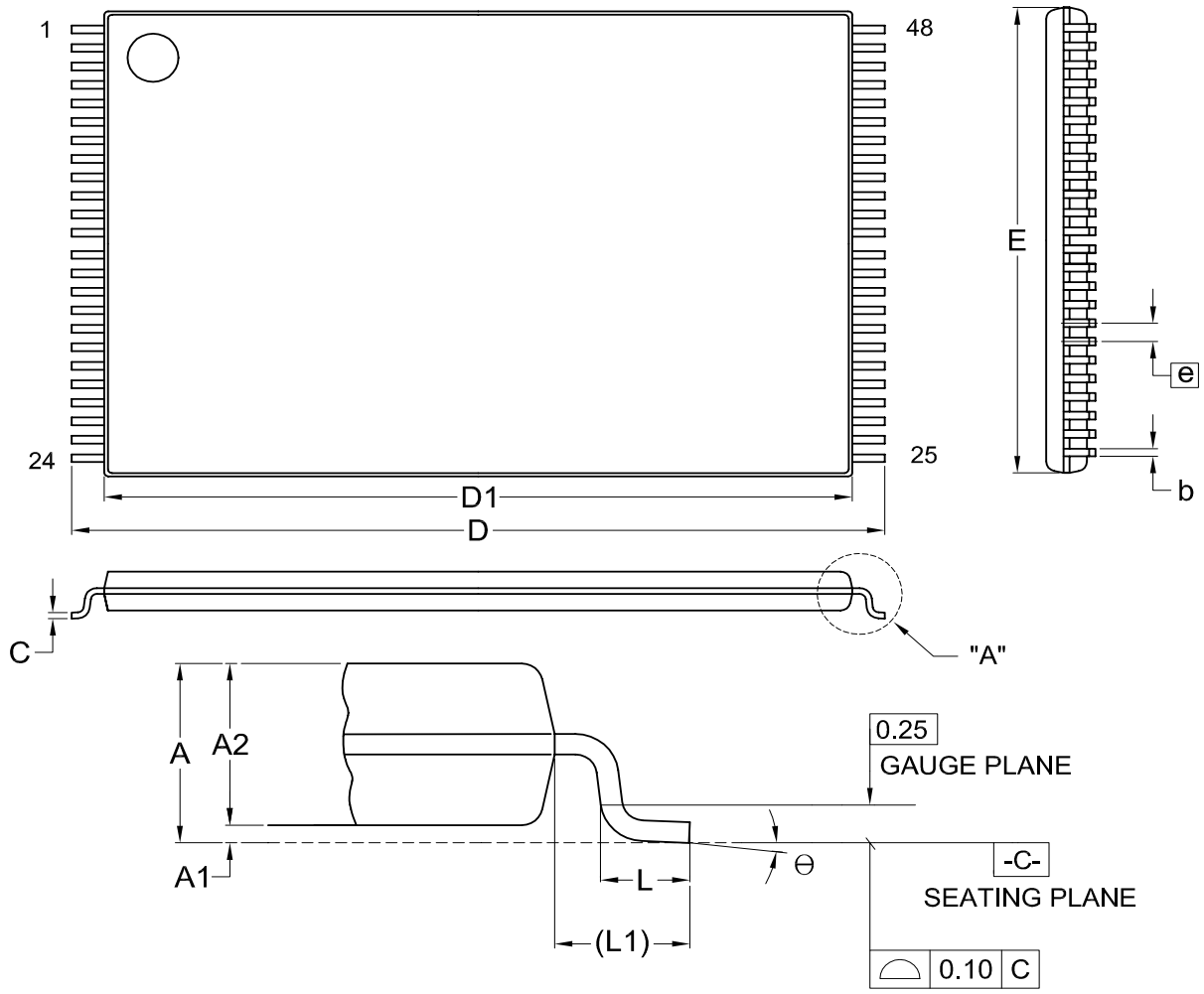
ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	Ball Pitch/ Ball size	PACKAGE	Remark
MX29LA320MTTC-70R	70		48 Pin TSOP (Normal Type)	
MX29LA320MTTC-90	90		48 Pin TSOP (Normal Type)	
MX29LA320MBTC-70R	70		48 Pin TSOP (Normal Type)	
MX29LA320MBTC-90	90		48 Pin TSOP (Normal Type)	
MX29LA320MTTI-90	90		48 Pin TSOP (Normal Type)	
MX29LA320MBTI-90	90		48 Pin TSOP (Normal Type)	
MX29LA320MTXBC-70R	70	0.8mm/0.3mm	48 Ball CSP	
MX29LA320MTXBC-90	90	0.8mm/0.3mm	48 Ball CSP	
MX29LA320MBXBC-70R	70	0.8mm/0.3mm	48 Ball CSP	
MX29LA320MBXBC-90	90	0.8mm/0.3mm	48 Ball CSP	
MX29LA320MTXBI-90	90	0.8mm/0.3mm	48 Ball CSP	
MX29LA320MBXBI-90	90	0.8mm/0.3mm	48 Ball CSP	
MX29LA320MTXEC-70R	70	0.8mm/0.4mm	48 Ball CSP	
MX29LA320MTXEC-90	90	0.8mm/0.4mm	48 Ball CSP	
MX29LA320MBXEC-70R	70	0.8mm/0.4mm	48 Ball CSP	
MX29LA320MBXEC-90	90	0.8mm/0.4mm	48 Ball CSP	
MX29LA320MTXEI-90	90	0.8mm/0.4mm	48 Ball CSP	
MX29LA320MBXEI-90	90	0.8mm/0.4mm	48 Ball CSP	
MX29LA320MTTC-90G	90		48 Pin TSOP (Normal Type)	PB-free
MX29LA320MBTC-90G	90		48 Pin TSOP (Normal Type)	PB-free
MX29LA320MTTI-90G	90		48 Pin TSOP (Normal Type)	PB-free
MX29LA320MBTI-90G	90		48 Pin TSOP (Normal Type)	PB-free
MX29LA320MTXBC-90G	90	0.8mm/0.3mm	48 Ball CSP	PB-free
MX29LA320MBXBC-90G	90	0.8mm/0.3mm	48 Ball CSP	PB-free
MX29LA320MTXBI-90G	90	0.8mm/0.3mm	48 Ball CSP	PB-free
MX29LA320MBXBI-90G	90	0.8mm/0.3mm	48 Ball CSP	PB-free
MX29LA320MTXEC-90G	90	0.8mm/0.4mm	48 Ball CSP	PB-free
MX29LA320MBXEC-90G	90	0.8mm/0.4mm	48 Ball CSP	PB-free
MX29LA320MTXEI-90G	90	0.8mm/0.4mm	48 Ball CSP	PB-free
MX29LA320MBXEI-90G	90	0.8mm/0.4mm	48 Ball CSP	PB-free

PART NO.	ACCESS TIME (ns)	Ball Pitch/ Ball size	PACKAGE	Remark
MX29LA321MTTC-70R	70		56 Pin TSOP (Normal Type)	
MX29LA321MTTC-90	90		56 Pin TSOP (Normal Type)	
MX29LA321MBTC-70R	70		56 Pin TSOP (Normal Type)	
MX29LA321MBTC-90	90		56 Pin TSOP (Normal Type)	
MX29LA321MTTI-90	90		56 Pin TSOP (Normal Type)	
MX29LA321MBTI-90	90		56 Pin TSOP (Normal Type)	
MX29LA321MTXCC-70R	70	1.0mm/0.4mm	64 Ball CSP	
MX29LA321MTXCC-90	90	1.0mm/0.4mm	64 Ball CSP	
MX29LA321MBXCC-70R	70	1.0mm/0.4mm	64 Ball CSP	
MX29LA321MBXCC-90	90	1.0mm/0.4mm	64 Ball CSP	
MX29LA321MTXCI-90	90	1.0mm/0.4mm	64 Ball CSP	
MX29LA321MBXCI-90	90	1.0mm/0.4mm	64 Ball CSP	
MX29LA321MTTC-90G	90		56 Pin TSOP (Normal Type)	PB-free
MX29LA321MBTC-90G	90		56 Pin TSOP (Normal Type)	PB-free
MX29LA321MTTI-90G	90		56 Pin TSOP (Normal Type)	PB-free
MX29LA321MBTI-90G	90		56 Pin TSOP (Normal Type)	PB-free
MX29LA321MTXCC-90G	90	1.0mm/0.4mm	64 Ball CSP	PB-free
MX29LA321MBXCC-90G	90	1.0mm/0.4mm	64 Ball CSP	PB-free
MX29LA321MTXCI-90G	90	1.0mm/0.4mm	64 Ball CSP	PB-free
MX29LA321MBXCI-90G	90	1.0mm/0.4mm	64 Ball CSP	PB-free

PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM



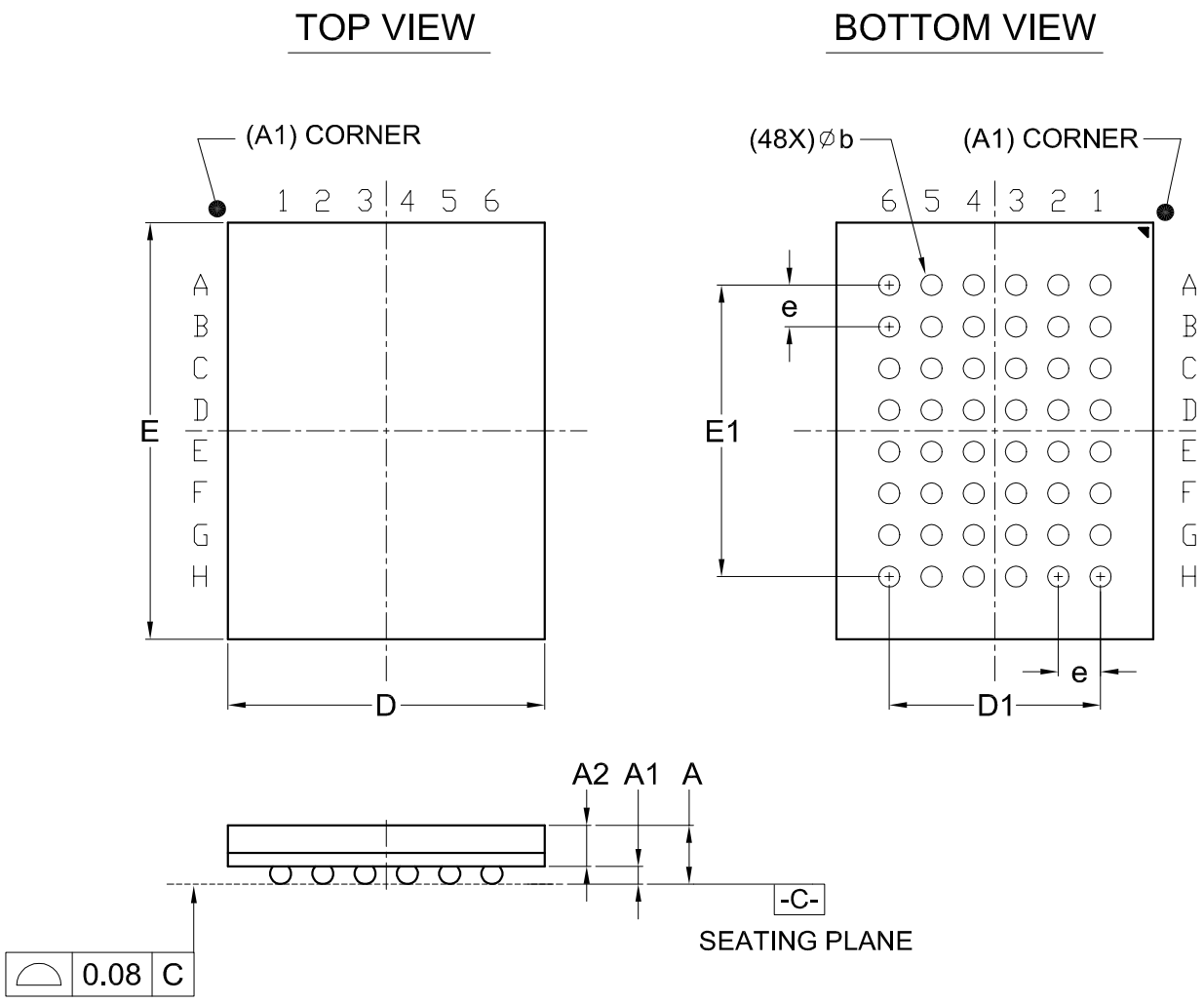
DETAIL"A"

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	7	MO-142			12-01-'03

Title: **Package Outline for CSP 48BALL(6X8X1.2MM,BALL PITCH 0.8MM,BALL DIAMETER 0.3MM)**



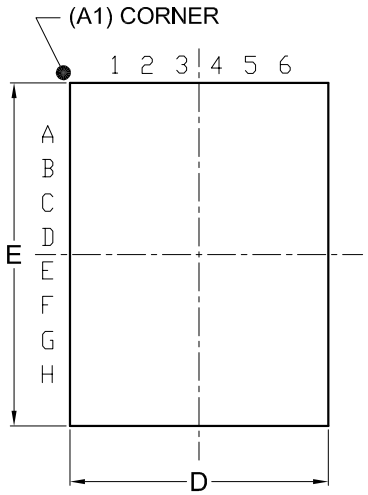
Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.18	0.65	0.27	5.90		7.90		
	Nom.	---	0.23	---	0.30	6.00	4.00	8.00	5.60	0.80
	Max.	1.20	0.28	---	0.37	6.10		8.10		
Inch	Min.	---	0.007	0.026	0.011	0.232		0.311		
	Nom.	---	0.009	---	0.012	0.236	0.157	0.315	0.220	0.031
	Max.	0.047	0.011	---	0.015	0.240		0.319		

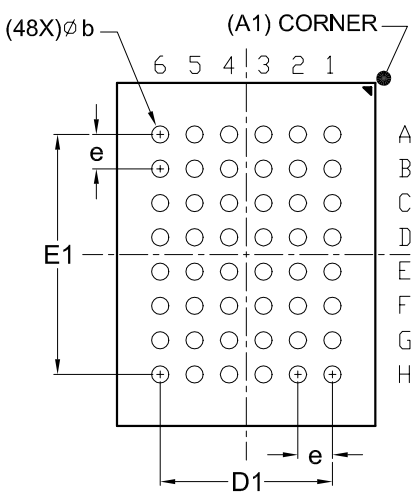
DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4201	4	MO-210			12-12-'03

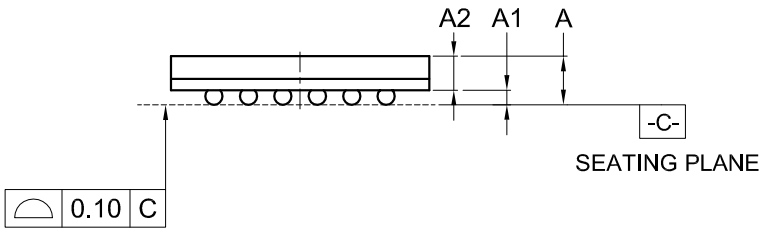
Title: **Package Outline for CSP 48BALL(6X8X1.3MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)**

TOP VIEW



BOTTOM VIEW



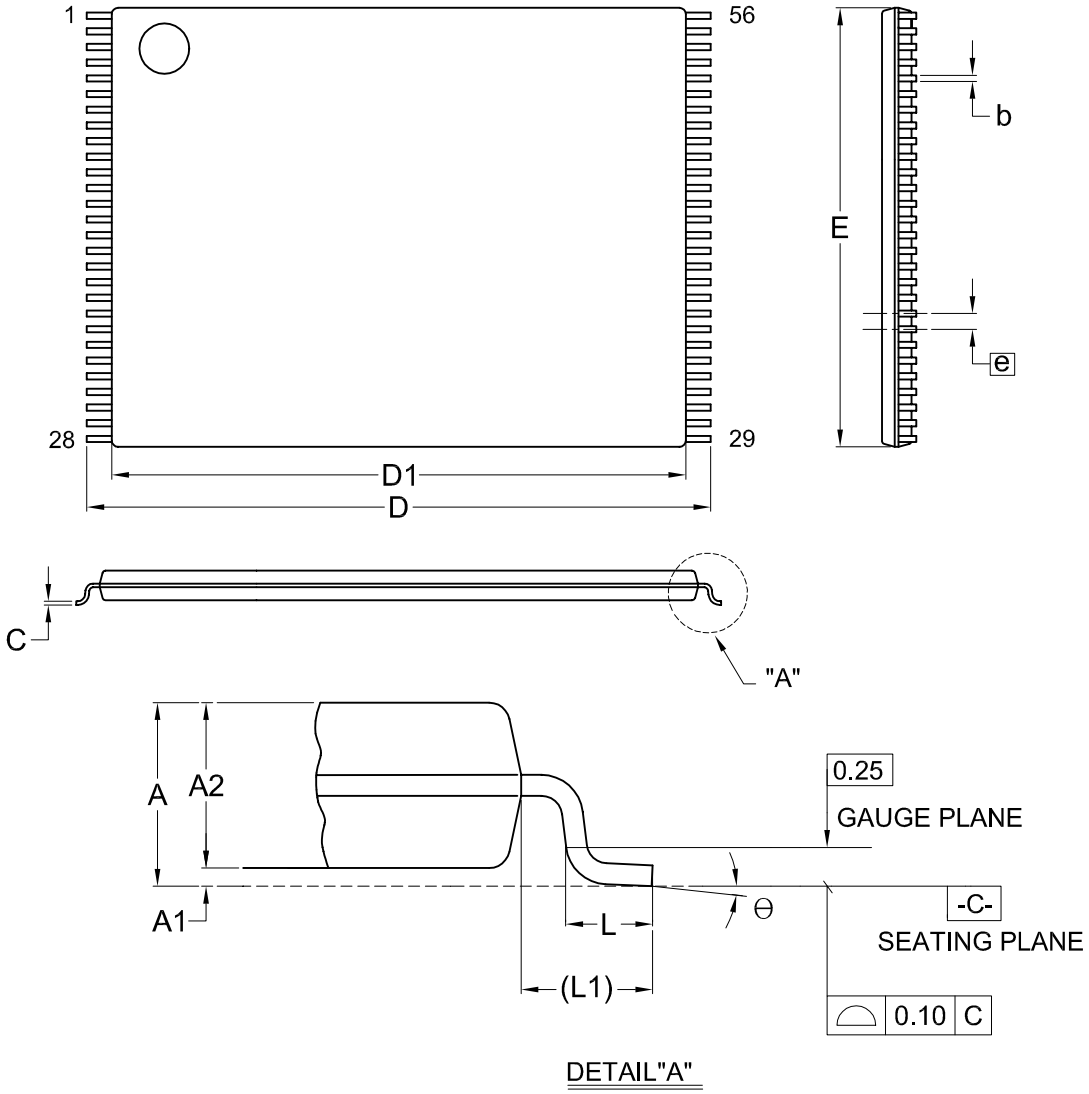


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	5.90		7.90		
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	5.60	0.80
	Max.	1.30	0.35	---	0.45	6.10		8.10		
Inch	Min.	—	0.010	0.026	0.014	0.232		0.311		
	Nom.	—	0.012	---	0.016	0.236	0.157	0.315	0.220	0.031
	Max.	0.051	0.014	---	0.018	0.240		0.319		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4202	4	MO-219			12-12-'03

Title: Package Outline for TSOP(I) 56L (14X20mm)

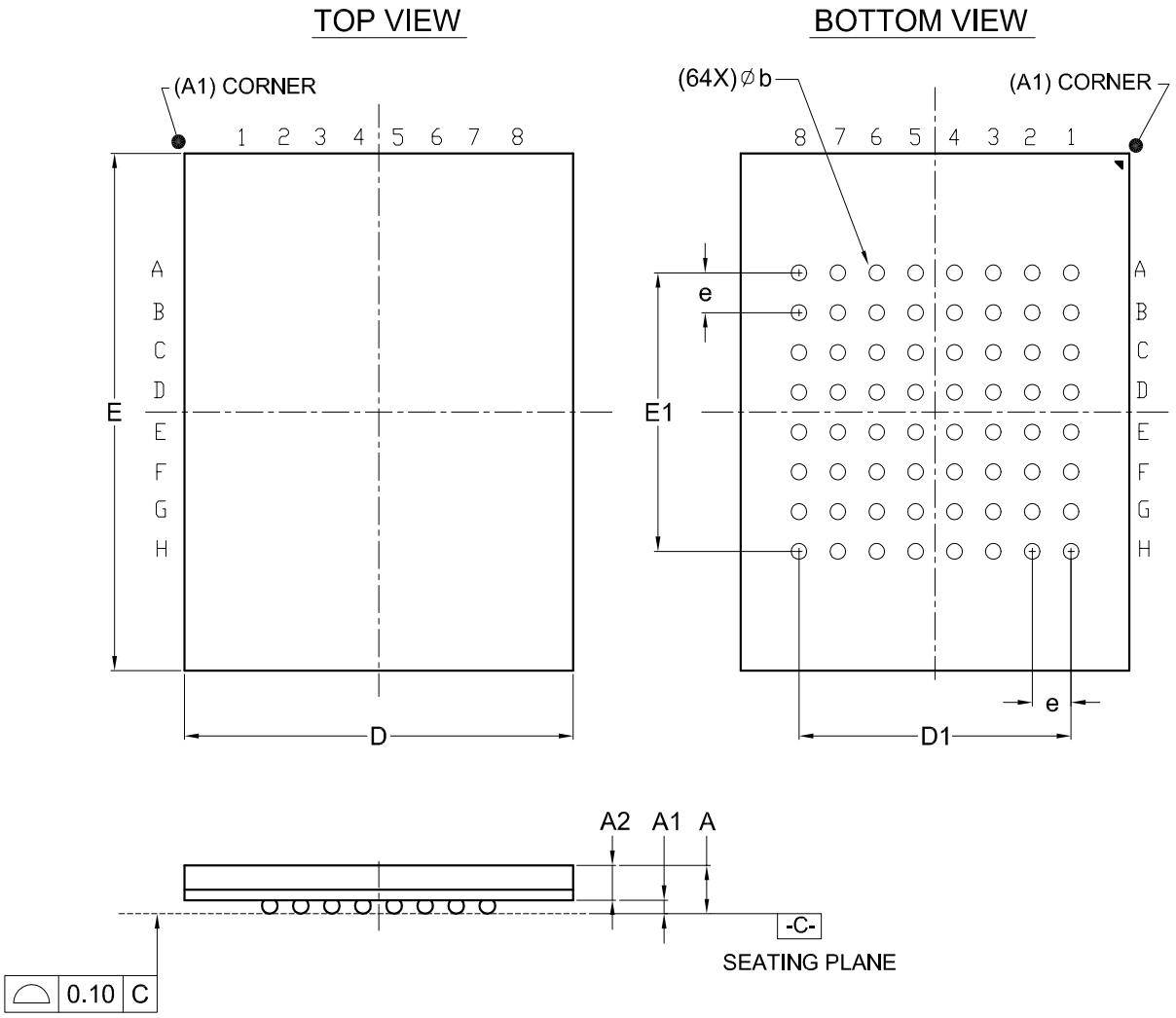


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	13.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	14.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	14.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.547		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.551	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.555		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1608	4	MO-142			12-01-'03

Title: **Package Outline for CSP 64BALL(10X13X1.2MM,BALL PITCH 1.00MM,BALL DIAMETER 0.4MM)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	9.90		12.90		
	Nom.	---	0.30	---	0.40	10.00	7.00	13.00	7.00	1.00
	Max.	1.20	0.35	---	0.45	10.10		13.10		
Inch	Min.	---	0.010	0.026	0.014	0.390		0.508		
	Nom.	---	0.012	---	0.016	0.394	0.276	0.512	0.276	0.039
	Max.	0.047	0.014	---	0.018	0.398		0.516		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4220	3	MO-216			12-15-'03

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Advanced Information" on title	P1	MAR/22/2005
1.1	1. To modify WP# protect function	P1,11,15	JUN/10/2005
1.2	1. To add note 7 for ILIT parameter in DC Characteristics table	P32	JUL/11/2005
	2. To add comments into performance table	P63	
1.3	1. To add "Chip Enable Truth" table for MX29LA321 option	P5	NOV/15/2005
	2. Removed "Temporary Sector Group Unprotect" function	All	

MACRONIX INTERNATIONAL CO., LTD.

Headquarters:
TEL:+886-3-578-6688
FAX:+886-3-563-2888

Europe Office :
TEL:+32-2-456-8020
FAX:+32-2-456-8021

Hong Kong Office :
TEL:+86-755-834-335-79
FAX:+86-755-834-380-78

Japan Office :
Kawasaki Office :
TEL:+81-44-246-9100
FAX:+81-44-246-9105
Osaka Office :
TEL:+81-6-4807-5460
FAX:+81-6-4807-5461

Singapore Office :
TEL:+65-6346-5505
FAX:+65-6348-8096

Taipei Office :
TEL:+886-2-2509-3300
FAX:+886-2-2509-2200

MACRONIX AMERICA, INC.
TEL:+1-408-262-8887
FAX:+1-408-262-8810

http : //www.macronix.com