**PRELIMINARY**

# 160-common x 132-segment DOT MATRIX LCD DRIVER FOR 4 GRAY SCALE

## ■GENERAL DESCRIPTION

The NJU6682 is a bit map LCD driver to display graphics or characters. It contains 84,480 bits display data RAM, microprocessor interface circuits, instruction decoder, and 160-common and 132-segment drivers.

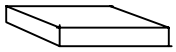
The bit image data is transferred to the internal display data RAM by serial interface or 8-bit/16-bit parallel interface.

The NJU6682 features 4-gray scale function which creates 4 types gray scale (for example : white/light gray/dark gray/black) or black & white with displays 160 x 132 dots graphics or 8-caracter 10line by 16 x 16 dots characters.

It oscillates by built-in OSC circuit without any external components. Furthermore, the NJU6682 features Partial Display Function which creates up to 2 blocks of active display area and optimizes duty cycle ratio. This function sets optimum boosted voltage by the combination with both of programmable voltage booster circuit and electrical variable resister. As result, it reduces the operating current.

The operating voltage from 2.4V to 3.3V and low operating current are useful for small size battery operating items.

## ■PACKAGE OUTLINE



NJU6682CH

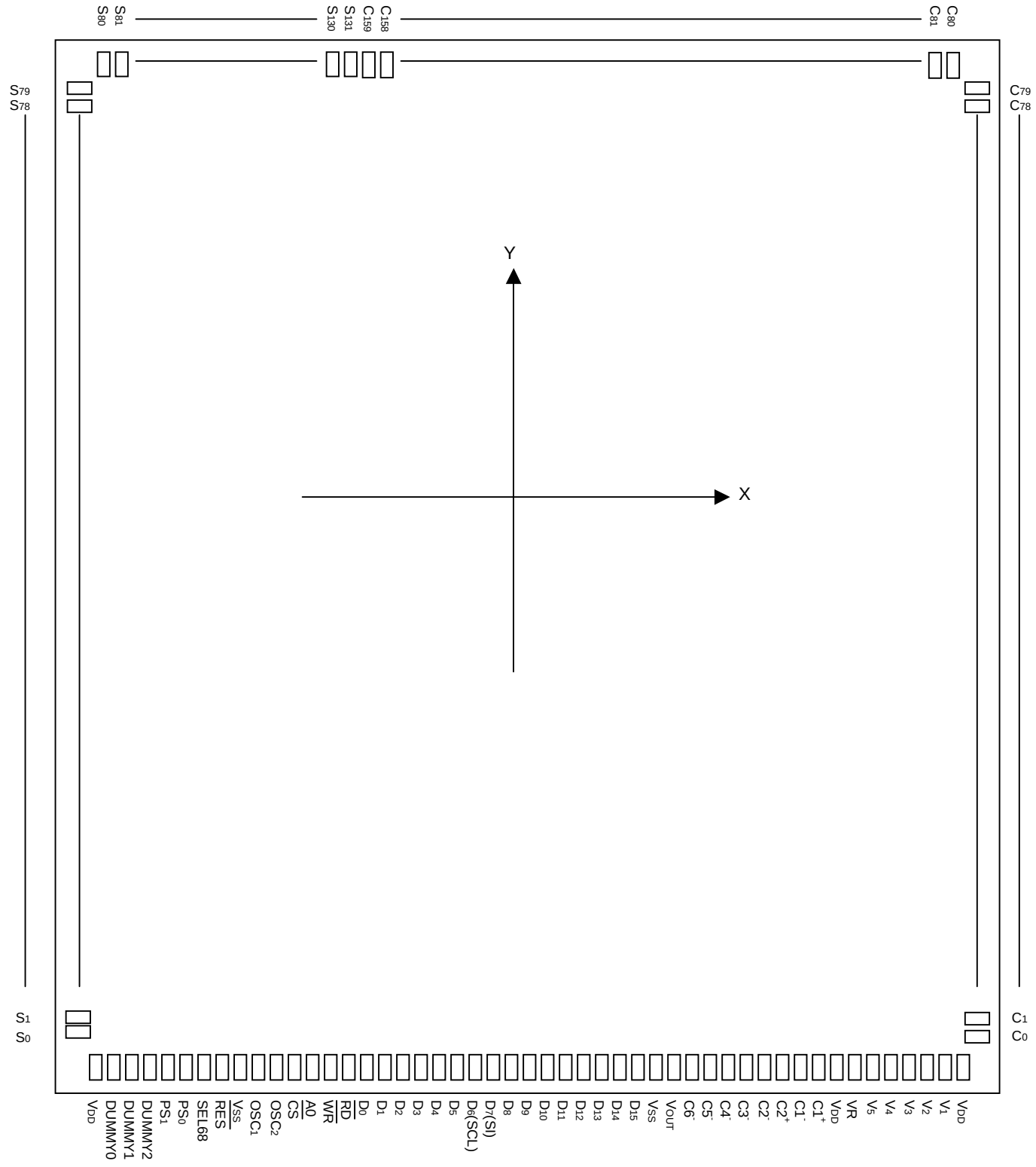
## ■FEATURES

- ●Direct Correspondence between Display Data RAM and LCD Pixel
- ●Display Data RAM - 84,480 bits ;( 160-Com x 132-Seg) x 2-area ) x 2bit
  ….2 times over than display size
- ●Display Method – Monochrome 4-Gray Scale / Black & White
- ●Partial Display Function
  ( 2 blocks of active display area and automatic duty cycle ratio selection )
- ●Variable RAM Mapping
  – The display screen can be composed from the RAM area in a maximum of 8 blocks not to continue.
- ●Easy Vertical Scroll by the variable start line address and over size display data RAM
  (This function doesn't work in Variable RAM Mapping mode )
- ●LCD drivers – 160-common and 132-segment
- ●Direct 8-bit / 16-bit Microprocessor interface for both of 68 type and 80 type MPU
- ●Serial Interface
- ●Programmable Bias selection ; 1/4, 1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11, 1/12, 1/13, 1/14 bias
- ●Common Driver Order Assignment by mask option

| Version | C0 to C159( Pin Name ) |
|---|---|
| NJU6682A | COM0 to COM159 |
| NJU6682B | COM159 to COM0 |

- ●Useful Instruction Set
  Display Data Read/Write, Display ON/OFF, Z-Address Set, X-Address Set, Y-Address Set, Status Read, Normal or Inverse ON/OFF, Static Drive ON/OFF, Partial Display, n-Line Inverse, EVR Resister Set, Variable RAM Mapping Mode, Gray Scale Level Select, Bias Select, Voltage Converter Multiple Select ( 7-times maximum ), Read Modify Write, Reset ,Internal Power Supply, Driver Outputs ON/OFF, Power Save, ADC Select, Display Mode Select, 8-bit / 16-bit Buss Select, etc.
- ●Power Supply Circuit for LCD; Programmable Booster Circuits( 7-time maximum ), Regulator, Voltage Follower x 4
- ●Precision Electrical Variable Resistance
- ●Low Power Consumption T.B.D ( typ. )
- ●Operating Voltage 2.4 to 3.3 V
- ●LCD Driving Voltage 6.0 to 18.0V
- ●Package Outline Bumped Chip / TCP
- ●C-MOS Technology

■PAD LOCATION




| | |
|---|---|
| Chip Center | :X=0um,Y=0um |
| Chip Size | :X=8.27m,Y=5.67mm |
| Chip Thickness | :675um ± 30um |
| Bump Size | :45um x 83um |
| Pad Pitch | :60um (min) |
| Bump Heght | :15um (typ) |
| Bump Material | :Au |

■ PAD Cordinates

Chip Size 8.27x5.67mm(Chip Center X=0um, Y=0um)

| PAD No. | Terminal | X(um) | Y(um) |
|---|---|---|---|
| 1 | $V_{DD}$ | -3933 | -2675 |
| 2 | DUMMY0 | -3863 | -2675 |
| 3 | DUMMY1 | -3793 | -2675 |
| 4 | DUMMY2 | -3723 | -2675 |
| 5 | $PS_1$ | -3562 | -2675 |
| 6 | $PS_0$ | -3325 | -2675 |
| 7 | SEL68 | -3105 | -2675 |
| 8 | $\overline{RES}$ | -2869 | -2675 |
| 9 | $V_{SS}$ | -2712 | -2675 |
| 10 | $OSC_1$ | -2555 | -2675 |
| 11 | $OSC_2$ | -2319 | -2675 |
| 12 | $\overline{CS}$ | -2098 | -2675 |
| 13 | A0 | -1862 | -2675 |
| 14 | $\overline{WR}$ | -1641 | -2675 |
| 15 | $\overline{RD}$ | -1405 | -2675 |
| 16 | $D_0$ | -1168 | -2675 |
| 17 | $D_1$ | -948 | -2675 |
| 18 | $D_2$ | -727 | -2675 |
| 19 | $D_3$ | -507 | -2675 |
| 20 | $D_4$ | -287 | -2675 |
| 21 | $D_5$ | -66 | -2675 |
| 22 | $D_6$(SCL) | 153 | -2675 |
| 23 | $D_7$(SI) | 374 | -2675 |
| 24 | $D_8$ | 594 | -2675 |
| 25 | $D_9$ | 814 | -2675 |
| 26 | $D_{10}$ | 1035 | -2675 |
| 27 | $D_{11}$ | 1255 | -2675 |
| 28 | $D_{12}$ | 1476 | -2675 |
| 29 | $D_{13}$ | 1696 | -2675 |
| 30 | $D_{14}$ | 1916 | -2675 |
| 31 | $D_{15}$ | 2137 | -2675 |
| 32 | $V_{SS}$ | 2298 | -2675 |
| 33 | $V_{OUT}$ | 2368 | -2675 |
| 34 | $C6^-$ | 2464 | -2675 |
| 35 | $C5^-$ | 2613 | -2675 |
| 36 | $C4^-$ | 2683 | -2675 |
| 37 | $C3^-$ | 2832 | -2675 |
| 38 | $C2^-$ | 2902 | -2675 |
| 39 | $C2^+$ | 3050 | -2675 |
| 40 | $C1^-$ | 3120 | -2675 |
| 41 | $C1^+$ | 3269 | -2675 |
| 42 | $V_{DD}$ | 3339 | -2675 |
| 43 | VR | 3519 | -2675 |
| 44 | $V_5$ | 3589 | -2675 |
| 45 | $V_4$ | 3659 | -2675 |
| 46 | $V_3$ | 3729 | -2675 |
| 47 | $V_2$ | 3799 | -2675 |
| 48 | $V_1$ | 3869 | -2675 |
| 49 | $V_{DD}$ | 3939 | -2675 |
| 50 | $C_0$ | 3975 | -2186 |

| PAD No. | Terminal | X(um) | Y(um) |
|---|---|---|---|
| 51 | $C_1$ | 3975 | -2126 |
| 52 | $C_2$ | 3975 | -2066 |
| 53 | $C_3$ | 3975 | -2006 |
| 54 | $C_4$ | 3975 | -1946 |
| 55 | $C_5$ | 3975 | -1886 |
| 56 | $C_6$ | 3975 | -1826 |
| 57 | $C_7$ | 3975 | -1766 |
| 58 | $C_8$ | 3975 | -1706 |
| 59 | $C_9$ | 3975 | -1646 |
| 60 | $C_{10}$ | 3975 | -1586 |
| 61 | $C_{11}$ | 3975 | -1526 |
| 62 | $C_{12}$ | 3975 | -1466 |
| 63 | $C_{13}$ | 3975 | -1406 |
| 64 | $C_{14}$ | 3975 | -1346 |
| 65 | $C_{15}$ | 3975 | -1286 |
| 66 | $C_{16}$ | 3975 | -1226 |
| 67 | $C_{17}$ | 3975 | -1166 |
| 68 | $C_{18}$ | 3975 | -1106 |
| 69 | $C_{19}$ | 3975 | -1046 |
| 70 | $C_{20}$ | 3975 | -986 |
| 71 | $C_{21}$ | 3975 | -926 |
| 72 | $C_{22}$ | 3975 | -866 |
| 73 | $C_{23}$ | 3975 | -806 |
| 74 | $C_{24}$ | 3975 | -746 |
| 75 | $C_{25}$ | 3975 | -686 |
| 76 | $C_{26}$ | 3975 | -626 |
| 77 | $C_{27}$ | 3975 | -566 |
| 78 | $C_{28}$ | 3975 | -506 |
| 79 | $C_{29}$ | 3975 | -446 |
| 80 | $C_{30}$ | 3975 | -386 |
| 81 | $C_{31}$ | 3975 | -326 |
| 82 | $C_{32}$ | 3975 | -266 |
| 83 | $C_{33}$ | 3975 | -206 |
| 84 | $C_{34}$ | 3975 | -146 |
| 85 | $C_{35}$ | 3975 | -86 |
| 86 | $C_{36}$ | 3975 | -26 |
| 87 | $C_{37}$ | 3975 | 34 |
| 88 | $C_{38}$ | 3975 | 94 |
| 89 | $C_{39}$ | 3975 | 154 |
| 90 | $C_{40}$ | 3975 | 214 |
| 91 | $C_{41}$ | 3975 | 274 |
| 92 | $C_{42}$ | 3975 | 334 |
| 93 | $C_{43}$ | 3975 | 394 |
| 94 | $C_{44}$ | 3975 | 454 |
| 95 | $C_{45}$ | 3975 | 514 |
| 96 | $C_{46}$ | 3975 | 574 |
| 97 | $C_{47}$ | 3975 | 634 |
| 98 | $C_{48}$ | 3975 | 694 |
| 99 | $C_{49}$ | 3975 | 754 |
| 100 | $C_{50}$ | 3975 | 814 |

| PAD No. | Terminal | X(um) | Y(um) |
|---|---|---|---|
| 101 | $C_{51}$ | 3975 | 874 |
| 102 | $C_{52}$ | 3975 | 934 |
| 103 | $C_{53}$ | 3975 | 994 |
| 104 | $C_{54}$ | 3975 | 1054 |
| 105 | $C_{55}$ | 3975 | 1114 |
| 106 | $C_{56}$ | 3975 | 1174 |
| 107 | $C_{57}$ | 3975 | 1234 |
| 108 | $C_{58}$ | 3975 | 1294 |
| 109 | $C_{59}$ | 3975 | 1354 |
| 110 | $C_{60}$ | 3975 | 1414 |
| 111 | $C_{61}$ | 3975 | 1474 |
| 112 | $C_{62}$ | 3975 | 1534 |
| 113 | $C_{63}$ | 3975 | 1594 |
| 114 | $C_{64}$ | 3975 | 1654 |
| 115 | $C_{65}$ | 3975 | 1714 |
| 116 | $C_{66}$ | 3975 | 1774 |
| 117 | $C_{67}$ | 3975 | 1834 |
| 118 | $C_{68}$ | 3975 | 1894 |
| 119 | $C_{69}$ | 3975 | 1954 |
| 120 | $C_{70}$ | 3975 | 2014 |
| 121 | $C_{71}$ | 3975 | 2074 |
| 122 | $C_{72}$ | 3975 | 2134 |
| 123 | $C_{73}$ | 3975 | 2194 |
| 124 | $C_{74}$ | 3975 | 2254 |
| 125 | $C_{75}$ | 3975 | 2314 |
| 126 | $C_{76}$ | 3975 | 2374 |
| 127 | $C_{77}$ | 3975 | 2434 |
| 128 | $C_{78}$ | 3975 | 2494 |
| 129 | $C_{79}$ | 3975 | 2554 |
| 130 | $C_{80}$ | 3930 | 2675 |
| 131 | $C_{81}$ | 3870 | 2675 |
| 132 | $C_{82}$ | 3810 | 2675 |
| 133 | $C_{83}$ | 3750 | 2675 |
| 134 | $C_{84}$ | 3690 | 2675 |
| 135 | $C_{85}$ | 3630 | 2675 |
| 136 | $C_{86}$ | 3570 | 2675 |
| 137 | $C_{87}$ | 3510 | 2675 |
| 138 | $C_{88}$ | 3450 | 2675 |
| 139 | $C_{89}$ | 3390 | 2675 |
| 140 | $C_{90}$ | 3330 | 2675 |
| 141 | $C_{91}$ | 3270 | 2675 |
| 142 | $C_{92}$ | 3210 | 2675 |
| 143 | $C_{93}$ | 3150 | 2675 |
| 144 | $C_{94}$ | 3090 | 2675 |
| 145 | $C_{95}$ | 3030 | 2675 |
| 146 | $C_{96}$ | 2970 | 2675 |
| 147 | $C_{97}$ | 2910 | 2675 |
| 148 | $C_{98}$ | 2850 | 2675 |
| 149 | $C_{99}$ | 2790 | 2675 |
| 150 | $C_{100}$ | 2730 | 2675 |

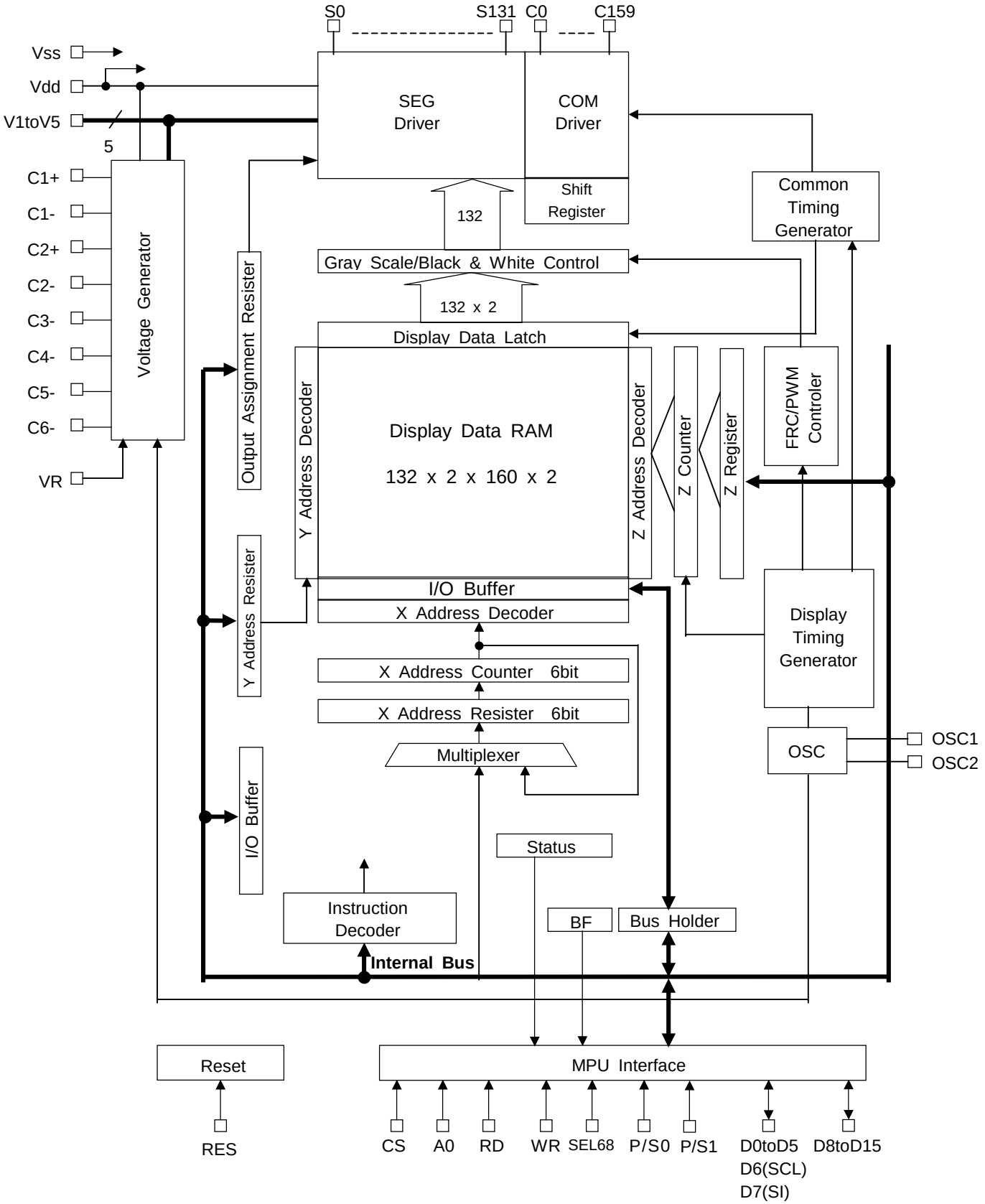
| PAD No. | Terminal | X(um) | Y(um) |
|---|---|---|---|
| 151 | $C_{101}$ | 2670 | 2675 |
| 152 | $C_{102}$ | 2610 | 2675 |
| 153 | $C_{103}$ | 2550 | 2675 |
| 154 | $C_{104}$ | 2490 | 2675 |
| 155 | $C_{105}$ | 2430 | 2675 |
| 156 | $C_{106}$ | 2370 | 2675 |
| 157 | $C_{107}$ | 2310 | 2675 |
| 158 | $C_{108}$ | 2250 | 2675 |
| 159 | $C_{109}$ | 2190 | 2675 |
| 160 | $C_{110}$ | 2130 | 2675 |
| 161 | $C_{111}$ | 2070 | 2675 |
| 162 | $C_{112}$ | 2010 | 2675 |
| 163 | $C_{113}$ | 1950 | 2675 |
| 164 | $C_{114}$ | 1890 | 2675 |
| 165 | $C_{115}$ | 1830 | 2675 |
| 166 | $C_{116}$ | 1770 | 2675 |
| 167 | $C_{117}$ | 1710 | 2675 |
| 168 | $C_{118}$ | 1650 | 2675 |
| 169 | $C_{119}$ | 1590 | 2675 |
| 170 | $C_{120}$ | 1530 | 2675 |
| 171 | $C_{121}$ | 1470 | 2675 |
| 172 | $C_{122}$ | 1410 | 2675 |
| 173 | $C_{123}$ | 1350 | 2675 |
| 174 | $C_{124}$ | 1290 | 2675 |
| 175 | $C_{125}$ | 1230 | 2675 |
| 176 | $C_{126}$ | 1170 | 2675 |
| 177 | $C_{127}$ | 1110 | 2675 |
| 178 | $C_{128}$ | 1050 | 2675 |
| 179 | $C_{129}$ | 990 | 2675 |
| 180 | $C_{130}$ | 930 | 2675 |
| 181 | $C_{131}$ | 870 | 2675 |
| 182 | $C_{132}$ | 810 | 2675 |
| 183 | $C_{133}$ | 750 | 2675 |
| 184 | $C_{134}$ | 690 | 2675 |
| 185 | $C_{135}$ | 630 | 2675 |
| 186 | $C_{136}$ | 570 | 2675 |
| 187 | $C_{137}$ | 510 | 2675 |
| 188 | $C_{138}$ | 450 | 2675 |
| 189 | $C_{139}$ | 390 | 2675 |
| 190 | $C_{140}$ | 330 | 2675 |
| 191 | $C_{141}$ | 270 | 2675 |
| 192 | $C_{142}$ | 210 | 2675 |
| 193 | $C_{143}$ | 150 | 2675 |
| 194 | $C_{144}$ | 90 | 2675 |
| 195 | $C_{145}$ | 30 | 2675 |
| 196 | $C_{146}$ | -30 | 2675 |
| 197 | $C_{147}$ | -90 | 2675 |
| 198 | $C_{148}$ | -150 | 2675 |
| 199 | $C_{149}$ | -210 | 2675 |
| 200 | $C_{150}$ | -270 | 2675 |

| PAD No. | Terminal | X(um) | Y(um) |
|---|---|---|---|
| 201 | $C_{151}$ | -330 | 2675 |
| 202 | $C_{152}$ | -390 | 2675 |
| 203 | $C_{153}$ | -450 | 2675 |
| 204 | $C_{154}$ | -510 | 2675 |
| 205 | $C_{155}$ | -570 | 2675 |
| 206 | $C_{156}$ | -630 | 2675 |
| 207 | $C_{157}$ | -690 | 2675 |
| 208 | $C_{158}$ | -750 | 2675 |
| 209 | $C_{159}$ | -810 | 2675 |
| 210 | $S_{131}$ | -870 | 2675 |
| 211 | $S_{130}$ | -930 | 2675 |
| 212 | $S_{129}$ | -990 | 2675 |
| 213 | $S_{128}$ | -1050 | 2675 |
| 214 | $S_{127}$ | -1110 | 2675 |
| 215 | $S_{126}$ | -1170 | 2675 |
| 216 | $S_{125}$ | -1230 | 2675 |
| 217 | $S_{124}$ | -1290 | 2675 |
| 218 | $S_{123}$ | -1350 | 2675 |
| 219 | $S_{122}$ | -1410 | 2675 |
| 220 | $S_{121}$ | -1470 | 2675 |
| 221 | $S_{120}$ | -1530 | 2675 |
| 222 | $S_{119}$ | -1590 | 2675 |
| 223 | $S_{118}$ | -1650 | 2675 |
| 224 | $S_{117}$ | -1710 | 2675 |
| 225 | $S_{116}$ | -1770 | 2675 |
| 226 | $S_{115}$ | -1830 | 2675 |
| 227 | $S_{114}$ | -1890 | 2675 |
| 228 | $S_{113}$ | -1950 | 2675 |
| 229 | $S_{112}$ | -2010 | 2675 |
| 230 | $S_{111}$ | -2070 | 2675 |
| 231 | $S_{110}$ | -2130 | 2675 |
| 232 | $S_{109}$ | -2190 | 2675 |
| 233 | $S_{108}$ | -2250 | 2675 |
| 234 | $S_{107}$ | -2310 | 2675 |
| 235 | $S_{106}$ | -2370 | 2675 |
| 236 | $S_{105}$ | -2430 | 2675 |
| 237 | $S_{104}$ | -2490 | 2675 |
| 238 | $S_{103}$ | -2550 | 2675 |
| 239 | $S_{102}$ | -2610 | 2675 |
| 240 | $S_{101}$ | -2670 | 2675 |
| 241 | $S_{100}$ | -2730 | 2675 |
| 242 | $S_{99}$ | -2790 | 2675 |
| 243 | $S_{98}$ | -2850 | 2675 |
| 244 | $S_{97}$ | -2910 | 2675 |
| 245 | $S_{96}$ | -2970 | 2675 |
| 246 | $S_{95}$ | -3030 | 2675 |
| 247 | $S_{94}$ | -3090 | 2675 |
| 248 | $S_{93}$ | -3150 | 2675 |
| 249 | $S_{92}$ | -3210 | 2675 |
| 250 | $S_{91}$ | -3270 | 2675 |

| PAD No. | Terminal | X(um) | Y(um) |
|---|---|---|---|
| 251 | $S_{90}$ | -3330 | 2675 |
| 252 | $S_{89}$ | -3390 | 2675 |
| 253 | $S_{88}$ | -3450 | 2675 |
| 254 | $S_{87}$ | -3510 | 2675 |
| 255 | $S_{86}$ | -3570 | 2675 |
| 256 | $S_{85}$ | -3630 | 2675 |
| 257 | $S_{84}$ | -3690 | 2675 |
| 258 | $S_{83}$ | -3750 | 2675 |
| 259 | $S_{82}$ | -3810 | 2675 |
| 260 | $S_{81}$ | -3870 | 2675 |
| 261 | $S_{80}$ | -3930 | 2675 |
| 262 | $S_{79}$ | -3975 | 2517 |
| 263 | $S_{78}$ | -3975 | 2457 |
| 264 | $S_{77}$ | -3975 | 2397 |
| 265 | $S_{76}$ | -3975 | 2337 |
| 266 | $S_{75}$ | -3975 | 2277 |
| 267 | $S_{74}$ | -3975 | 2217 |
| 268 | $S_{73}$ | -3975 | 2157 |
| 269 | $S_{72}$ | -3975 | 2097 |
| 270 | $S_{71}$ | -3975 | 2037 |
| 271 | $S_{70}$ | -3975 | 1977 |
| 272 | $S_{69}$ | -3975 | 1917 |
| 273 | $S_{68}$ | -3975 | 1857 |
| 274 | $S_{67}$ | -3975 | 1797 |
| 275 | $S_{66}$ | -3975 | 1737 |
| 276 | $S_{65}$ | -3975 | 1677 |
| 277 | $S_{64}$ | -3975 | 1617 |
| 278 | $S_{63}$ | -3975 | 1557 |
| 279 | $S_{62}$ | -3975 | 1497 |
| 280 | $S_{61}$ | -3975 | 1437 |
| 281 | $S_{60}$ | -3975 | 1377 |
| 282 | $S_{59}$ | -3975 | 1317 |
| 283 | $S_{58}$ | -3975 | 1257 |
| 284 | $S_{57}$ | -3975 | 1197 |
| 285 | $S_{56}$ | -3975 | 1137 |
| 286 | $S_{55}$ | -3975 | 1077 |
| 287 | $S_{54}$ | -3975 | 1017 |
| 288 | $S_{53}$ | -3975 | 957 |
| 289 | $S_{52}$ | -3975 | 897 |
| 290 | $S_{51}$ | -3975 | 837 |
| 291 | $S_{50}$ | -3975 | 777 |
| 292 | $S_{49}$ | -3975 | 717 |
| 293 | $S_{48}$ | -3975 | 657 |
| 294 | $S_{47}$ | -3975 | 597 |
| 295 | $S_{46}$ | -3975 | 537 |
| 296 | $S_{45}$ | -3975 | 477 |
| 297 | $S_{44}$ | -3975 | 417 |
| 298 | $S_{43}$ | -3975 | 357 |
| 299 | $S_{42}$ | -3975 | 297 |
| 300 | $S_{41}$ | -3975 | 237 |

| PAD No. | Terminal | X(um) | Y(um) |
|---|---|---|---|
| 301 | $S_{40}$ | -3975 | 177 |
| 302 | $S_{39}$ | -3975 | 117 |
| 303 | $S_{38}$ | -3975 | 57 |
| 304 | $S_{37}$ | -3975 | -2 |
| 305 | $S_{36}$ | -3975 | -62 |
| 306 | $S_{35}$ | -3975 | -122 |
| 307 | $S_{34}$ | -3975 | -182 |
| 308 | $S_{33}$ | -3975 | -242 |
| 309 | $S_{32}$ | -3975 | -302 |
| 310 | $S_{31}$ | -3975 | -362 |
| 311 | $S_{30}$ | -3975 | -422 |
| 312 | $S_{29}$ | -3975 | -482 |
| 313 | $S_{28}$ | -3975 | -542 |
| 314 | $S_{27}$ | -3975 | -602 |
| 315 | $S_{26}$ | -3975 | -662 |
| 316 | $S_{25}$ | -3975 | -722 |
| 317 | $S_{24}$ | -3975 | -782 |
| 318 | $S_{23}$ | -3975 | -842 |
| 319 | $S_{22}$ | -3975 | -902 |
| 320 | $S_{21}$ | -3975 | -962 |
| 321 | $S_{20}$ | -3975 | -1022 |
| 322 | $S_{19}$ | -3975 | -1082 |
| 323 | $S_{18}$ | -3975 | -1142 |
| 324 | $S_{17}$ | -3975 | -1202 |
| 325 | $S_{16}$ | -3975 | -1262 |
| 326 | $S_{15}$ | -3975 | -1322 |
| 327 | $S_{14}$ | -3975 | -1382 |
| 328 | $S_{13}$ | -3975 | -1442 |
| 329 | $S_{12}$ | -3975 | -1502 |
| 330 | $S_{11}$ | -3975 | -1562 |
| 331 | $S_{10}$ | -3975 | -1622 |
| 332 | $S_{9}$ | -3975 | -1682 |
| 333 | $S_{8}$ | -3975 | -1742 |
| 334 | $S_{7}$ | -3975 | -1802 |
| 335 | $S_{6}$ | -3975 | -1862 |
| 336 | $S_{5}$ | -3975 | -1922 |
| 337 | $S_{4}$ | -3975 | -1982 |
| 338 | $S_{3}$ | -3975 | -2042 |
| 339 | $S_{2}$ | -3975 | -2102 |
| 340 | $S_{1}$ | -3975 | -2162 |
| 341 | $S_{0}$ | -3975 | -2222 |

■BLOCK DIAGRAM



## ■TERMINAL DESCRIPTION

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>2 to 4</td><td>DUMMY</td><td></td><td>Dummy Terminals.<br>These terminals are insulated.</td></tr>
<tr><td>1,42,49</td><td>VDD</td><td>Power</td><td>2.4V to 3.3V</td></tr>
<tr><td>9,32</td><td>VSS</td><td>GND</td><td>GND</td></tr>
<tr><td>48<br>47<br>46<br>45<br>44</td><td>V1<br>V2<br>V3<br>V4<br>V5</td><td>Power</td><td>LCD Driving Voltage Supplying Terminal. When the internal voltage booster is not used, supply each level of LCD driving voltage from outside with following relation.<br>VDD≥V1≥V2≥V3≥V4≥V5<br><br>When the internal power supply is used, the internal circuits generate and supply following LCD bias voltage from V1 to V4 terminals.
<table>
<tr><th>Bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/4Bias</td><td>V5+3/4Vlcd</td><td>V5+2/4Vlcd</td><td>V5+2/4Vlcd</td><td>V5+1/4Vlcd</td></tr>
<tr><td>1/5Bias</td><td>V5+4/5Vlcd</td><td>V5+3/5Vlcd</td><td>V5+2/5Vlcd</td><td>V5+1/5Vlcd</td></tr>
<tr><td>1/6Bias</td><td>V5+5/6Vlcd</td><td>V5+4/6Vlcd</td><td>V5+2/6Vlcd</td><td>V5+1/6Vlcd</td></tr>
<tr><td>1/7Bias</td><td>V5+6/7Vlcd</td><td>V5+5/7Vlcd</td><td>V5+2/7Vlcd</td><td>V5+1/7Vlcd</td></tr>
<tr><td>1/8Bias</td><td>V5+7/8Vlcd</td><td>V5+6/8Vlcd</td><td>V5+2/8Vlcd</td><td>V5+1/8Vlcd</td></tr>
<tr><td>1/9Bias</td><td>V5+8/9Vlcd</td><td>V5+7/9Vlcd</td><td>V5+2/9Vlcd</td><td>V5+1/9Vlcd</td></tr>
<tr><td>1/10Bias</td><td>V5+9/10Vlcd</td><td>V5+8/10Vlcd</td><td>V5+2/10Vlcd</td><td>V5+1/10Vlcd</td></tr>
<tr><td>1/11Bias</td><td>V5+10/11Vlcd</td><td>V5+9/11Vlcd</td><td>V5+2/11Vlcd</td><td>V5+1/11Vlcd</td></tr>
<tr><td>1/12Bias</td><td>V5+11/12Vlcd</td><td>V5+10/12Vlcd</td><td>V5+2/12Vlcd</td><td>V5+1/12Vlcd</td></tr>
<tr><td>1/13Bias</td><td>V5+12/13Vlcd</td><td>V5+11/13Vlcd</td><td>V5+2/13Vlcd</td><td>V5+1/13Vlcd</td></tr>
<tr><td>1/14Bias</td><td>V5+13/14Vlcd</td><td>V5+12/14Vlcd</td><td>V5+2/14Vlcd</td><td>V5+1/14Vlcd</td></tr>
</table>
(Vlcd=Vdd-V5)</td></tr>
<tr><td>41<br>40<br>39<br>38<br>37<br>36<br>35<br>34</td><td>C1+<br>C1-<br>C2+<br>C2-<br>C3-<br>C4-<br>C5-<br>C6-</td><td>O</td><td>Step up capacitor connecting terminals.<br>Voltage booster circuit ( adjustable with 2 to 7 times )</td></tr>
<tr><td>33</td><td>VOUT</td><td>O</td><td>Step up voltage output terminal. Connect the step up capacitor between this terminal and VSS.</td></tr>
<tr><td>43</td><td>VR</td><td>I</td><td>Voltage adjust terminal. V5 level is adjusted by external bleeder resistance connecting between VDD and V5 terminal.</td></tr>
<tr><td>16<br>to<br>23<br>(23)<br>(22)</td><td>D0<br>to<br>D7<br>(SI)<br>(SCL)</td><td>I/O</td><td>( P/S="H" )In Pararel Interface Mode<br>•8-bit bus mode*1: I/O terminals for 8-bit bus.<br>•16-bit bus mode*1: I/O terminals for the 8-bits of lower ranks of 16-bit bus.<br><br>*1 To set these 8-bit / 16-bit mode, use Instruction ” 8-bit / 16-bit Bus Select ”.<br><br>( P/S="L" )In Serial Interface Mode<br>•D7: Input terminal for serial data ( SI ).<br>•D6: Input terminal for serial data clock ( SCL ).<br>When select these mode, D0 to D5 will be Hi-Z status.<br><br>( CS=”H” ) D0 to D7 shown Hi-Z.</td></tr>
</table>

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>24<br>to<br>30</td><td>D8<br>to<br>D15</td><td>I/O</td><td>8-bit Bus Mode & Serial Mode<br>•Output terminal with Hi-Z status.<br>16-bit Bus Mode<br>•I/O terminals for the upper 8-bits of 16-bit bus.</td></tr>
<tr><td>13</td><td>A0</td><td>I</td><td>Normaly, connect to the address bus of MPU. The data on the D0 to D7 is distinguished as Display Data or Instruction by status of A0.
<table>
<tr><th>PS1 terminal</th><th>PS0 terminal</th><th>Ao terminal</th><th>Distinction</th></tr>
<tr><td rowspan="2">H</td><td rowspan="2">—</td><td>H</td><td>Display Data</td></tr>
<tr><td>L</td><td>Instruction</td></tr>
<tr><td rowspan="3">L</td><td rowspan="2">H</td><td>H</td><td>Display Data</td></tr>
<tr><td>L</td><td>Instruction</td></tr>
<tr><td>L</td><td>—</td><td>The 17th data of serial data is recognized as A0.</td></tr>
</table>
— : H or L</td></tr>
<tr><td>8</td><td>$\overline{\text{RES}}$</td><td>I</td><td>Reset terminal. When the $\overline{\text{RES}}$ terminal goes to “L”, the initialization is performed. Reset operation is executing during “L” state of $\overline{\text{RES}}$.</td></tr>
<tr><td>12</td><td>$\overline{\text{CS}}$</td><td>I</td><td>Chip serect terminal. Data Input/Output are available during $\overline{\text{CS}}$=”L”.</td></tr>
<tr><td rowspan="2">15</td><td>$\overline{\text{RD}}$</td><td>I</td><td>< In case of 80 type MPU ( PS1=”H”, SEL68=”L” ) ><br>RD signal of 80 type MPU input terminal. Active “L”.<br>During this signal is “L”, D0 to D7 terminals are output.</td></tr>
<tr><td>(E)</td><td>I</td><td>< In case of 68 type MPU ( PS1=”H”, SEL68=”H” ) ><br>Enable signal of 68 type MPU input terminal. Active “H”.</td></tr>
<tr><td rowspan="2">14</td><td>$\overline{\text{WR}}$</td><td>I</td><td>< In case of 80 type MPU ( PS1=”H”, SEL68=”L” ) ><br>Connect to the 80 type MPU WR signal. Active “L”.<br>The data on the data bus input syncronizeing the rise edge of this terminal.</td></tr>
<tr><td>(R/W)</td><td>I</td><td>< In case of 68 type MPU ( PS1=”H”, SEL68=”H” ) ><br>The read / Write control signal of 68 type MPU input terminal.
<table>
<tr><td>R/W</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>Read</td><td>Write</td></tr>
</table></td></tr>
<tr><td>7</td><td>SEL68</td><td>I</td><td>MPU interface type selection terminal.
<table>
<tr><td>SEL68</td><td>H</td><td>L</td></tr>
<tr><td>State</td><td>68 type</td><td>80 type</td></tr>
</table></td></tr>
<tr><td>6<br>5</td><td>PS0<br>PS1</td><td>I</td><td>Serial or parallel type interface selection terminal.
<table>
<tr><th>PS1</th><th>PS0</th><th>Interface</th><th>Chip Select</th><th>Data/ Command</th><th>Data</th><th>Read/ Write</th><th>Serial Clock</th></tr>
<tr><td>“H”</td><td>-</td><td>Parallel</td><td>$\overline{\text{CS}}$</td><td>A0</td><td>$\overline{\text{RD}}$ $\overline{\text{WR}}$</td><td>Write Only</td><td>-</td></tr>
<tr><td rowspan="2">“L”</td><td>“H”</td><td>Serial 4-wire</td><td>$\overline{\text{CS}}$</td><td>A0</td><td>SI(D7)</td><td>Write Only</td><td>SCL (D6)</td></tr>
<tr><td>“L”</td><td>Serial 3-wire</td><td>$\overline{\text{CS}}$</td><td>The 17th data of serial data is recognized as A0.</td><td>SI(D7)</td><td>Write Only</td><td>SCL (D6)</td></tr>
</table>
•In case of serial interface ( PS1=0 ), $\overline{\text{RD}}$ and $\overline{\text{WR}}$ must be fixed to “H” or “L”, and D0 to D5 will be Hi-Z.</td></tr>
<tr><td>10<br>11</td><td>OSC1<br>OSC2</td><td>I/O</td><td>System clock input terminal for Maker testing. ( This terminal should be Open )<br>For external clock operation, the clock should be input to OSC1 terminal.</td></tr>
</table>

<table>
<tr><th>No</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>50<br>to<br>209</td><td>C0<br>to<br>C159</td><td rowspan="2">O</td><td rowspan="2">LCD driving signal output terminal.<br>•Common output terminal :C0 to C159<br>•Segment output terminal :S0 to S131<br><br>•Segment output terminal<br>The following output voltage are selected by the combination of FR and data in the RAM.
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">Alternating Signal</th><th colspan="2">Sn OutPut Voltage</th></tr>
<tr><th>Disp. Positive</th><th>Disp. Negative</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>VDD</td><td>V2</td></tr>
<tr><td>L</td><td>V5</td><td>V3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V2</td><td>VDD</td></tr>
<tr><td>L</td><td>V3</td><td>V5</td></tr>
</table>
<br>•Common output terminal<br>The following output voltage are selected by the combination of FR and status of common.
<table>
<tr><th>Scan Data</th><th>Alternating Signal</th><th>COn Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V5</td></tr>
<tr><td>L</td><td>VDD</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
</table></td></tr>
<tr><td>341<br>to<br>210</td><td>S0<br>to<br>S131</td></tr>
</table>

Functional Description

(1)Description for each blocks

1-1) Busy Flag (BF)

As for NJU6682, in case of the inner operation, busy flag (BF) doesn't accept an instruction except of "1". In the status reed instruction, a busy flag is output by the D7 terminal. If cycle time (tcyc) is secured, to check this flag in front of the instruction isn't necessary and the throughput of the CPU can be substantially improved.

1-2) X-Address Counter

The X-address counter is the 6 bit presettable counter which gives an address for the row of the display data RAM as shown in figure 1 and is done in +1 increment by the execution of the display data read / write instruction. But, when the X-address counter reaches the maximum of the exist address, the count locks by the X-address counter. With to set X-address once again, as for the count lock of cancellation again this counter is independent with Y-address register.

By the address inverse instruction(ADC), it is possible for X-address decoder to reverse correspondence relation between X-address and segment output of display data RAM.

1-3)Z-Address counter

The Y-address counter generates an address to the display RAM direction of the line, it is reset when the inner FR signal switching timing and count up synchronizes with common cycle of NJU6682.

1-4)Y-Address Register

Y-address register is which gives an address to the display data RAM direction of the line as shown in figure 1. When replacing Y-address from the CPU and accessing to them, it does by the instruction of the set of Y-address.

1-5)Z-Address Register

Z-address register can be generally used for the scrolling of a screen, in addition to the display with the register which sets the low address of the data RAM which corresponds to the display line ( being the best line generally ) of COM0. It sets a display beginning line by setting the display beginning address of 9 bits in this register by the instruction of the set of Z-address.

1-6)Display data RAM

Display data RAM is the bit map RAM which stores the data for the display which corresponds to the LCD pixel and is composed of 84,480 bits. Each bit of the display data RAM corresponds to 2:1 in case of gray scale display to each pixel of LCD and in case of Black and White display, it corresponds to 1:1. The relation between the display data and the LCD in case of gray scale display is as follows.

The relation between Display data and LCD in Gray Scale Display

The Display RAM data : "00" = Gray Scale Level 0 ( setting by the gray scale level select )
The Display RAM data : "01" = Gray Scale Level 1 ( " )
The Display RAM data : "10" = Gray Scale Level 2 ( " )
The Display RAM data : "11" = Gray Scale Level 3 ( " )

The relation between Display data and LCD in Black and White Display

In Positive Display : "1"=Turn-On Display,"0" =Turn-Off Display
In Negative Display: "1"=Turn-Off Display,"0" =Turn-On Display

When the Display method chooses 16 bit access by the gray scale display, because RAM area of X-address = 16 become 8 bits, lower 8bit (D7-D0) is ignored ( Figure 1-1 ). When the display method chooses 16 bit access by the Black and White display, as for RAM area of X-address = 8 (Layer0) or 40 (Layer1) becomes 4-bits, lower 12 bit (D11-D0) is ignored. The bus with in access to the Display Data RAM is 8-bit access an d 16-bit access with the 8-bit / 16-bit Bus Select instruction. The access can be chosen.

Correspondence with Display Data RAM Address ( in gray scale mode)

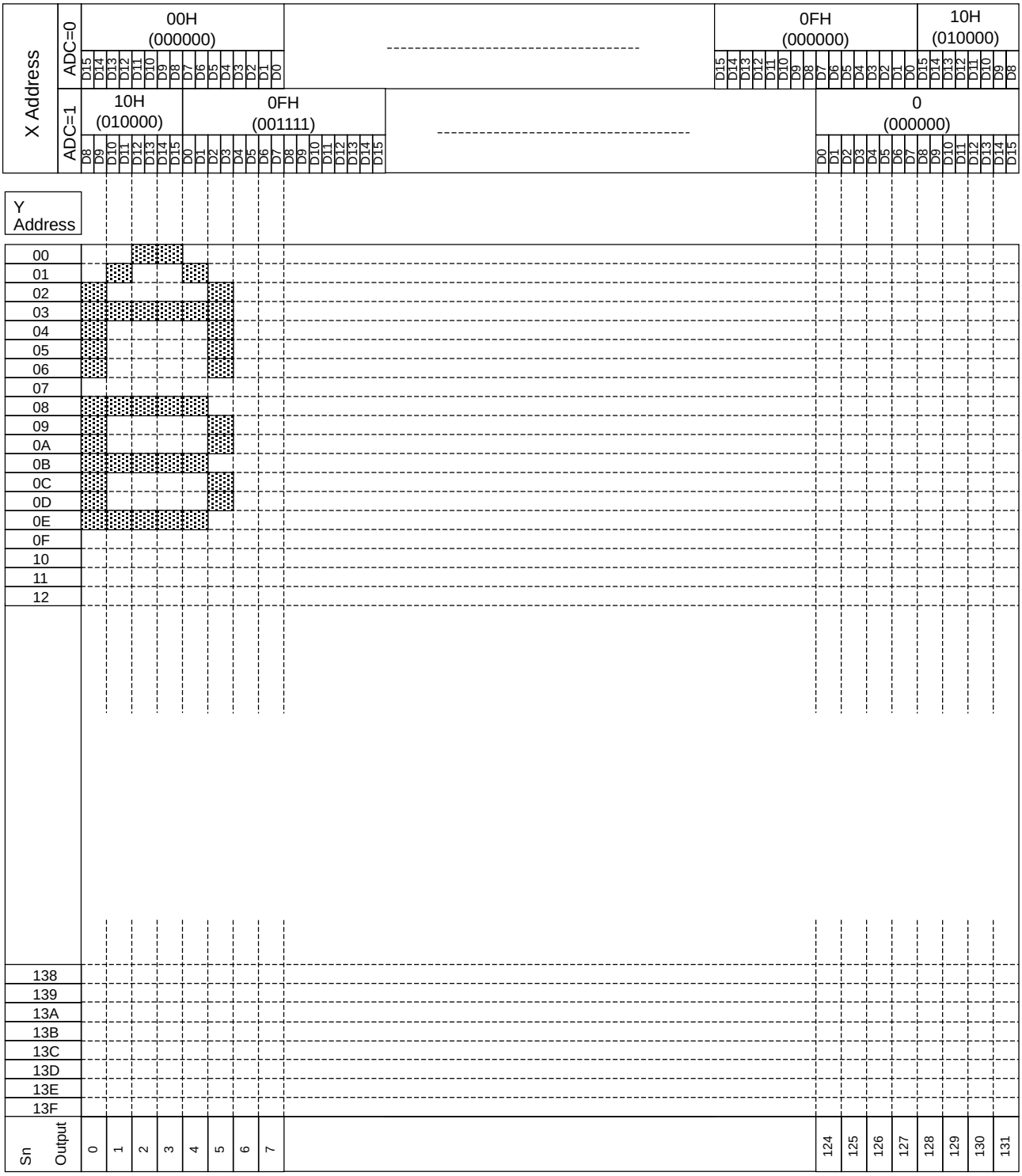



Fig.1-1

Correspondence with Display Data RAM Address ( in black & white mode)

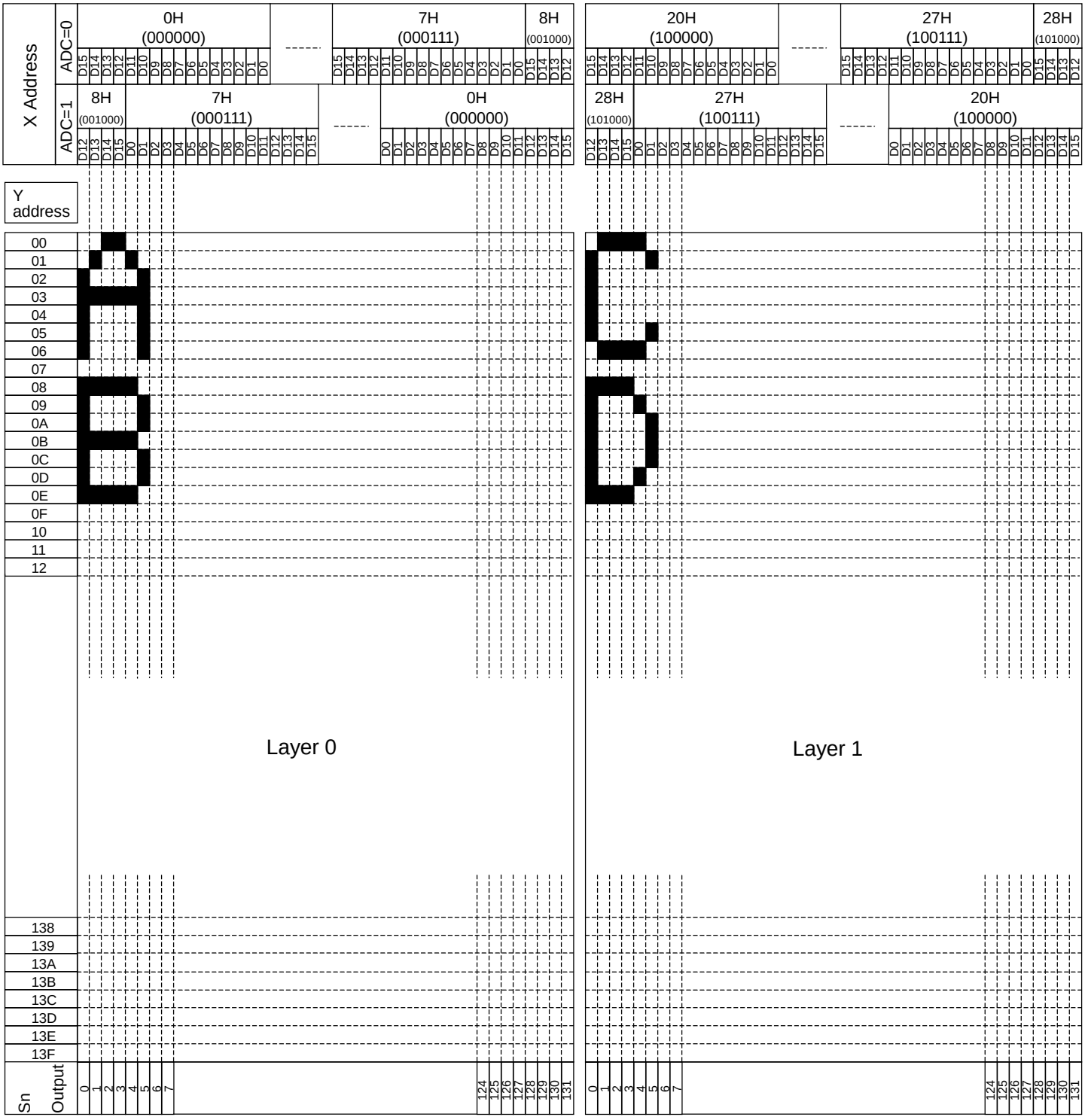



Fig.1-1

1-7)Output Assignment Register
This circuit can choose the direction of the scan of the common output.

Table1

| | Common Output Terminal | | |
|---|---|---|---|
| PAD No. | 50 | | 209 |
| Terminal Name | C0 | | C159 |
| Ver. A | COM0 | → | COM159 |
| Ver. B | COM159 | ← | COM0 |

•Able to be changed with the mask option of it by the choice (version A or B) to the common scan direction.
1-8)Reset Circuit
This reset circuit does following initialization when the RES input becomes “L” level.

•The initialization condition (The default setting)
1.It sets a display method in the 4 Gray Scale Display Mode.
2.Display Off
3.Display Positive
4.ADC select ; Positive
5.Read Modify Write
6.Voltage Booster off, Voltage Regulator off, Voltage follower off
7.Static Drive off
8.Driver output off
9.Clear the register data of serial interface
10.Set the X-address counter to (00)h
11.Set the Y-Address register to (00)h
12.Set the Z-Address at (00)h
13.The continuous RAM address(Variable RAM Mapping Mode)
14.Set the EVR register to (FF)h
15.Set the Duty 1/160 (Whole Display On)
16.Bias select D3,2,1,0="1,0,1,0" (1/14 Bias)
17.Voltage Booster Select D2,1,0,="1,0,1" ((7 times)
18.Set n-line inverting register to (0)h
19.Set to 8 Bit bus interface mode

To be in " the MPU interface ( the reference example ) ", the RES terminal make connect with the reset terminal of the MPU and does at the same time as a MPU is initialized. The reset signal must put "L" pulse above minimum 10us to be in the clause of " the DC characteristic ". The RES signal becomes an operation condition generally after 1us from the rise-up edge.

When not using a built-in LCD power supply circuit in NJU6682, in case of the outside liquid crystal power supply turning on, it is necessary to be RES="L". It clears each register by RES="L" and it is set in the above initialization condition but it doesn't have an influence about the oscillation circuit and output terminal (D0-D15).

When initialization by the RES terminal isn't accomplished in power supply impressing, it sometimes enters the condition about which it is impossible to cancel.

When using a reset instruction, 9 - 19 of the above initialization are executed.

1-9)The LCD drive circuit system

1-9-1)The LCD drive circuit

The common output has a shift register and it forwards a common scan signal in order. It outputs liquid crystal drive voltage in the combination of the display data, the common scan signal, the inner FR signal, the liquid crystal flowing mutually signal. A segment, common output corrugated example are shown in figure 2.

1-9-2)Display Data Latch-Circuit

The display data latch circuit is the latch which stores the display data of 132 x 2 bits which are addressed by the Z-address counter and are output from the display data RAM to the LCD drive circuit every 1 common 1 period temporarily. Data in the display data RAM is changed and not held because display turn to Positive / Negative ( In case of Black & White display ),displaying on / off, Static Drive On / Off instructions are controls data in this latch circuit.

1-9-3)Gray Scale / Black & White Control Circuit

A Gray Scale control circuit chooses the gray scale level which was set by the command instruction from the gray scale data of 264 bits which latched with the display data latch circuit and is output for LCD drive output Sn. A Black & White display control circuit chooses layer which was set by the command instruction from the 264 bit Black & White data which latched with the display data latch circuit and is output for LCD drive output Sn.

1-9-4)Z-Counter, Signal Genelate of Display Data Latch Circuit

It generates a latch signal to the clock(CL) to Z-counter and to the display data latch circuit. It synchronizes with the internal display clock and the line address of the display data RAM occurs, and the display data of 132 x 2 bits synchronizes with the display clock, latches by the display data latch circuit and is output by the gray scale control / Black & White display control circuit. The read out to the display data LCD drive circuit is independent totally with the access to the display data RAM from the CPU.

1-9-5)Display Timing Genelate Circuit

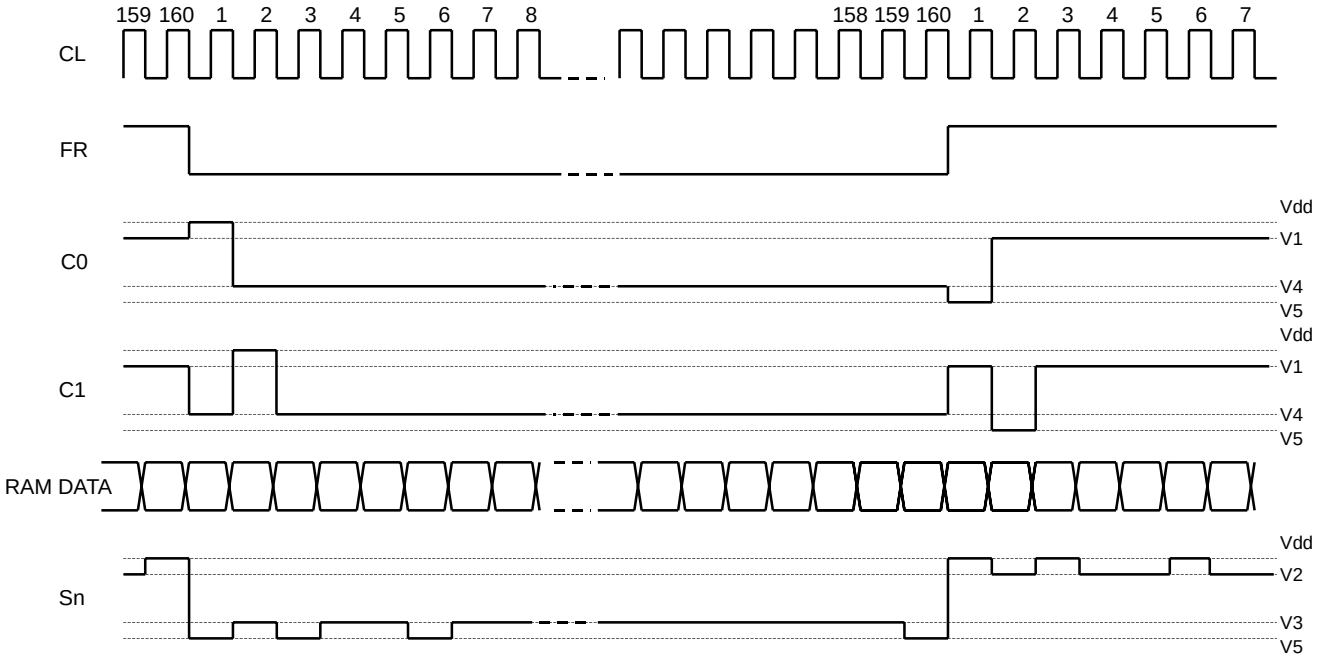
The display timing occurrence circuit generates the internal timing of the display system by the master clock and the internal FR signal. As for it, the internal FR signal and the LCD flowing mutually signal make the drive corrugation of the 2 frame alternating current drive or the n-line inverting drive method occur to the LCD Driving circuit.

1-9-6)FRC / PWM Control Circuit

PWM & FRC(Frame Rate Control) to realize 4Gray Scale display function.

1-9-7)Common Timing Genegation
The common timing is generated by display clock CL ( refer to Fig. )

① 2 frame alternating current drive mode




② n-line inverting drive mode

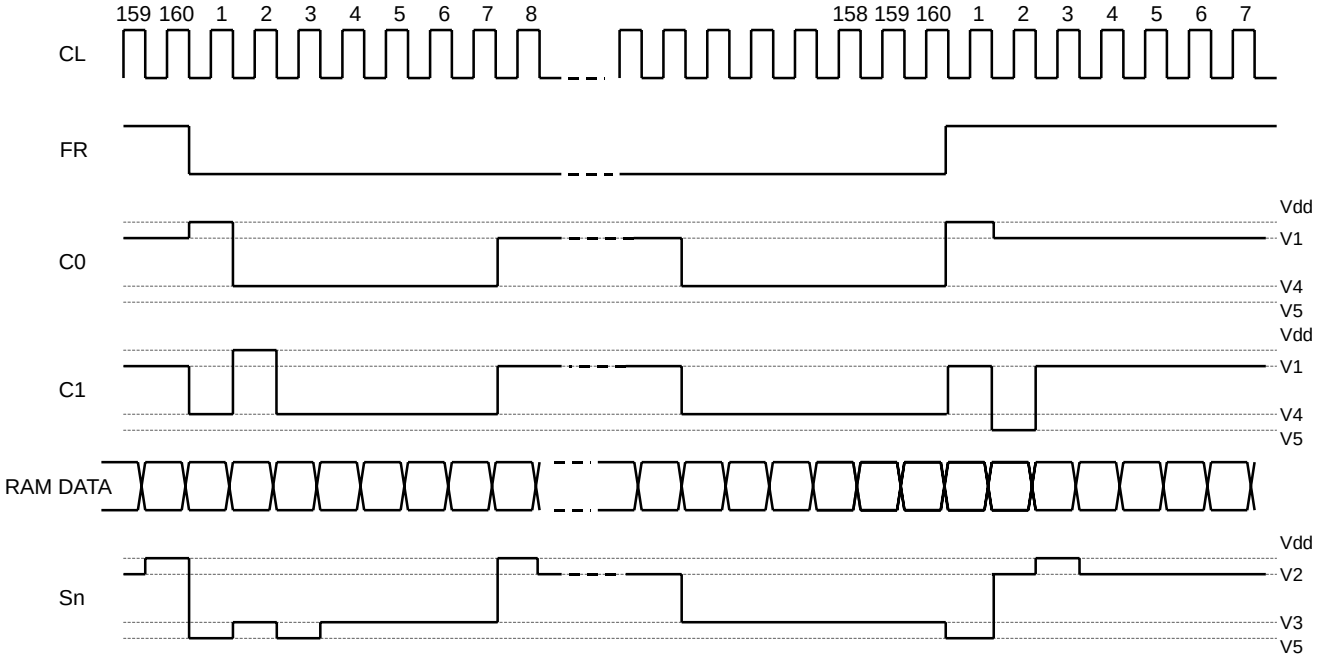



Fig.2 Waveform of Display Timing

1-9-8)Oscillation Circuits

The Oscillation Circuit is a low power CR oscillator incorporating with a Resistor and a Capacitor. it generates clocks for display timing signal source and the clock for step up circuits for LCD driving. The oscillation circuit output frequency is divided as display clock CL.

Table 3

| Duty | 1/4 | 1/8 | 1/12 | 1/16 | 1/20 | 1/24 | 1/28 | 1/32 | 1/36 | 1/40 | 1/44, 1/48 | 1/52, 1/56 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Divide | 1/1200 | 1/600 | 1/400 | 1/300 | 1/240 | 1/200 | 1/170 | 1/150 | 1/135 | 1/120 | 1/105 | 1/90 |

| Duty | 1/60, 1/64, 1/68 | 1/72, 1/76, 1/80, 1/84, 1/88 | 1/92, 1/96, 1/100, 1/104, 1/108, 1/112, 1/116, 1/120 |
|---|---|---|---|
| Divide | 1/75 | 1/60 | 1/45 |

| Duty | 1/124, 1/128, 1/132, 1/136, 1/140, 1/144, 1/148, 1/152, 1/156, 1/160 |
|---|---|
| Divide | 1/30 |

1-9-9)Power Supply Circuits

Internal Power Supply Circuit generates voltage for LCD driving. The power supply circuits consists of Step Up Circuits ( 2 times to 7 times ), Regulator Circuits, and Voltage Followers. The internal Power Supply is designed for small size LCD panel, therefore it is not suitable for the large size LCD panel application, please supply the external.

The suitable value of the capacitors connecting to the V1 to V5 terminals and the step up circuit, and the feedback resistors for V5 operational amplifier depend on the LCD panel. And the power consumption with the LCD panel is depending on the display pattern. Please evaluate with actual LCD module.

The operation of Internal Power Supply Circuits is controlled by the Internal Power Supply Control Instruction.

( R / W )

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | * | * | * | * | * | DC | VR | VF |

*:Don't Care

DC : Step Up Circuit

DC=1 : Step Up Circuit ON

DC=0 : Step Up Circuit OFF ( In this time, terminals C1+,C1-,C2+,C2-,C3-,C4-,C5- and C6- should be open, and VOUT should be supplied from outside. )

VR : Regulator Circuit

VR=1 : Regulator Circuit ON

VR=0 : Regulator Circuit OFF ( In this time, terminal VR should be open, and V5 should be supplied from outside. )

VF : Voltage Follower

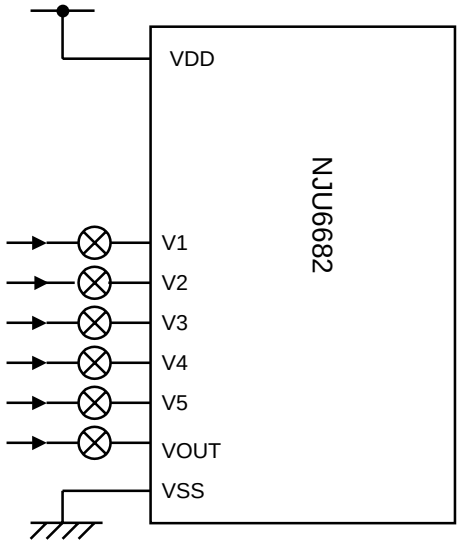
VR=1 : Voltage Follower ON

VR=0 : Voltage Follower OFF ( In this time, terminals V1 to V5 should be supplied from outside. )

Examples for application circuits of the internal Power Supply

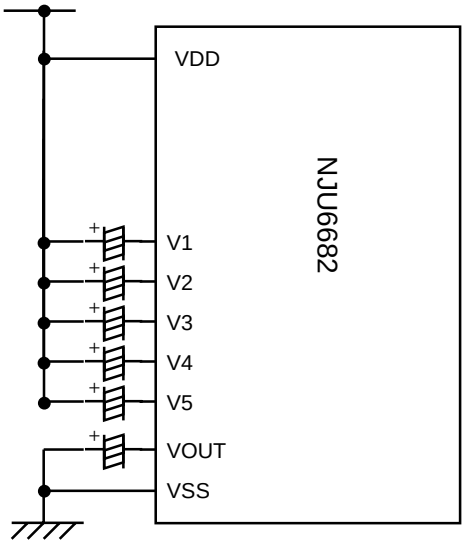
①None of the internal power supply functions

( DC,VR,VF ) = ( 0, 0, 0 )



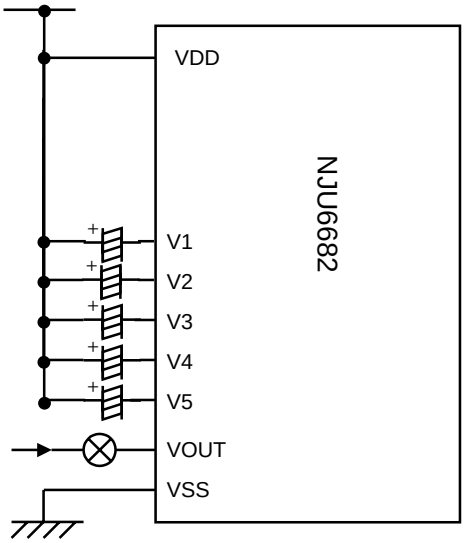

②All of the internal power supply functions.
( Step Up, Voltage Regulator, Voltage Follower )

( DC,VR,VF ) = ( 1, 1, 1 )



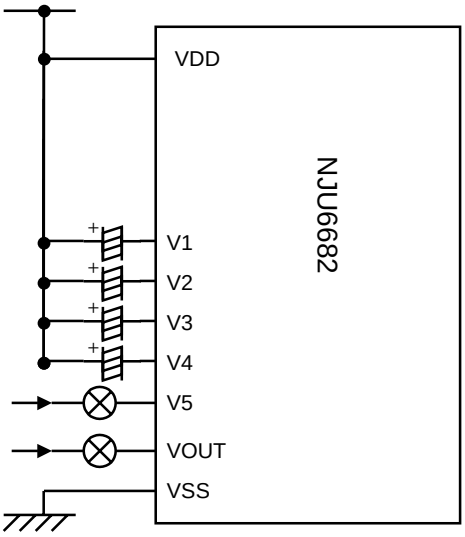

③Some of the internal power supply functions
( Voltage Regulator, Voltage Follower )

( DC,VR,VF ) = ( 0, 1, 1 )




④Some of the internal power supply functions.
( Voltage Follower )

( DC,VR,VF ) = ( 0, 0, 1 )




( Caution ) ⊗ : These switches should be open during the power save mode.

(2)Instruction

The NJU6682 distinguishes the signal on the data bus D0 to D15 by conbination of A0, $\overline{RD}$, and $\overline{WR}$(R/W). The decode of the instruction and exection performes only depending on the internal timing only neither the external clock. In case of serial interface, the data input as MSB first serially.

The table.4 shows the instruction codes of the NJU6682.

Table.4

| Instruction | | Code | | | | | | | | | | | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| (1) | Display ON/OFF | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | | | | | | | 0<br>1 | LCD Display ON/OFF<br>D0=0:OFF, D0=1:ON |
| (2) | Z Address Set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | Line Address | | | | | | | | | Determine the Line Address of RAM to the COM0. |
| (3) | X Address Set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | * | * | X Address | | | | | | Determine the X Address of Display RAM. |
| (4) | Y Address Set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | Y Address | | | | | | | | | Determine the Y Address of Display RAM. |
| (5) | Status Read | 0 | 0 | 1 | Status | | | | | | 0 | 0 | Status | | | | | | 0 | 0 | Read out the internal status. |
| (6) | Write Desplay Data | 1 | 1 | 0 | Write Data | | | | | | | | | | | | | | | | Write the data into the Display Data RAM |
| (7) | Read Desplay Data | 1 | 0 | 1 | Read Data | | | | | | | | | | | | | | | | Read the data from the Display Data RAM |
| (8) | Normal or Inverse of ON/OFF | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | | | | | | | 0<br>1 | Inverse the ON and OFF Display<br>D0=0:Normal D0=1:Inverse |
| (9) | Static Drive ON/OFF | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | * | | | | | | | 0<br>1 | Whole Display Turns ON<br>D0=0:Normal D0=1:Whole Display ON |
| (10) | Partial Display | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | * | Start Unit of 1st Block | | | | | | | Set the Display Start Unit of Block 1 |
| | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | * | Display Unit Number of 1st Block | | | | | | | Set the Display Unit Number of Block 1 |
| | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | * | Start Unit of 2nd Block | | | | | | | Set the Display Start Unit of Block 2 |
| | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | * | Display Unit Number of 2nd Block | | | | | | | Set the Display Unit Number of Block 2 |
| | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | * | | | | | | | 0 | Display the Status |
| (11) | n-Line Inverse Resister Set | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | * | The Number of Inverse Line | | | | | | | Set the number of inverse line |
| (12) | EVR Resister Set | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | EVR Resister Data | | | | | | | | Set the V5 output level to the EVR resister |
| (13) | Variable RAM Mapping Mode | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Y Address of Display Block 1 | | | | | | | | | Set Y address of Display block 1 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | * | Line Number of Block 1 | | | | | | | Set the line number of Display block 1 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | Y Address of Display Block 2 | | | | | | | | | Set Y address of Display block 2 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | * | Line Number of Block 2 | | | | | | | Set the line number of Display block 2 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | Y Address of Display Block 3 | | | | | | | | | Set Y address of Display block 3 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | * | Line Number of Block 3 | | | | | | | Set the line number of Display block 3 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | Y Address of Display Block 4 | | | | | | | | | Set Y address of Display block 4 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | * | Line Number of Block 4 | | | | | | | Set the line number of Display block 4 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | Y Address of Display Block 5 | | | | | | | | | Set Y address of Display block 5 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | * | Line Number of Block 5 | | | | | | | Set the line number of Display block 5 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | Y Address of Display Block 6 | | | | | | | | | Set Y address of Display block 6 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | * | Line Number of Block 6 | | | | | | | Set the line number of Display block 6 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | Y Address of Display Block 7 | | | | | | | | | Set Y address of Display block 7 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | * | Line Number of Block 7 | | | | | | | Set the line number of Display block 7 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | Y Address of Display Block 8 | | | | | | | | | Set Y address of Display block 8 |
| | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | * | Line Number of Block 8 | | | | | | | Set the line number of Display block 8 |
| | | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | * | | | | | | | 0<br>1 | Variable RAM Mapping Mode<br>D0=0:ON D0=1:OFF |

| Instruction | | Code | | | | | | | | | | | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A0 | $\overline{RD}$ | $\overline{WR}$ | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| (14) | Select Gray Scale Level | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | PWM Data (Frame No.1) | | | | PWM Data (Frame No.2) | | | | Gray Scale Level 0:Set the PWM Data of Frame No.1 and No.2 |
| | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | PWM Data (Frame No.3) | | | | PWM Data (Frame No.4) | | | | Gray Scale Level 0:Set the PWM Data of Frame No.3 and No.4 |
| | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | PWM Data (Frame No.1) | | | | PWM Data (Frame No.2) | | | | Gray Scale Level 1:Set the PWM Data of Frame No.1 and No.2 |
| | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | PWM Data (Frame No.3) | | | | PWM Data (Frame No.4) | | | | Gray Scale Level 1:Set the PWM Data of Frame No.3 and No.4 |
| | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | PWM Data (Frame No.1) | | | | PWM Data (Frame No.2) | | | | Gray Scale Level 2:Set the PWM Data of Frame No.1 and No.2 |
| | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | PWM Data (Frame No.3) | | | | PWM Data (Frame No.4) | | | | Gray Scale Level 2:Set the PWM Data of Frame No.3 and No.4 |
| | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | PWM Data (Frame No.1) | | | | PWM Data (Frame No.2) | | | | Gray Scale Level 3:Set the PWM Data of Frame No.1 and No.2 |
| | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | PWM Data (Frame No.3) | | | | PWM Data (Frame No.4) | | | | Gray Scale Level 3:Set the PWM Data of Frame No.3 and No.4 |
| (15) | Bias Select | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | * | | | | Bias | | | | Select Bias (11 types) |
| (16) | Voltage Converter Multiple Select | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | * | | | | | Boost Multiple | | | Set the Boost Multiple :2 to 7 times |
| (17) | Read Modify Write /End | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | * | | | | | | | 0<br>1 | Increase X Address Counter +1 when writing but no-change when reading<br>D0=0:ON D0=1:END |
| (18) | Reset | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | * | | | | | | | 1 | Initialize the internal circuits |
| (19) | Internal Power Supply | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | * | | | | | DC | VR | VF | DC=1:Voltage converter ON<br>DC=0:Voltage converter OFF<br>VR=1:Voltage Regurator ON<br>VR=0:Voltage Regurator OFF<br>VF=1:Voltage Follower ON<br>VF=0:Voltage Follower OFF |
| (20) | Driver Outputs ON/OFF | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | * | | | | | | | 0<br>1 | Set LCD driver outputs after the inter-nal(external) power supply ON<br>D0=0:Driver Outouts OFF<br>D0=1:Driver Outputs ON |
| (21) | Powehr Save (dual command) | 0<br>0 | 1<br>1 | 0<br>0 | 0<br>0 | 0<br>0 | 0<br>0 | 0<br>0 | 0<br>0 | 0<br>0 | 0<br>1 | 0<br>0 | * | | | | | | | 0<br>1 | Set the Power Save mode<br>(Reverse input sequence is possible) |
| (22) | ADC Select | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | * | | | | | | | 0<br>1 | Output the Disp. RAM address Sn<br>D0=0:Normal D0=1:Reverse |
| (23) | Display Mode Select | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | * | | | | | GS | L1 | L0 | Set Display mode<br>GB=1:Gray scale mode<br>GB=0:Black and white mode<br>L1=1:Select layer 1<br>L1=0:Not select layer 1<br>L0=1:select layer 0<br>L0=0:Not select layer 0 |
| (24) | 8-bit/16-bit Bus Select | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0<br>1 | * | | | | | | | | D8=0:Set 8-bit interface bus<br>D8=1:Set 16-bit interface bus |

( * : Don't care)

(3)Explanation of Instruction Code

3-1)Display ON/OFF

This instruction executes whole display ON/OFF without relationship of the data in the Display Data RAM and internal conditions.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | * | * | * | D |

* : Don't Care

D=0:Display OFF

D=1:Display ON

3-2)Z Address Set

This instruction sets the line address of Display Data RAM which correspond to COM0 terminal (Normally, it means the most upper line of the display ). The display area is only the number of lines which is equivalent to display duty in the increasing direction from the line address is automatically.

At that time, the data of Display Data RAM isn't changed at all. When the RAM mapping is set to Variable RAM Mapping Mode, the status of Variable RAM Mapping takes priority over this instruction. Therefore, the status of this Z Address Set instruction will be unavailable.

(R/W)

| A0 | $\overline{RD}$ | $\overline{WR}$ | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

R/W

| A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | Z Address (HEX) |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | | : | | | | | : |
| | | | | : | | | | | : |
| | | | | : | | | | | : |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 13E |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 13F |

3-3)X Address Set

In the case of access to the Display Data RAM from MPU side, it is needed that to set the X Address which correspond to Column Address by using of this X Address Set instruction, before data writing. The access to the Display Data RAM is possible by set of both X Address and Y Address. There is no influence to the Display with changing the Y Address.

The area of X Address is depended on the Display mode. In gray scale mode, it is from 00H to 10H. In black and white mode, it is from 00H to 08H(layer 0), and from 20H to 28H(layer 1). When Address is set unlike listed above, the Address will be invalid.

When MPU accesses to the Display Data RAM continuously, X Address is increased +1 from initial X Address every time RAM is accessed. Therefore, the MPU can access the only Data continuously without resetting of X Address.

The increment of X Address is stopped automatically at the point of the maximum value of X Address which is due to each mode +1.

At that time, Y Address isn't changed at all.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | * | * | A5 | A4 | A3 | A2 | A1 | A0 |

* : Don't Care

<table>
<tr><th rowspan="2">A5 A4 A3 A2 A1 A0</th><th colspan="3">X Address</th></tr>
<tr><th>Gray Scale Mode</th><th colspan="2">Black & White Mode</th></tr>
<tr><td rowspan="3">0 0 0 0 0 0<br>0 0 0 0 0 1<br>0 0 0 0 1 0<br>:<br>:<br>0 0 1 0 0 0<br>:<br>:<br>0 0 1 1 1 0<br>0 0 1 1 1 1<br>0 1 0 0 0 0<br>:<br>:<br>:<br>:<br>1 0 0 0 0 0<br>1 0 0 0 0 1<br>:<br>:<br>1 0 0 1 1 1<br>1 0 1 0 0 0<br>:<br>:<br>:</td><td rowspan="2">0<br>1<br>2<br>:<br>:<br>:<br>14<br>15<br>16</td><td>Layer 0</td><td>0<br>1<br>2<br>:<br>:<br>:<br>8</td></tr>
<tr><td colspan="2">Address Set is Invalid</td></tr>
<tr><td>Address Set is Invalid</td><td>Layer 1</td><td>32<br>33<br>:<br>:<br>39<br>40</td></tr>
<tr><td></td><td colspan="2">Address Set is Invalid</td></tr>
</table>

3-4)Y Address Set

In case of access to the Display Data RAM from MPU side, it is needed that to set the Low Address by using of this Y Address Set instruction, in addition to the using of 3-3) the X Address Set instruction is already described, before data writing.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

| A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | Y Address(HEX) |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | | | | : | | | | | : |
| | | | | : | | | | | : |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 13E |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 13F |

7-5)Status Read

This instruction reads out the intenal status of "BUSY", "ADC", "ON/OFF", "RESET", "GB" and "LY" are described below. When the extenal bus is set to 8-bit mode, this Status Read instruction will finish in 1 cycle.

___ (R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | BUSY | ADC | ON/ OFF | RESET | GB | LY1 | LY0 | 0 | BUSY | ADC | ON/ OFF | RESET | GB | LY1 | LY0 | 0 |

BUSY :BUSY=1 indicates the operationg or the Reset cycle.
This instruction can be input after the BUSY status change to “0”.

ADC :Indidates the output correspondence of X Address(Segment Address) and Segment Driver.
0:Counterclockwise output (Inverse)
1:Clockwise output (Normal)
(Note)The data “0=Inverse” and “1=Normal” of ADC is inverted with the ADC Select instruction of “1=Inverse” and “0=Normal”.

ON/OFF :Indicates the whole display ON/OFF status.
0:Whole Display “ON”
1:Whole Display “OFF”
(Note)The data “0=ON” and “1=OFF” of Display ON/OFF status read out is inverted with the Display ON/OFF instruction data of “1=ON” and ”0=OFF”.

RESET :Indicates the initializing period by RES signal or Reset instruction.
0:Without Reset status
1:In the Reset status

GB :Indicates the current Display Mode.
0:Black & White Mode
1:Gray Scale Mode

LY1 :Indicates the status of Layer 1 when the Display Mode is set to Black & White Mode.
0:Layer 1 isn’t selected
1:Layer 1 is selected

LY0 :Indicates the status of Layer 0 when the Display Mode is set to Black & White Mode.
0:Layer 0 isn’t selected
1:Layer 0 is selected

3-6)Write Display Data

This instruction writes the data on the data bus into the Display Data RAM. The X Address increases automatically after data writing, therefore, the MPU can write the data into the Display Data RAM continuously without any address setting after the start address setting.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

D15-D0:Write Data

3-7)Read Display Data

This instruction reads out the 16-bit data ftom Display Data RAM which addressed by the X Assress and Y Address. The X Address increase “+1” automaticaly after 16-bit data reading out, therefore, the MPU can read out the 16-bit data ftom Display Data RAM continuously without any address setting after the atart address setting. The one time of dummy read must operate after X Address set as the explanation in “(5-4) Access to the Display Data RAM and internal Resister”. In the serial interface mode, the display data is not read out.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

D15-D0:Read Data

3-8)Normal or Inverse ON/OFF Set

This instruction changes the condition of display turn ON and OFF as normal or inverse. The contents of Display Data RAM is not changed by this instruction exection.

(R/W)

| A0 | $\overline{RD}$ | $\overline{WR}$ | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | * | * | * | * | * | * | D |

*:Don’t Care

Black & White Mode:

| D | RAM=”1” | RAM=”0” |
|---|---|---|
| 0(Normal) | LCD ON | LCD OFF |
| 1(Inverse) | LCD OFF | LCD ON |

Gray Scale Mode:

| D | RAM=”00” | RAM=”01” | RAM=”10” | RAM=”11” |
|---|---|---|---|---|
| 0(Normal) | Gray Scale Level 0 | Gray Scale Level 1 | Gray Scale Level 2 | Gray Scale Level 3 |
| 1(Inverse) | Gray Scale Level 3 | Gray Scale Level 2 | Gray Scale Level 1 | Gray Scale Level 0 |

3-9)Static Drive ON/OFF

This instruction turns ON the all pixels independent of the contents of the Display Data RAM. At this time, the contents of Display Data RAM is not changed and kept. This instruction takes precedence over the “Normal or Inverse ON/OFF Set” Instruction.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | * | * | * | * | * | * | * | D |

* : Don’t Care

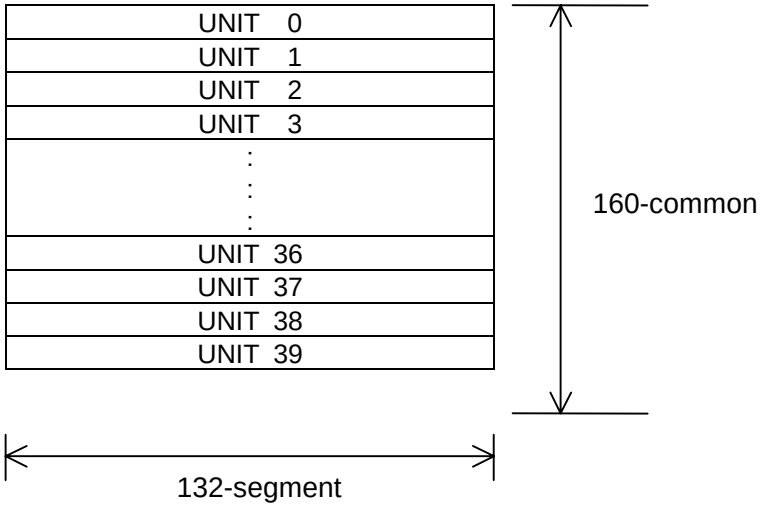
D=0:Normal Display
D=1:Whole Displplay Turns ON

If this Static Drive ON/OFF instruction is executed when Display OFF status, the NJU6682 will be in Power Save Mode. The details about this Power Save Mode is descrived in it’s own section.

3-10)Partial Display

This instrcution devides display area into 40 unit with 4-common each, then display these required area which is selected. Therefore, the duty will be low automatically, so that LCD driving voltage will be low. So, it is suitable when low operating power is requied.

•Display Unit Construction




When executing the Partial Display function, at first, it must be defined both the Top Unit Number of display area (the Start Unit) and the number of the effective unit start from the Start Unit. And it is possible to set these definition as two blocks. If setting the Start Unit of the 1st Block as “0” (0,0,0,0), and then if setting the Display Unit Number as “40” (1,0,1,0,0,0), it means that to define the all unit of the Display, it becomes that all Display ON (1/160 Duty), and the definition of the 2nd Block will be invalid. And when Partial Display instruction is executed, the duty is changed to optimum condition automaticaly, but LCD Driving Voltage and Bias Voltage aren’t changed at all. Therefore, before execution of Partial Display instruction, “Driver Output OFF” instruction must be done, then execute the instruction Bias Set, Voltage Converter Multiple Select, and EVR Resister Set to reset each status with execution of this Partial Display instruction.

(Notes)
- •The Start Unit of the 1st Block must be less than the Start Unit of the 2nd Block.
- •Don’t overlap the 1st Block and the 2nd Block.
- •The Start Unit of the 1st Block must not be more than 39.
- •The all Display Unit Number (the sum of the 1st Block Unit Number and the 2nd Block Unit Number) must not be more than 39.
- •According to a setting, the area is made from the 1st Block to the 2nd Block may be empty, but the Y Address of the Display RAM is continuous.

(1)Set the Start Unit of the 1st Block

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | * | * | D5 | D4 | D3 | D2 | D1 | D0 |

(2)Set the Display Unit Number of the 1st Block

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | * | * | D5 | D4 | D3 | D2 | D1 | D0 |

(3)Set the Start Unit of the 2nd Block

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | * | * | D5 | D4 | D3 | D2 | D1 | D0 |

(4)Set the Display Unit Number of the 2nd Block

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | * | * | D5 | D4 | D3 | D2 | D1 | D0 |

* : Don't Care

D5 to D0 : The Start Unit, or the Display Unit Number

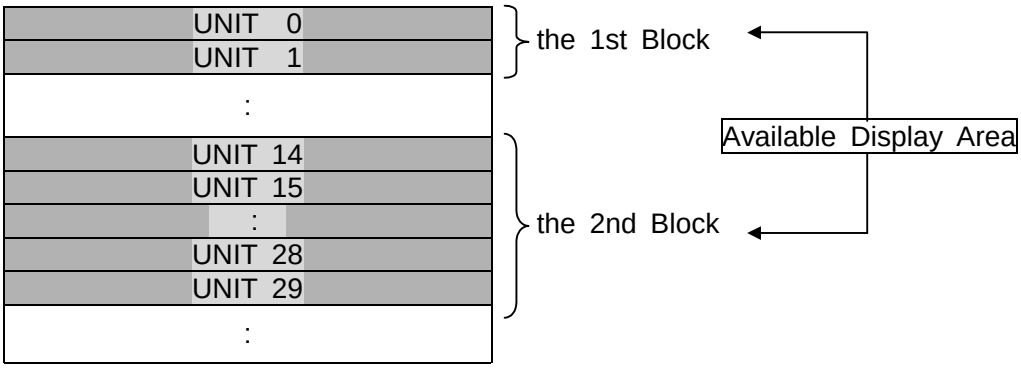
Finally, by execution of the command below, it will be changed into the status of the Display have already been defined, and it will be changed into the optimum Duty Ratio.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | * | * | * | * | * | * | * | 0 |

* : Don't Care

The example and the method of Partial Display are listed below.




(1)Set the Start Unit of the 1st Block “0”.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

(2)Set the Display Unit Number of the 1st Block “2”.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

(3)Set the Start Unit of the 2nd Block “14”.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |

(4)Set the Display Unit Number of the 2nd Block “16”.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

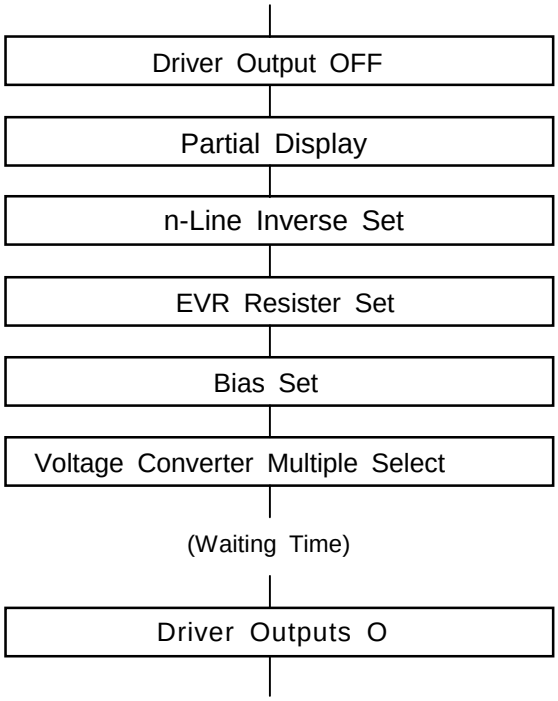
Then, the Duty will be changed to 1/128 automatically.

(4)Execute the Partial Display

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The Sequence about the Partial Display function




3-11)n-Line Inverse Resister Set
This instruction drives the Display with inverse mode at the specified line.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | * | * | A5 | A4 | A3 | A2 | A1 | A0 |

* : Don't Care

| A5 | A4 | A3 | A2 | A1 | A0 | Inverse Line |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | - |
| 0 | 0 | 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 0 | 0 | 1 | 0 | 3 |
| | | | : | | | : |
| | | | : | | | : |
| 1 | 1 | 1 | 1 | 1 | 0 | 63 |
| 1 | 1 | 1 | 1 | 1 | 1 | 64 |

✶When A5 to A0 are "000000", it will be 2-frame alternating drive mode.

3-12)EVR Resister Set

This instruction controls Voltage Adjustment Circuit of internal LCD power supply and changes LCD driving voltage “V5”. Finally, it adjusts the contrast of LCD display. By setting a data into EVR resister, V5 output voltage selects one condition out of 201-voltage conditions. The range of V5 voltage is adjusted by setting external resister as mentioned in (4-2) Voltage Regulator

| | (R/W) | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A0 | $\overline{RD}$ | $\overline{WR}$ | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | VLCD |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | Low |
| | | | | : | | | | : |
| | | | | : | | | | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | : |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | High |

VLCD=VDD-V5

If EVR isn’t used, set the EVR Resister to (1,1,1,1,1,1,1,1).

3-13)Variable RAM Mapping Mode

At this Variable RAM Mapping Mode, it is possible to define the RAM area in a maximum of 8-blocks not to continue to display the screen. Therefore, it is easy to replace a part of the Display Data each other(Fig.7, 8).

When using this Variable RAM Mapping Mode, the Z Address is defined by “3-2)Z Address Set instruction” will be invalid. So, Vertical Scroll with changing a Z Address will be unable.

And, it is available to define the Display Line Number of each blocks as “1” to “63”, but it must not define as “0”.

If setting the all Display Line Number more than the Duty, the line data which is over the Duty will not be displaied.

After Reset is executed, the resister about this Variable RAM Mapping Mode will be indefinite.

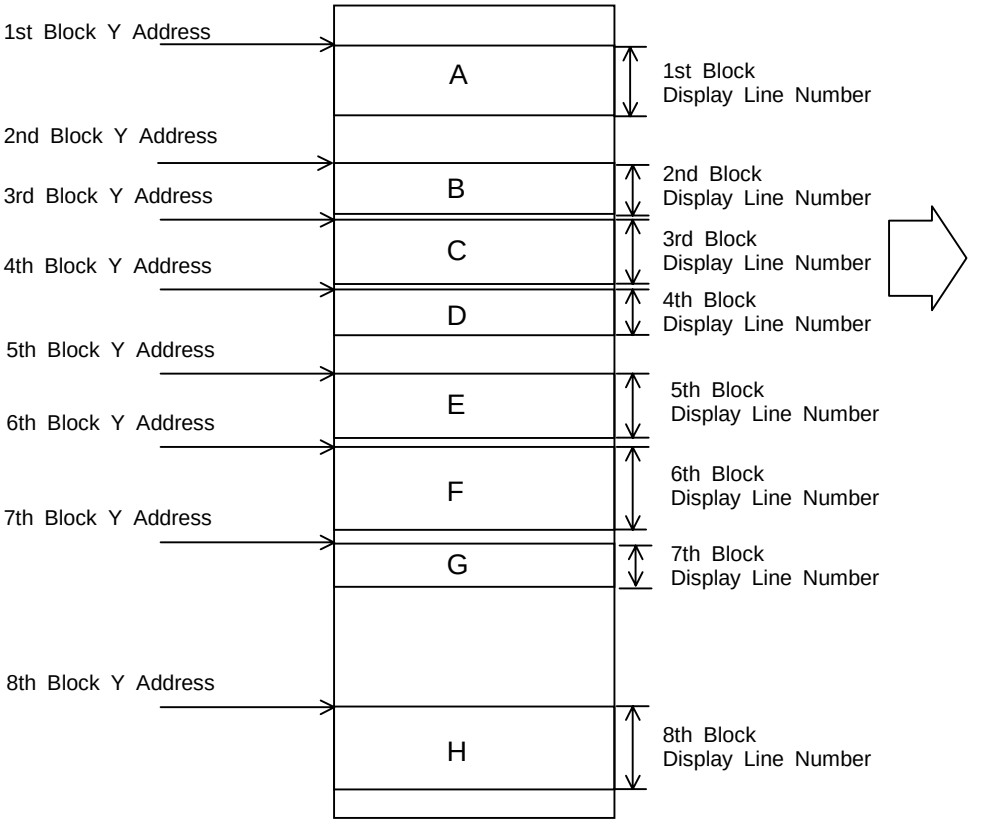



Fig.7-1 The setup of Variable RAM Mapping Mode, and the Address Map

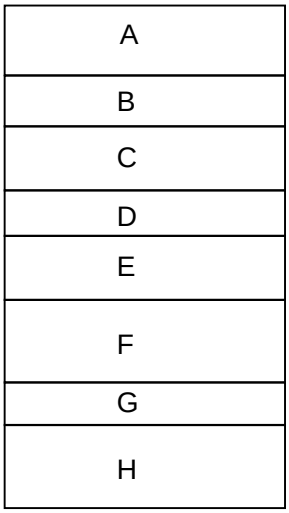



Fig.7-2 The actual view of the Display

The Example of Variable RAM Mapping Mode

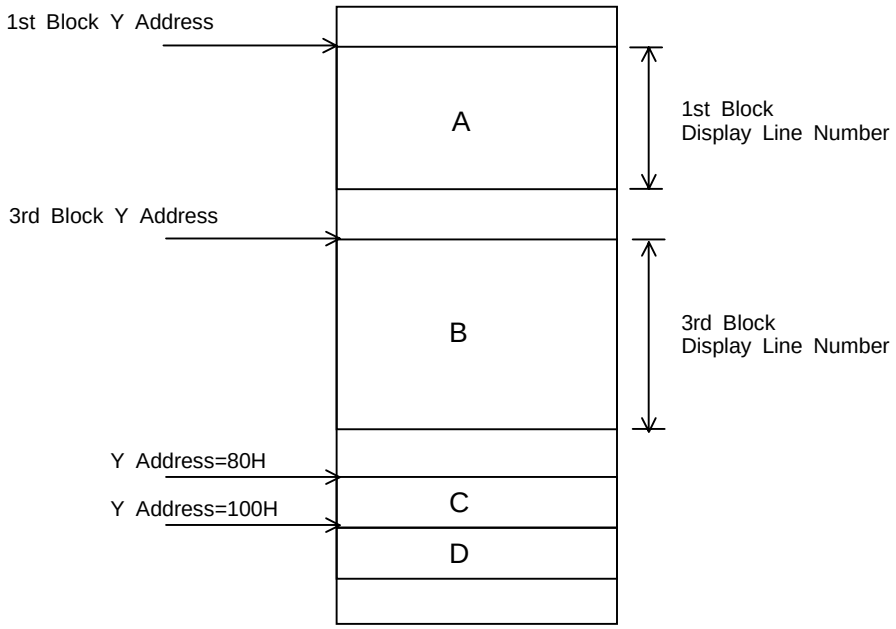



Fig.8-1 The setup of Variable RAM Mapping Mode, and the Address Map

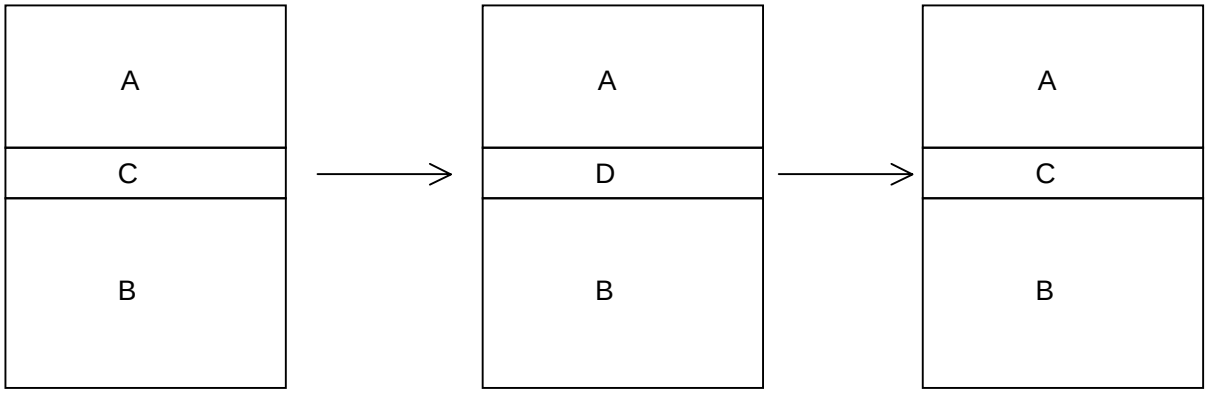



Fig.8-2 The actual Views of the Display when the 2nd Block Y-Address is changed like the sequence of “80”H -> “100”H -> “80”H

(1)Set the Y Address of the 1st Block

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

A8 to A0:the Y Address of the 1st Block (0 to 319)

(2)Set the Display Line Number of the 1st Block

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | * | * | D5 | D4 | D3 | D2 | D1 | D0 |

* : Don't Care

D5 to D0:the Display Line Number of the 1st Block (1 to 63)

(3)Set the Y Address of the 2nd Block

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

A8 to A0:the Y Address of the 2nd Block (0 to 319)

(4)Set the Display Line Number of the 2nd Block

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | * | * | D5 | D4 | D3 | D2 | D1 | D0 |

* : Don't Care

D5 to D0:the Display Line Number of the 2nd Block (1 to 63)

(5)Set the Y Address of the 3rd Block

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

A8 to A0:the Y Address of the 3rd Block (0 to 319)

(6)Set the Display Line Number of the 3rd Block

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | * | * | D5 | D4 | D3 | D2 | D1 | D0 |

* : Don't Care

D5 to D0:the Display Line Number of the 3rd Block (1 to 63)

(7)Set the Y Address of the 4th Block

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

A8 to A0:the Y Address of the 4th Block (0 to 319)

(8)Set the Display Line Number of the 4th Block

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | * | * | D5 | D4 | D3 | D2 | D1 | D0 |

* : Don't Care

D5 to D0:the Display Line Number of the 4th Block (1 to 63)

(9)Set the Y Address of the 5th Block

| | (R/W) | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

A8 to A0:the Y Address of the 5th Block (0 to 319)

(10)Set the Display Line Number of the 5th Block

| | (R/W) | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | * | * | D5 | D4 | D3 | D2 | D1 | D0 |

* : Don't Care

D5 to D0:the Display Line Number of the 5th Block (1 to 63)

(11)Set the Y Address of the 6th Block

| | (R/W) | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

A8 to A0:the Y Address of the 6th Block (0 to 319)

(12)Set the Display Line Number of the 6th Block

| | (R/W) | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | * | * | D5 | D4 | D3 | D2 | D1 | D0 |

* : Don't Care

D5 to D0:the Display Line Number of the 6th Block (1 to 63)

(13)Set the Y Address of the 7th Block

| | (R/W) | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

A8 to A0:the Y Address of the 7th Block (0 to 319)

(14)Set the Display Line Number of the 7th Block

| | (R/W) | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | * | * | D5 | D4 | D3 | D2 | D1 | D0 |

* : Don't Care

D5 to D0:the Display Line Number of the 7th Block (1 to 63)

(15)Set the Y Address of the 8th Block

| | (R/W) | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

A8 to A0:the Y Address of the 8th Block (0 to 319)

(16)Set the Display Line Number of the 8th Block

| | (R/W) | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | * | * | D5 | D4 | D3 | D2 | D1 | D0 |

* : Don't Care

D5 to D0:the Display Line Number of the 8th Block (1 to 63)

By using of the following instruction, Variable RAM Mapping Mode will be executed.

| A0 | RD (R/W) | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | * | * | * | 1 |

* : Don't Care

And, by using of the following instruction, it will go back to the normal status from Variable RAM Mapping Mode.

| A0 | RD (R/W) | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | * | * | * | 0 |

* : Don't Care

3-14)Gray Scale Level Select

This instruction sets the level of 4-gray scale. The setting of each gray scale level is executed by writing the PWM data (0 to $F_H$) to the 4-Resisters of the 4-Flames consists of 1st to 4th.

And, among the 4-gray scale levels, the level 0 corresponds to the data (0,0) of the Display Data RAM, the level 1 is the data (0,1), the level 2 is the data (1,0), and the level 3 is the data (1,1).

Just after Reset, a Resister is related to the Gray Scale Level Select will be initialized like a following table.

| PWM Data | HEX | Gray Scale Level |
|---|---|---|
| 0 | 0 | 0/15(initialized value of level 0) |
| 1 | 1 | 1/15 |
| 2 | 2 | 2/15 |
| 3 | 3 | 3/15 |
| 4 | 4 | 4/15 |
| 5 | 5 | 5/15(initialized value of level 1) |
| 6 | 6 | 6/15 |
| 7 | 7 | 7/15 |
| 8 | 8 | 8/15 |
| 9 | 9 | 9/15 |
| 10 | A | 10/15(initialized value of level 2) |
| 11 | B | 11/15 |
| 12 | C | 12/15 |
| 13 | D | 13/15 |
| 14 | E | 14/15 |
| 15 | F | 15/15(initialized value of level 3) |

(1)Set the PWM Data of both the 1st Frame and the 2nd Frame with the Gray Scale Level 0.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | D13 | D12 | D11 | D10 | D23 | D22 | D21 | D20 |

D13 to D10 : the PWM Data of the 1st Frame
D23 to D20 : the PWM Data of the 2nd Frame

(2)Set the PWM Data of both the 3rd Frame and the 4th Frame with the Gray Scale Level 0.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | D33 | D32 | D31 | D30 | D43 | D42 | D41 | D40 |

D33 to D30 : the PWM Data of the 3rd Frame
D43 to D40 : the PWM Data of the 4th Frame

(3)Set the PWM Data of both the 1st Frame and the 2nd Frame with the Gray Scale Level 1.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | D13 | D12 | D11 | D10 | D23 | D22 | D21 | D20 |

D13 to D10 : the PWM Data of the 1st Frame
D23 to D20 : the PWM Data of the 2nd Frame

(4)Set the PWM Data of both the 3rd Frame and the 4th Frame with the Gray Scale Level 1.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | D33 | D32 | D31 | D30 | D43 | D42 | D41 | D40 |

D33 to D30 : the PWM Data of the 3rd Frame
D43 to D40 : the PWM Data of the 4th Frame

(5)Set the PWM Data of both the 1st Frame and the 2nd Frame with the Gray Scale Level 2.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | D13 | D12 | D11 | D10 | D23 | D22 | D21 | D20 |

D13 to D10 : the PWM Data of the 1st Frame
D23 to D20 : the PWM Data of the 2nd Frame

(6)Set the PWM Data of both the 3rd Frame and the 4th Frame with the Gray Scale Level 2.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | D33 | D32 | D31 | D30 | D43 | D42 | D41 | D40 |

D33 to D30 : the PWM Data of the 3rd Frame
D43 to D40 : the PWM Data of the 4th Frame

(7)Set the PWM Data of both the 1st Frame and the 2nd Frame with the Gray Scale Level 3.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | D13 | D12 | D11 | D10 | D23 | D22 | D21 | D20 |

D13 to D10 : the PWM Data of the 1st Frame
D23 to D20 : the PWM Data of the 2nd Frame

(8)Set the PWM Data of both the 3rd Frame and the 4th Frame with the Gray Scale Level 3.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | D33 | D32 | D31 | D30 | D43 | D42 | D41 | D40 |

D33 to D30 : the PWM Data of the 3rd Frame
D43 to D40 : the PWM Data of the 4th Frame

3-15)Bias Select

This instruction sets the Bias Voltage. And it must be done with the setting of the Partial Display Mode.

(R/W)

| A0 | $\overline{RD}$ | $\overline{WR}$ | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | * | * | * | * | A3 | A2 | A1 | A0 |

* : Don't Care

| A3 | A2 | A1 | A0 | Bias |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1/4 |
| 0 | 0 | 0 | 1 | 1/5 |
| 0 | 0 | 1 | 0 | 1/6 |
| 0 | 0 | 1 | 1 | 1/7 |
| 0 | 1 | 0 | 0 | 1/8 |
| 0 | 1 | 0 | 1 | 1/9 |
| 0 | 1 | 1 | 0 | 1/10 |
| 0 | 1 | 1 | 1 | 1/11 |
| 1 | 0 | 0 | 0 | 1/12 |
| 1 | 0 | 0 | 1 | 1/13 |
| 1 | * | 1 | * | 1/14 |

*: Don't Care

3-16)Voltage Converter Multiple Select

This instruction sets the boost level multiple of Internal Voltage Converter Circuits(2-times to 7-times). It must be done with the setting of the Partial Display Mode. If the external capasitor is connected as the boost level multiple is lower than 6-times, don't select the multiple with this instruction over its multiple is owing to its connection of the external capacitor. There is a fear of an incorrect function.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | * | * | * | * | * | A2 | A1 | A0 |

* : Don't Care

| A2 | A1 | A0 | Boost Multiple |
|---|---|---|---|
| 0 | 0 | 0 | 2-times |
| 0 | 0 | 1 | 3-times |
| 0 | 1 | 0 | 4-times |
| 0 | 1 | 1 | 5-times |
| 1 | 0 | 0 | 6-times |
| 1 | * | 1 | 7-times |

* : Don't Care

3-17)Read Modify Write

This instruction sets the Read Modify Write Mode for the page address increment control. In this mode, the X Address insreases "+1" automatically when the Display Data Write instruction is exexuted, but the X Address doesn't change when the Display Data Read Instruction is executed. This status is continued until the End instruction execution. When the End instruction is executed, the X Adddress goes back to the start address before the execution of this Read Modify Write instruction. This function reduces the load of MPU for repeating the display data change in the fixed area(ex. cursor blink).

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | * | * | * | * | * | * | * | D |

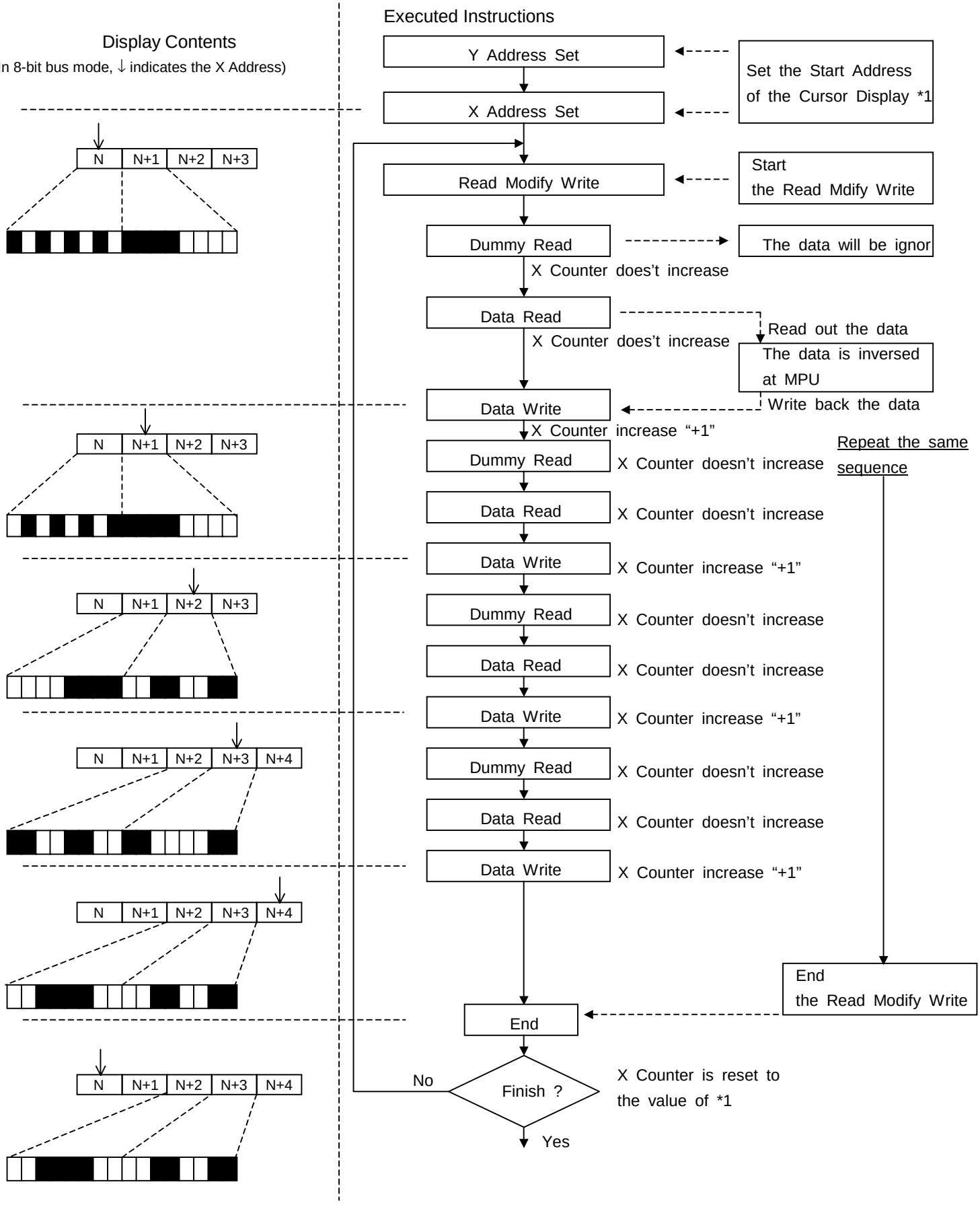
* : Don't Care

D=0:Read Modify Write ON

D=1:End

(Note)In mode of this Read Modify Write, any instructions except Y Address Set can execute.

The Example of Read Modify Write Sequence



3-18)Reset

This instruction executes the following initialization.

Initialization

1:Clear the Resister of the Selial Interface.
2:Set the X Address Counter (00)H.
3:Set the Y Address Resister (000)H.
4:Set the Z Address Counter (000)H
5:Normal RAM Address Mapping(Variable RAM Mapping Mode OFF).
6:Set the EVR Resister (FF)H.
7:Set the Duty “1/160”(All ON).
8:Set the Bias Select “1/14”.
9:Set the Voltage Boost Multiple “7-times”.
10:Set the n-Line Inverse Resister (0)H.
11:Set the Bus 8-bit Bus Mode.

(R/W)

| A0 | $\overline{RD}$ | $\overline{WR}$ | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | * | * | * | * | * | * | * | D |

* : Don’t Care

At this time, the Display Data RAM is not influenced.
The reset signal input to the RES terminal ( hardware reset ) must be input for the power on intialization.
Reset instruction does not perform completely instead of hardware reset using the RES terminal.

3-19)Internal Power Supply

This instruction set ON/OFF of Voltage Converter, Voltage Regulator and Voltage Follower. To operate the Voltage Converter, the oscillation circuits must be operating.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | * | * | * | * | * | DC | VR | VF |

* : Don’t Care

DC=1:Voltage Converter ON
DC=0:Voltage Converter OFF※1)
VR=1:Voltage Regulator ON
VR=0:Voltage Regulator OFF※2)
VF=1:Voltage Follower ON
VF=0:Voltage Follower OFF※3)

※1)At this time, terminals C1+,C1-,C2+,C2-,C3-,C4-,C5- and C6- should be open, and VOUT should be supplied from outside.
※2)At this time, terminal VR should be open, and V5 should be supplied from outside.
※3)At this time, terminals V1 to V5 should be supplied from outside.

※The time which is needed for complitely starting up of the Internal Power Supply is depending on each settings (Supply Voltage, VLCD=VDD-V5, External Capacitor of Voltage Converter, External Capacitor which is connected to V1 to V5). To know the time corretly, the test with actual LCD module must be needed.

3-20)Driver Outputs ON/OFF

This instruction controlls ON/OFF of the LCD Driver Outputs.

| | (R/W) | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A0 | $\overline{RD}$ | $\overline{WR}$ | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | * | * | * | * | * | * | * | D |

* : Don't Care

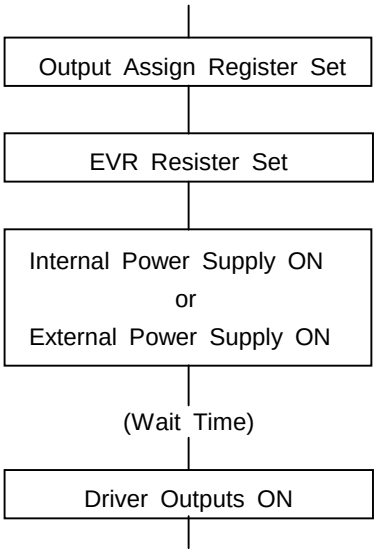
D=0:Driver Outputs OFF(No signal is output)
D=1:Driver Outputs ON(Signal is output)

The NJU6682 contains low power LCD driving voltage generator circuit reducing own operating current. Therefore, it requires the following sequence procedures at power on for power source stabilized operation.

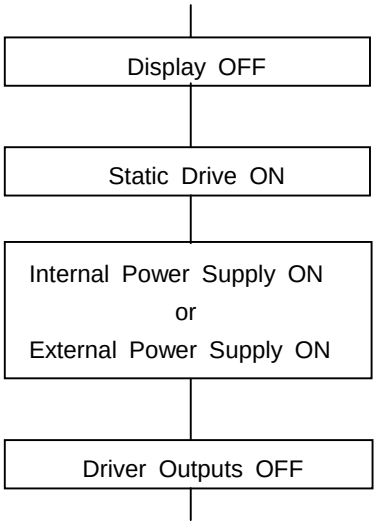
●LCD Driving Power Supply ON/OFF Sequences

The following sequences are required when the power supply is turned ON/OFF.
When the Power Supply is turned on again after the turn off (by the Power Save instruction), the power save release sequence(s) is required.

❍Turn ON Sequence




❍Turn OFF Sequence



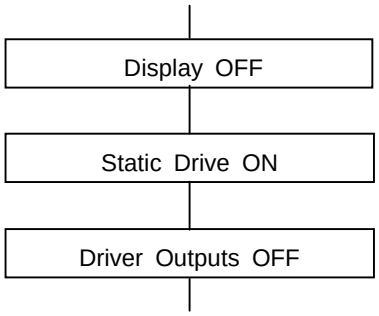
3-21)Power Save

When both of Display OFF and Static Drive ON are executed( its sequence is not required ), the internal circuits go to the Power Saving Mode and the operating current is reduced as same as the stand by current.
The internal status in this Power Save Mode is shown in follows;

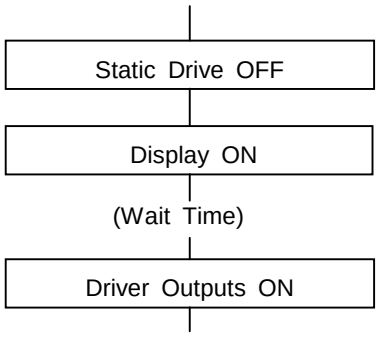
1:The operation of both the Oscillation Circuits and the Internal Power Supply Circuits is stopped.
2:LCD driving is stopped. Segment and Common drivers output Vdd level voltage.
3:Both the display data and the operating mode just before the Power Save Mode is kept.
4:All of the LCD driving bias voltage is fixed to the VDD level.

*1 In the Power Save sequence, the Power Save Mode is started after the second instruction (Static Drive ON).
*2 In the Power Save release sequence, the Power Save Mode is released after the Static Drive OFF instruction.The Display ON instruction can input at any timming after the Static Drive OFF instruction in Power Save release sequence.
*3 LCD driving signal isn't output until the xexection of the Driver Outputs ON instruction.
*4 In case of the external power supply for LCD driving, it should be turn off and made condition like as disconnection or connection to VDD before the Power Save Mode or at the same time. In this time, VOUT terminal should be made codition like as disconection or connection to the lowest voltage of the system.

❍Power Save Sequence




❍Power Save Release Sequence




❋NJU6682 spends the current regularly without the execution of the Driver Outputs OFF instruction. The LCD drive signal will not be output until the Driver Outputs ON instruction is done.

3-22)ADC Select

This instruction defines the correspondence of X Address of the display RAM with the Segment Driver Outputs.
By using of this instruction, it is possible to invert the sequence of the Segment Driver Output. Therefore, the limitation like a arrangement of IC with LCD module making will decrease.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | * | * | * | * | * | * | * | D |

* : Don't Care

D=0:Clockwise Output (Normal)
D=1:Counterclockwise Output (Inverting)

3-23)Display Mode Select
This instruction selects the Display Mode.

(R/W)S

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | * | * | * | * | * | GS | L1 | L0 |

* : Don't Care

GS=1:Gray Scale Mode
GS=0:Black & White Mode

❋When GS=0(Black & White Mode), the following L1 and L2 bit are valid.

L1=1:Select the Layer 1
L1=0:Not select the Layer 1
L0=1:Select the Layer 0
L0=0:Not select the Layer 0

3-24)8-bit/16-bit Bus Select
This instruction sets the interface bus as 8-bit or 16-bit.

(R/W)

| A0 | RD | WR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | D | * | * | * | * | * | * | * | * |

* : Don't Care

D=0:Select 8-bit interface bus (D7 to D0).
D=1:Select 16-bit interface bus (D15 to D0)

(4)Internal Power Supply

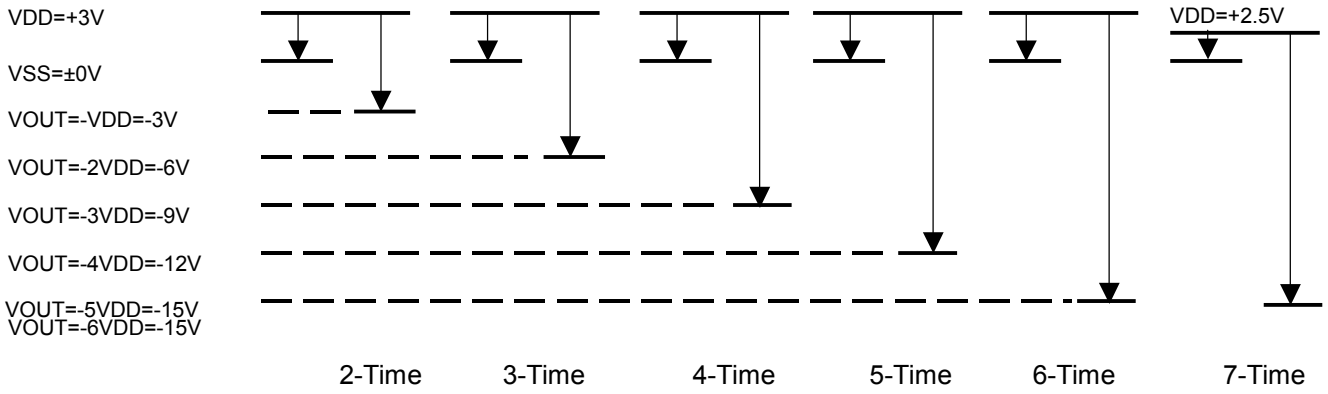
4-1)7-Time Voltage Booster circuits

7-time voltage booster circuit connecting seven capacitors between C1+, C1- and C2+, C2- and ,C3-,C4-, C5- and C6- ,VSS and VOUT boost the voltage of VDD-VSS to negative Voltage(VDD Common) and output the boosted voltage from VOUT terminal. It selects one of boost time from 2 to 7 times by external capacitors connection.Furthermore,it also selects one of boost time by “Voltage Booster circuits mulitiple select” instruction.The boost voltage and the voltage booster circuits are shown below.

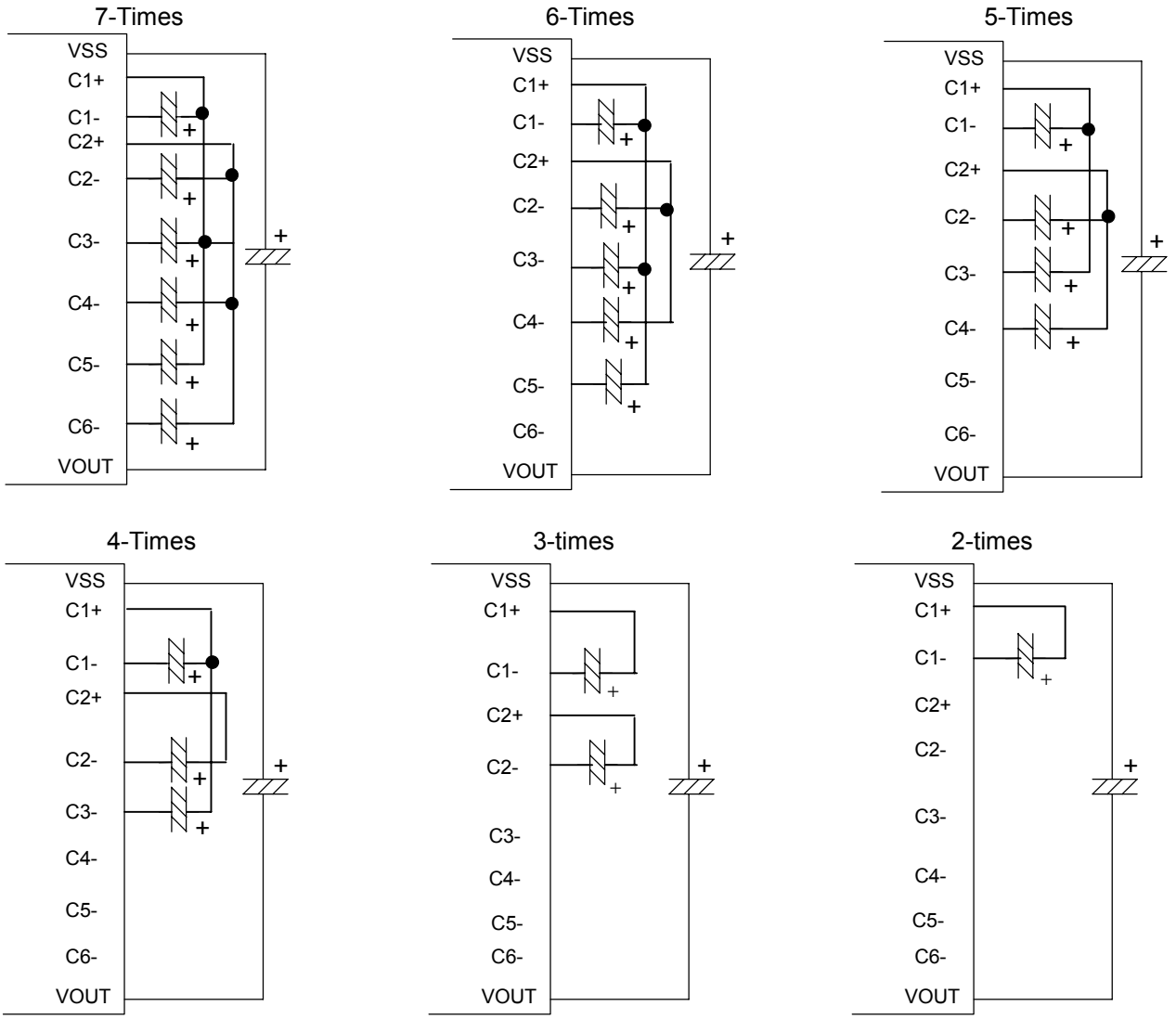
Voltage Booster circuits requires the clock signals from internal oscillation circuit,therefore ,the oscillation circuits must be operating when voltage boost operation. The boost voltage times are shown in below.

When 7 times boost operation,the operation voltage of VDD-VOUT should be less than 18V.

The relationship with Boosted voltage and VDD,VSS




Example of Capacitor connection in voltage Booster circuits



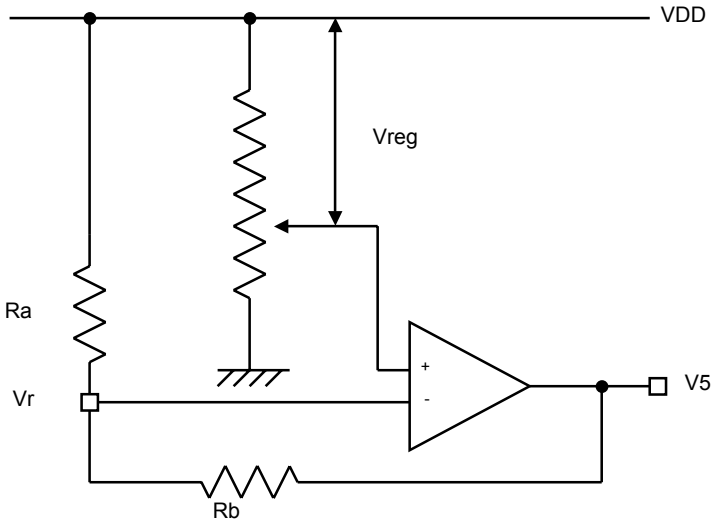
4-2)Voltage Adjust Circuit

The boosted voltage of VOUT output from V5 through the voltage adjust circuits for LCD driving. The output voltage of V5 is adjusted by changing the Ra+Rb within the range of |V5| < |VOUT|.
The output is calcurated by the following fomula(1).

$$VLCD=VDD-V5=(1+Rb/Ra)\bullet VREG \quad \text{----------(1)}$$

The voltage of VREG is a standard voltage produce from built-in bleeder registance.VREG is possibleto be fine-adjusted by EVR functions mentioned in(4-3).

For fine-adjustment of V5,R2 as variable resistor,R1 and R3 as fixed constant should be connectedto VDD terminal,VR and V5 ,as shown below.




< Design example for R1, R2 and R3 /Reference >

- R1+R2+R3=5MΩ
  (Determind by the current flown between VDD-V5)
- Variable voltage range by the R2. 6V to 7.5V (VLCD=VDD-V5)
  (Determind by the LCD electrical characteristics)
- VREG=3V
  (In case of VDD=3V)

R1,R2 and R3 are calculated by above conditions and the fomula of(1) to below;

R1=2.0MΩ
R2=0.5MΩ
R3=2.5MΩ

Note) If the power supply voltage between VDD and VSS changes,V5 changes too.therefore the power supply voltage should be stabilized for V5 stable operation.

4-3)Contrast adjustment by the EVR function

The EVR control voltage of VREG by instruction and changes voltage of V5.
AS result,LCD Display contrast is adjusted by V5.The EVR selects a voltage of VREG in the following 201 conditions by setting 8 bits data into the EVR register.
A step with EVR is set like table shown below.

| EVR register | VREG |
|---|---|
| (37)h | (100/300) x (VDD-VSS) |
| (38)h | (101/300) x (VDD-VSS) |
| (39)h | (102/300) x (VDD-VSS) |
| : | : |
| : | : |
| : | : |
| : | : |
| (FD)h | (298/300) x (VDD-VSS) |
| (FE)h | (299/300) x (VDD-VSS) |
| (FF)h | (300/300) x (VDD-VSS) |

When using an EVR function, the voltage adjustment circuit must be turn on by the power supply instruction.

●Adjustable range of the LCD driving voltage by EVR function
The adjustable range is decided by the power supply voltage VDD and the ratio of external resistors.

Example) NJU6682
Condition:VDD=3.0V
Ra=1MΩ, Rb=4MΩ (Ra:Rb=1:4)
The adjustable range and step voltage are calculated as follows in the above condition.
In case of setting 37(H) in the EVR register,

$$VLCD=(1+Rb/Ra) \times VREG$$
$$=(1+4) \times (100/300) \times 3.0$$
$$=5.0$$

In case of setting FF(H) in the EVR register,

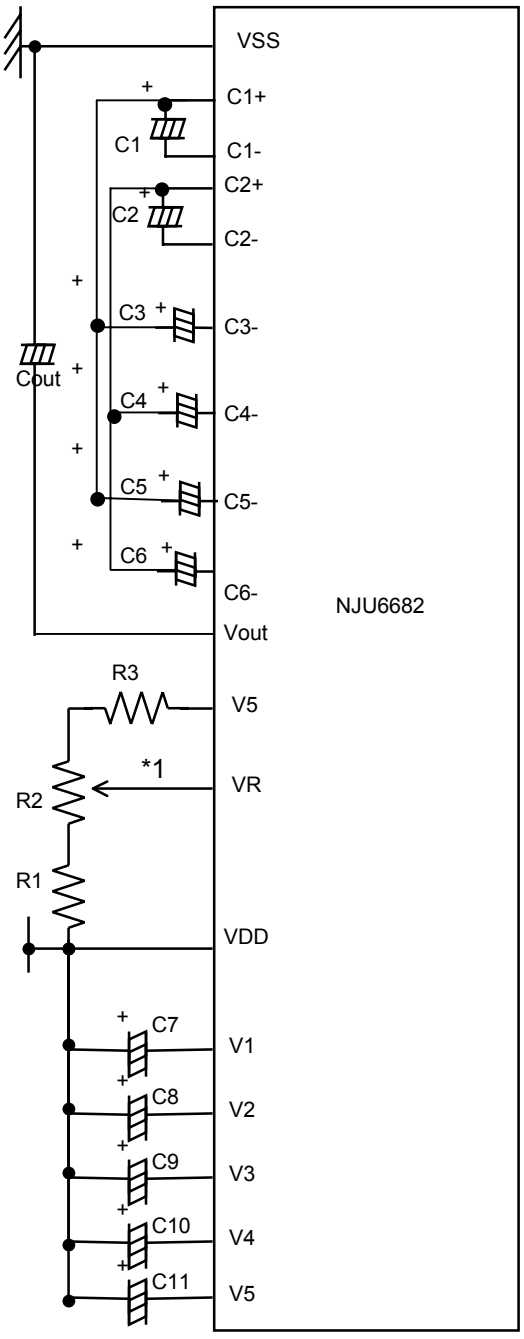
$$VLCD=(1+Rb/Ra) \times VREG$$
$$=(1+4) \times (300/300) \times 3.0$$
$$=15.0$$

4-4)LCD Driving Voltage Generation Circuit

The LCD driving bias voltage of V1,V2,V3,V4 are generated internally by dividing the V5 voltage with the internal bleeder resistance.And it is supplied to the LCD driving circuits after the impedence conversion with voltage follower circuit.

As shown Fig-3,Five capacitors are required to connect to each LCD driving voltage terminal for voltage atabilizing. And the value of C7 to C11 are determind depending on the actual LCD panel display evaluation.

In case of Internal Power Supply




In case of using External Power Supply

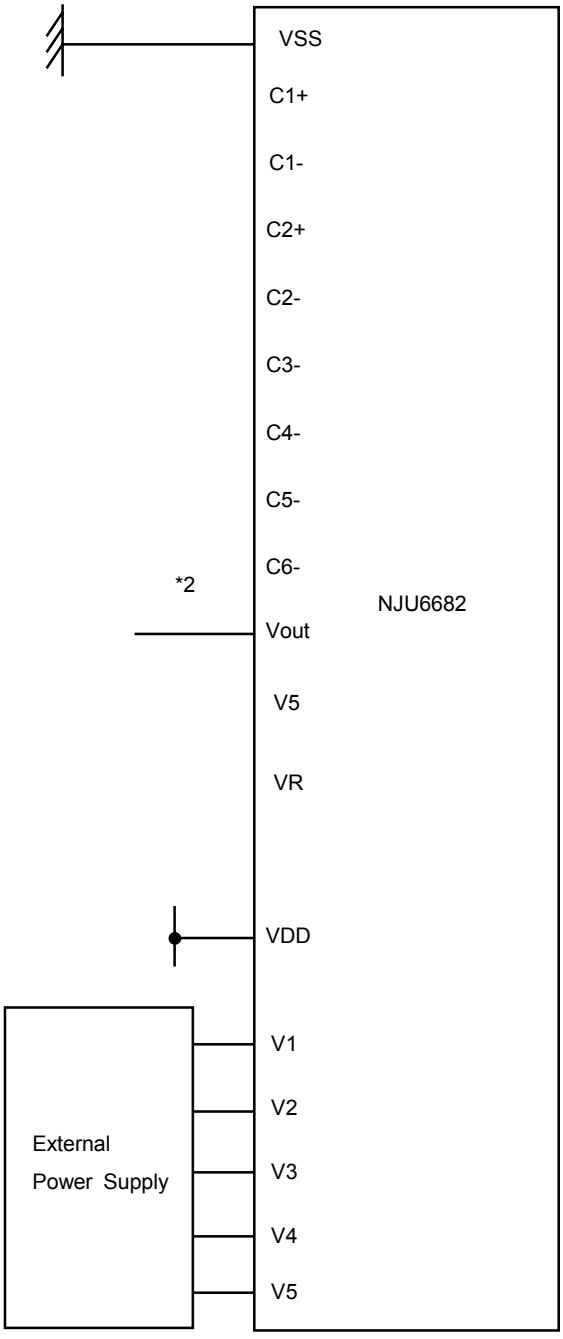



Fig-3

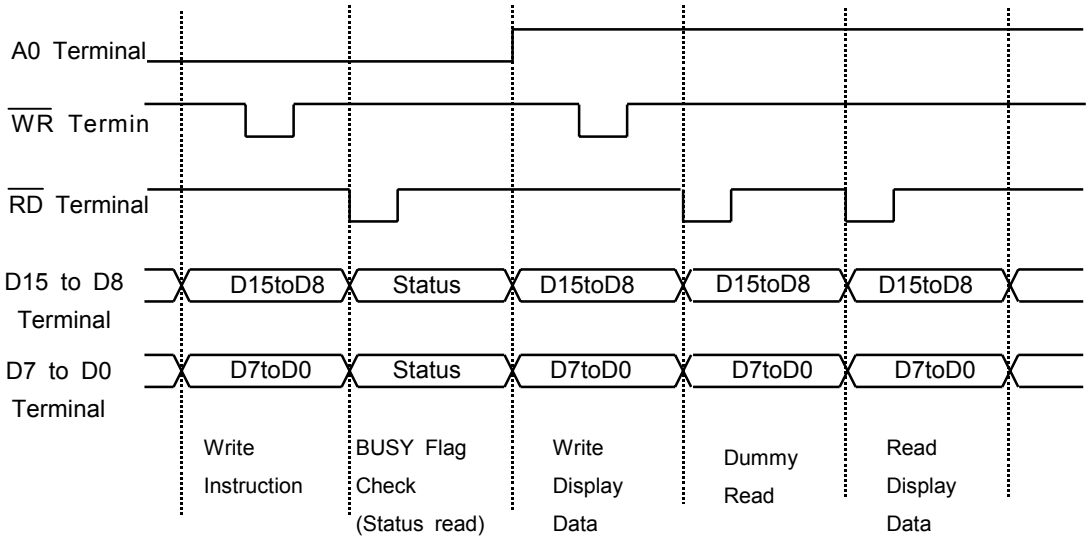
*1 Short wiring or sealed wiring to the VR terminal is required due to the high impedance of VR Terminal.

*2 Following connection of VOUT is required when external power supply using.
When VSS>V5 --- VOUT=V5
When VSS≤V5 --- VOUT=VSS

Reference set up value
VLCD=VDD-V5≅9.0 to 10.5V

| | |
|---|---|
| COUT | ~1.0uF |
| C1 to C6 | ~1.0uF |
| C7 to C11 | 0.1~0.47 uF |
| R1 | 2MΩ |
| R2 | 500KΩ |
| R3 | 2.5MΩ |

(b) Interface with 16 bit MPU (16 bit BUS Interface Mode)




5-3) Serial Data Input (PS1="L")

In the serial interface of NJU6682 consists 16-bit shift register and 4-bit counter, In case of chip select ($\overline{CS}$=L) means it becomes to input D7(SI) and D6(SCL), and in case of chip isn't select, a shift register and a counter are reset to the initial condition.

The data input from terminal(SI) is MSB first like as the order of D15, D14, •••D0 by a serial interface, it is entered into with rise edge of serial clock(SCL). The data converted into parallel data of 16-bit with the rise edge of 16th serial clock and processed.

The serial interface of NJU6682 can two way select to 3-wire type and 4-wire type by PS0 terminal. In choosen PS0 terminal to "H", it become 4-wire interface and discliminate display data, instructions by A0 input terminal. A0 is read with rise edge of (16 X n)th of serial clock (SCL), it is recognize display data by A0=H" and instruction by A0="L". A0 input is read in the rise edge of (16 X n)th of serial clock (SCL) after chip select and distinguished.

However,in case of $\overline{RES}$="L" or $\overline{CS}$="H" with trasfered data does not fill 16 bit, attention is necessary because it will processed as there was command input. Always, input the data of (16 X n) style. In choosen PS0 terminal to "L",it becomes 3-wire interface and discleminate data after the serial data of 16-bit as the A0 data.

Note) The SCL signal must be careful of the termination reflection by the wiring length and the external noise and confirmation by the actual machine is recommended by it.

(a) 4-wired Serial Interface

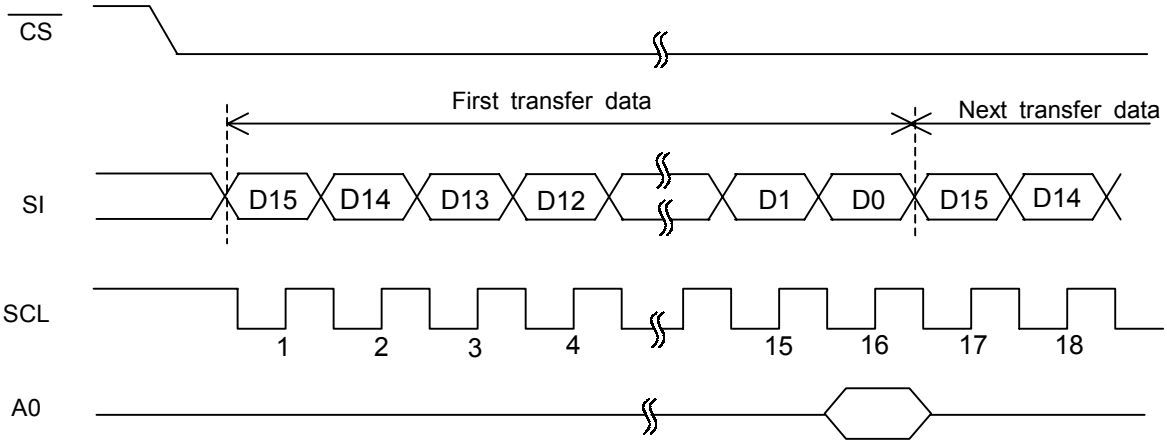



Fig 4-1

A0=”H”: Display Data
A0=”L”: Instruction

(b) 3-wire Serial Interface

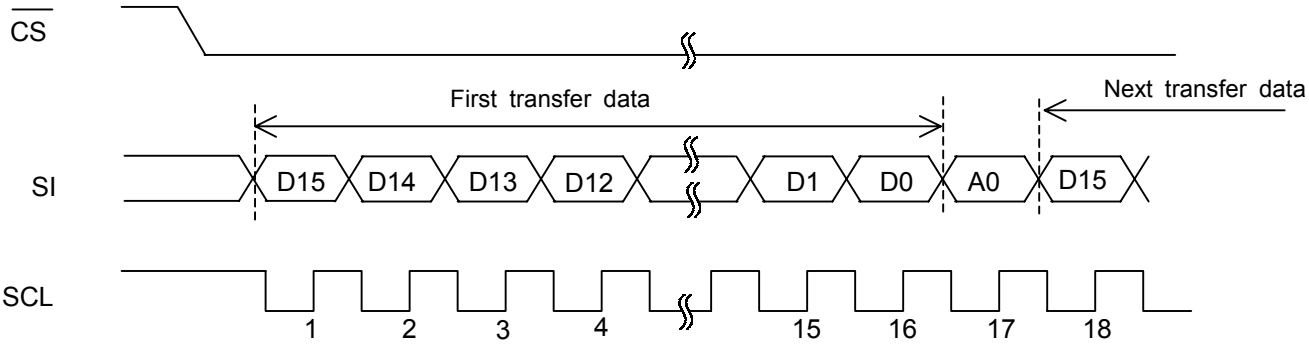



Fig 4-2

A0="1":Display Data
A0="0":Instruction

5-4)Display Data RAM , Access of Internal Register

NJU6682 communicates with the CPU through bus holder with the internal data BUS.

In case of reads the display data contents in Data RAM, the data which was read in the first data read cycle ( the dummy read ) is memorized in bus holder and is read on the system BUS from BUS holder in the following data read cycle. Also, In case of MPU writes into Display Data RAM, after once maintained by bus holder, it is written Into Display Data RAM by the following data write cycle.

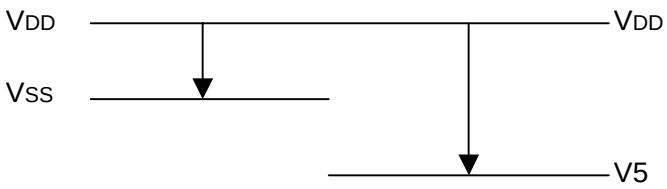
Therefore, the restrict in case of access by NJU6682 which was seen from MPU side is not access time (tACC,tDS) of Display Data RAM and the cycle time becomes dominant. With this, speed-up of the data transfer with the MPU becomes possible. In case of cycle time isn't met, the MPU inserts NOP operation and becomes equivalent to for this to execute wait operation on sutisfy condition.In MPU . But, there is an restricts in the read sequence of Display Data RAM.

When setting an address, the data of the specified address isn't output by the read operation immediately after setting an address and the data of the specification address is output at the the 2nd data read.

Therefore, the dummy read is always necessary once after address set and the write cycle.

■**ASOLUTE MAXIMUM RATING**

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|
| Supply Voltage(1) | | VDD | -0.3 to +5.0 | V |
| Supply Voltage(2) | | V5 , VOUT | VDD-20.0 to VDD+0.3 | V |
| Supply Voltage(3) | | V1,V2,V3,V4 | V5 to VDD+0.3 | V |
| Input Voltage | | $V_{IN}$ | -0.3 to VDD+0.3 | V |
| Operating Temperature | | $T_{OPR}$ | -30 to +80 | °C |
| Strage Temperature | TCP | $T_{STG}$ | -55 to +100 | °C |
| | Bare chip | | -55 to +125 | |




(Note 1) Voage values are specified as VSS=0.
(Note 2) Inase of using voltage boost circuit, as for the supply voltage, conditioned of 18.0V≥VDD-VOUT
(Note 3) The relation VDD≥V1≥V2≥V3≥V4≥V5;VDD>VSS≥VOUT must be maintained.
When inputting external LCD driving voltage , LCD drive voltage is simultaneous with the rise of $V_{DD}$ power supply or after rises VDD.
(Note 4) If the LSI are used on condition above the absolute maximum rating,the LSI may be destroyed.
Using LSI within electrical characteristics is strongly recommended for normal operation.
Use beyond the erectric characteristics conditions will cause malfunction and poor reliability.

(Note 5) Decoupling capacitor should be connected between VDD and VSS due to stabilized operation for the Voltage Converter.

■ELECTRICAL CHARACTERISTICS

(VDD=2.4 to 3.3V, VSS=0V, Ta=-30 to +80°C)

| PARAMETER | | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|---|
| Operating voltage(1) | | VDD | | | 2.4 | | 3.3 | V | 1 |
| Operating Voltage(2) | | V5 | | | VDD-18.0V | | VDD-6.0V | V | 2 |
| | | V1,V2 | VLCD=VDD-V5 | | VDD-0.5VLCD | | VDD | | |
| | | V3,V4 | | | V5 | | VDD - 0.5VLCD | | |
| Input Voltage | High Level | VIHC1 | A0,D0-D15,$\overline{RD}$,$\overline{WR}$,$\overline{RES}$,$\overline{CS}$ Exclude P/S, SEL68,OSC1 terminal | | 0.8VDD | | VDD | V | |
| | Low Level | VILC1 | | | VSS | | 0.2VDD | | |
| Output Voltage | High Level | VHC11 | D0toD1 Terminal | IOH=-0.5mA | 0.8VDD | | VDD | V | |
| | Low Level | VOLC11 | | IOL= 0.5mA | VSS | | 0.2VDD | | |
| Input Leagage Current | | ILI0 | All input terminal, D0 to D15 Terminal in High Z | | -1.0 | | 1.0 | µA | |
| Driver On-resistance | | RON | Ta=25°C VLCD=15V | | | 2.0 | 3.0 | kΩ | 3 |
| Stand-by Current | | IDDQ | During Power Save Mode | | | T.B.D | T.B.D | µA | 4 |
| Input Terminal Capacitance | | CIN | Ta=25°C | | | 10 | | pF | 6 |
| Oscillation Frequency | | fOSC | VDD= 3.0V, Ta=25°C | | | T.B.D | | kHz | |
| Reset Time | | tR | $\overline{RES}$ terminal | | 1.0 | | | µS | 7 |
| Reset "L" level pulse Width | | tRW | | | 10 | | | µS | 8 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Voltage boost output voltage | VOUT1 | 7-times boost, VDD=2.5V | VDD-17.5V | | VDD-17.0V | V | |
| Voltage boost On-resistance | RTRI | 7-times boost, VDD=2.5V,Cout=4.7µF | | | 3.0 | kΩ | |
| Adjustment range of LCD driving Voltage | VOUT2 | Voltage boost operation off | VDD - 8.0V | | VDD - 6.0V | V | 9 |
| Voltage Follower | V5 | Voltage adjustment circuit "OFF" | VDD - 18.0V | | VDD - 6.0V | V | |
| Operating Current In use external Power supply | IDD01 | Display VLCD=16V | | TBD | TBD | µA | 10 |
| | IDD02 | Access fCYC=200KHz | | TBD | TBD | | |
| Operating Current In use internal power supply | IDD | Display VDD=3V,VLCD=16V , 6-time boost COn/Sn are Open , non-access , Display Checkerd pattern | | 300 | TBD | µA | |
| Voltage Regulator | VREG% | VDD=3.0V, Ta=25°C | | | T.B.D | % | 11 |

*1:NJU6682 can ooerate wide operating rangr,but it is not guarantee immideate voltage changing during the accessing of the MPU.

*2:The operating current in use external power supply.

*3:RON is the resistance values beteen power supply terminals (V1,V2,V3,V4) and each output terminals of common and segment suppliedby 0.1V. This is specified within the range of supply voltage(2).

*4,5:In case of not use internal power supply circuit,meaning current of IC's. LCD driving power supply are external power supply.

*4,5,11:The value of after execute driver output-oninstruction.

*4:Apply no access from MPU.

*5:The operating current when always writing a vertical stripe pattern in tcyc. In accessing current is proportional to the access frequency approximately. When not accessed, I become only IDD01.

*6:Apply A0,D0toD15,$\overline{RD}$,$\overline{WR}$,$\overline{CS}$,$\overline{RES}$,SEL68,PS0,PS1 terminals.

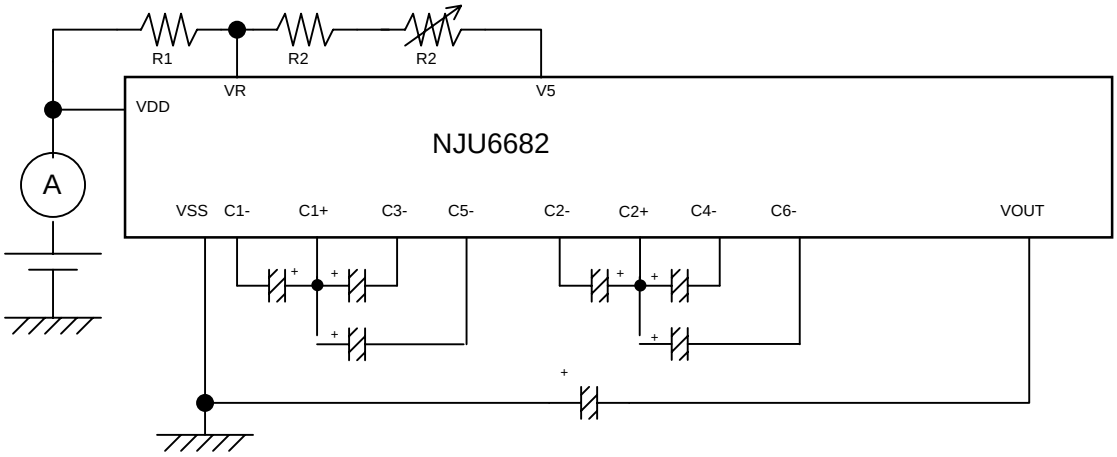
*7:tR ( the reset time ) shows the time of the inner circuit reset completion from the rise edge of the $\overline{RES}$ signal.

*8:Apply minimum pulse width of the RES signal. To operate the reset, the "L" pulse over tRW must be inputted.$\overline{RES}$.
*9:The voltage adjustment circuit controls V5 in the voltage follower operation voltage
*10:Each operating current is defined as being measured in the following condition.

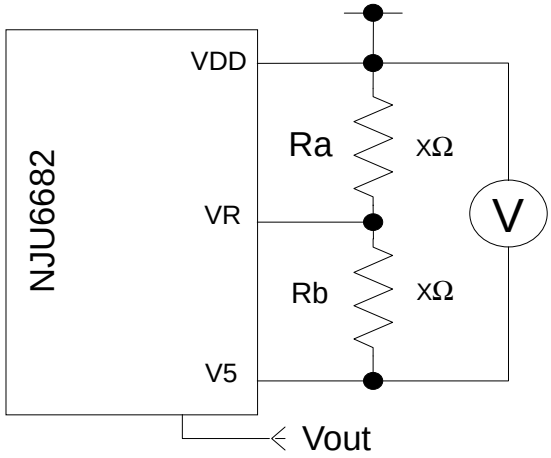
| SYMBOL | POWER SUPPLY SET INSTRUCTION | | | OPERATING CONDITION | | | | EXTERNAL VOLTAGE SUPPLY (INPUT TERMINAL) |
|---|---|---|---|---|---|---|---|---|
| | DC | VR | VF | Internal Oscillator | Voltage Booster | Voltage Adjustment | V/F Circuit | |
| $I_{DD1}$ | 1 | 1 | 1 | Validity | Validity (6-time boost) | Validity | Validity | Unuse |

- LCD output terminal Open.
- Display on,Display checered pattern,No access from MPU
- Set $V_{LCD}$=16V
- Set to R1+R2+R3=2MΩ

Mesurment Block Diagram
:$I_{DD1}$



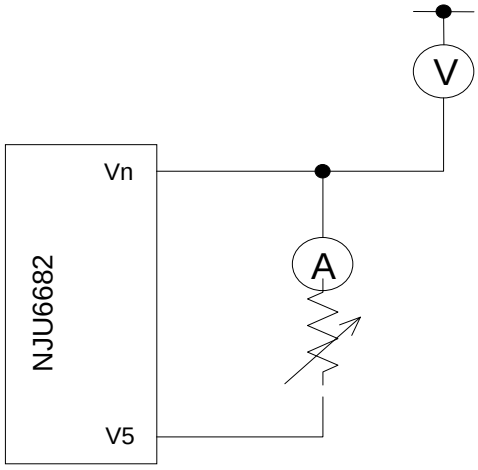
*11:As for power supply VREG, provide by the error of the $V_{LCD}$ output with the electronic volume.
It use the measurement system shown below.



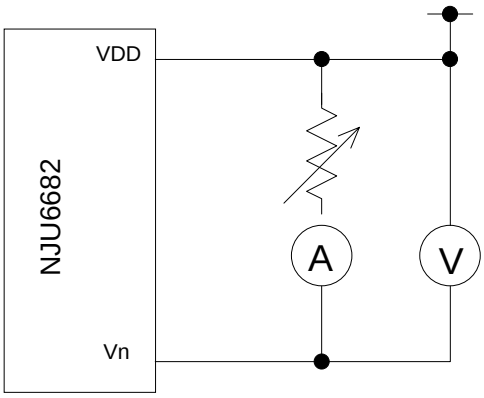

VREG%=(VREAL-VIDEAL)/VIDEALX100
- $V_{IDEAL}$ means a ideal value and $V_{REAL}$ means a measurement value.
- As for the calculation of VIDEAL, refer to voltage adjustment circuit (6-9-11), the voltage adjustment circuit (6-9-11) which used an electronic volume function.

*12:The voltage change by the output current prescribes a range within Vlcd X 5%. $V_{LCD}$=12.0V;($V_{DD}$-Vout)=16.0V.
It define a measurement system shown below.

*:Vn shows either of V1-V5 measurement terminal. V/F current supply performance is reduceed to the minimize because of the low consumption current.
Therefore, when measuring, the current which flows through the voltmeter in the figure, too, becomes not able to be ignored. When measuring, it requeire enough consideration.



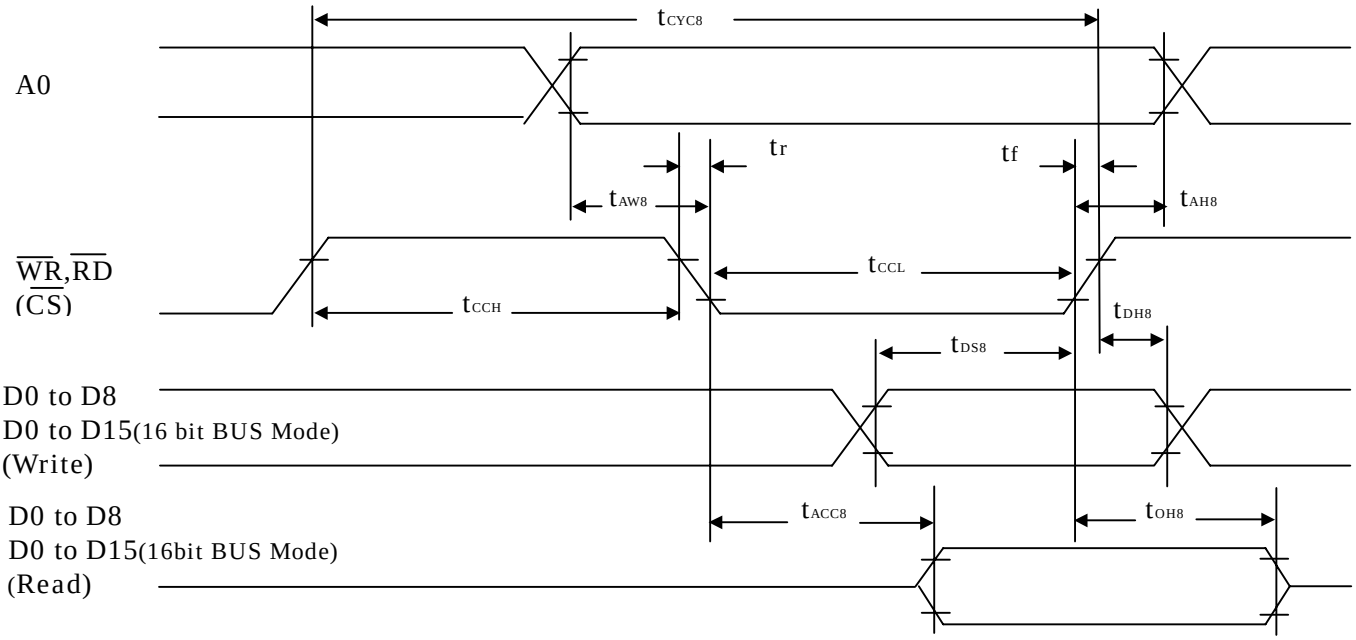

Measurement circuit for
Source current




Measurement circuit for
Sink current

■BUS TIMING CHARACTERISTICS

•Read/Write operation sequence(80 type MPU)

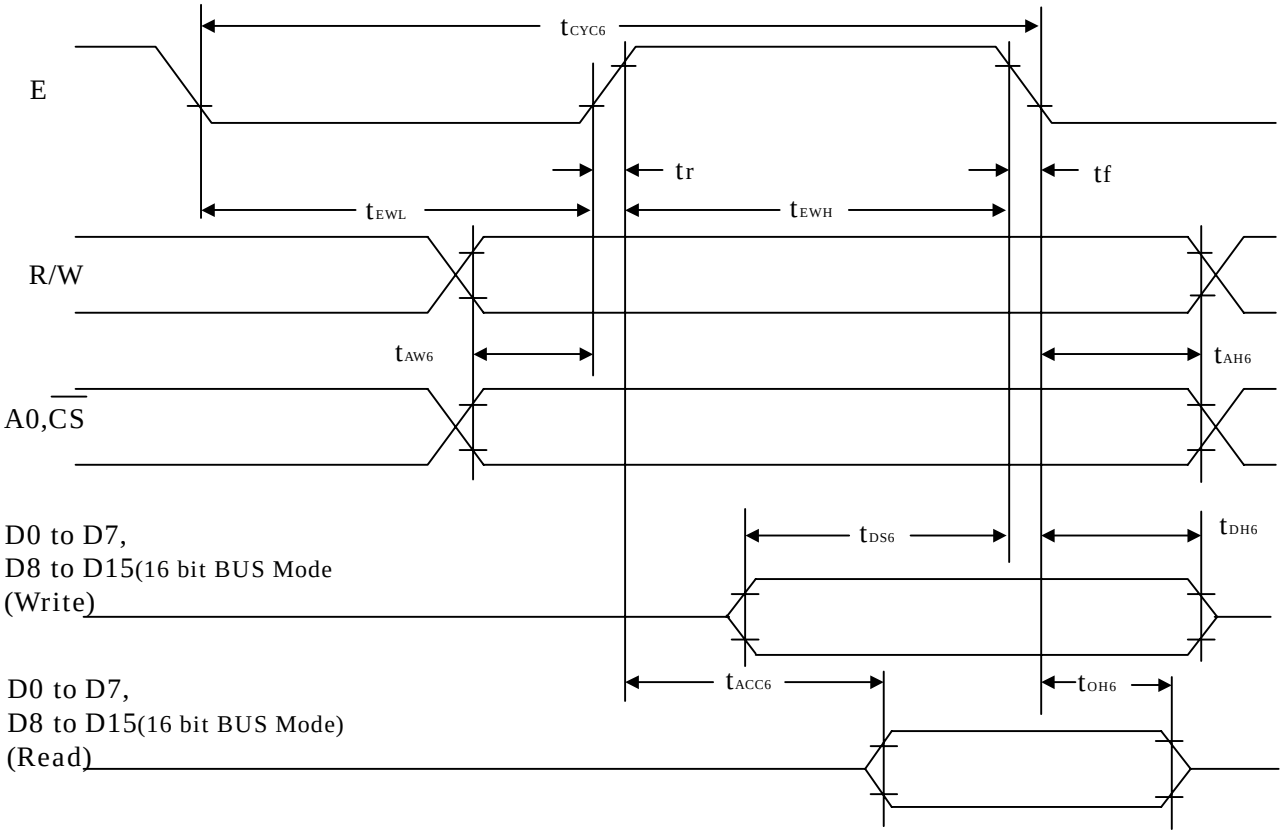



(VDD=2.4V to 3.3V, Ta=-30 to 80°C)

| PARAMETER | SIGNAL | SYMBOL | Measurement Condition | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Address Hold Time | A0,$\overline{CS}$ | tAH8 | | 0 | | | ns |
| Address Set up Time | | tAW8 | | 0 | | | |
| System Cycle Time (WRITE) | $\overline{WR}$ | tCYC8(W) | | 160 | | | |
| System Cycle Time (READ) | | tCYC8(R) | | 360 | | | |
| Control Pulse Width ($\overline{WR}$) | $\overline{RD}$ | tCCL(W) | | 50 | | | |
| Control Pulse Width ($\overline{RD}$) | | tCCL(R) | | 250 | | | |
| Control “H” Pulse Width | $\overline{WR}$,$\overline{RD}$ | tCCH | | 110 | | | |
| Data Set Up Time | D0 to D7 D8 to D15 | tDS8 | | 30 | | | |
| Data Hold Time | | tDH8 | | 5 | | | |
| Rdaccess Time | | tACC8 | CL=100pF | | | 240 | |
| Output Disable Time | | tOH8 | | 0 | | 50 | |
| Rise Time / FallTime | $\overline{CS}$,$\overline{WR}$,$\overline{RD}$ | tr, tf | | | | 15 | |

*1 All timing based on 20% and 80% of VDD.

•System BUS Sequence (Read / Write) (68-type MPU)

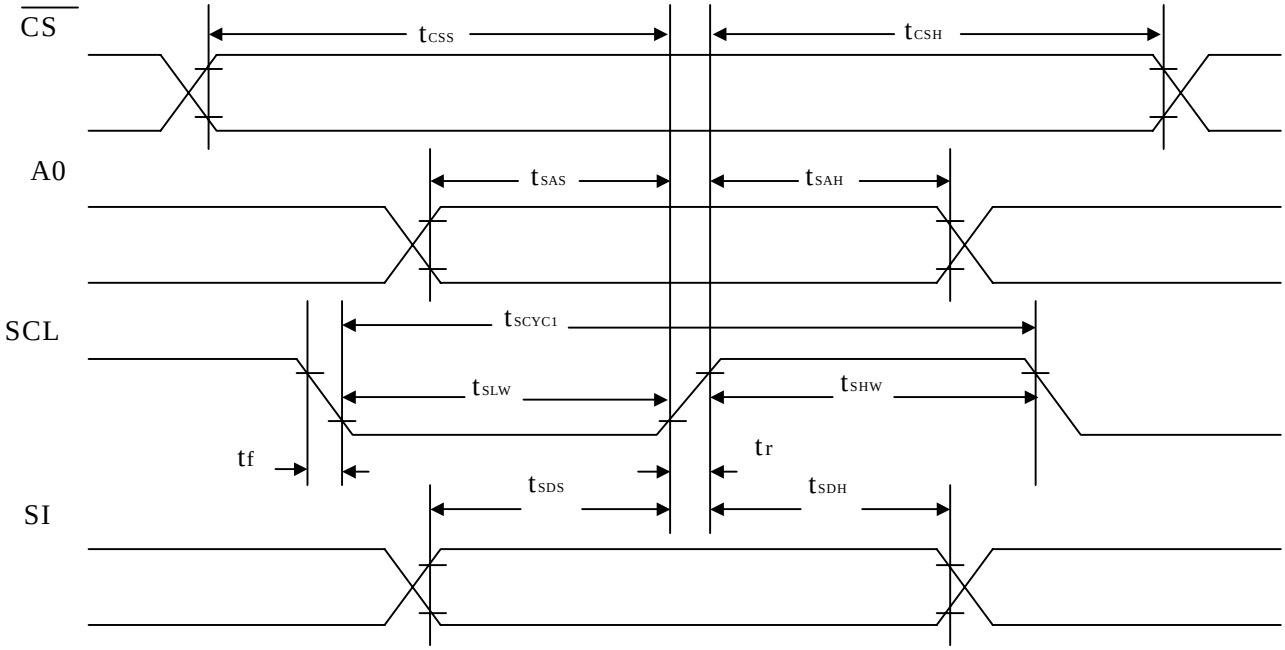



(VDD=2.4V to 3.3V, Ta=-30 to 80°C)

| PARAMETER | | SIGNAL | SYMBOL | Measurement Condition | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| Address Hold Time | | A0,$\overline{CS}$ R/W | tAH6 | | 0 | | | ns |
| Address Set Up time | | | tAW6 | | 0 | | | |
| System Cycle Time (WRITE) | | | tCYC6(W) | | 160 | | | |
| System Cycle Time (READ) | | | tCYC6(R) | | 360 | | | |
| Enable "H" Pulse Width | READ | E | tEWH | | 250 | | | |
| | WRITE | | | | 50 | | | |
| Enable "L" PilseWidth (READ/WRITE) | | | tEWL | | 110 | | | |
| Data Set Up Time | | D0toD7, D8toD15 | tDS6 | | 30 | | | |
| Data Hold Time | | | tDH6 | | 5 | | | |
| Access Time | | | tACC6 | CL=100pF | | | 240 | |
| Output Disable Time | | | tOH6 | | 0 | | 50 | |
| Rise Time / Fall Time | | tr, tf | E | | | | 15 | |

*1 All timing are based on 20% and 80% of VDD.
*2 tCYC6 shows the cycle of the E signal to place in the in active CS.

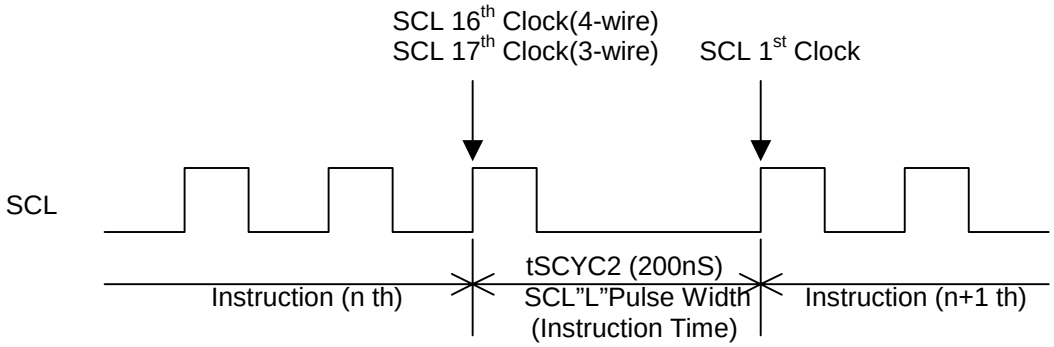
•Serial Interfave




(VDD=2.4V to 3.3V, Ta=-30 to 80°C)

| PARAMETER | | SIGNAL | SYMBOL | Measurement Condition | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| Serial Clock Cycle | Instruction Input | SCL | tSCYC1 | | 60 | | | ns |
| | Instruction Time*2) | | tSCYC2 | | 200 | | | |
| SCL"H" Pulse Width | | | tSHW | | 30 | | | |
| SCL"L" Pilse Width | | | tSLW | | 30 | | | |
| Address Set Up Time | | A0 | tSAS | | 15 | | | |
| Address Hold Time | | | tSAH | | 15 | | | |
| Data Set Up Time | | SI | tSDS | | 15 | | | |
| Data Hold Time | | | tSDH | | 15 | | | |
| $\overline{CS}$-SCLTime | | $\overline{CS}$ | tCSS | | 30 | | | |
| | | | tCSH | | 30 | | | |
| Rise Time / Fall Time | | SCL | tf, tr | | | | 15 | |

*1 All timing are based on 20% and 80% of $V_{DD}$.
*2 When inputting an instruction continuously, provide the cycle of SCL among the instructions as follows by 200 nS.



■LCD Driving Wave Form (Black & Whitr Mode)

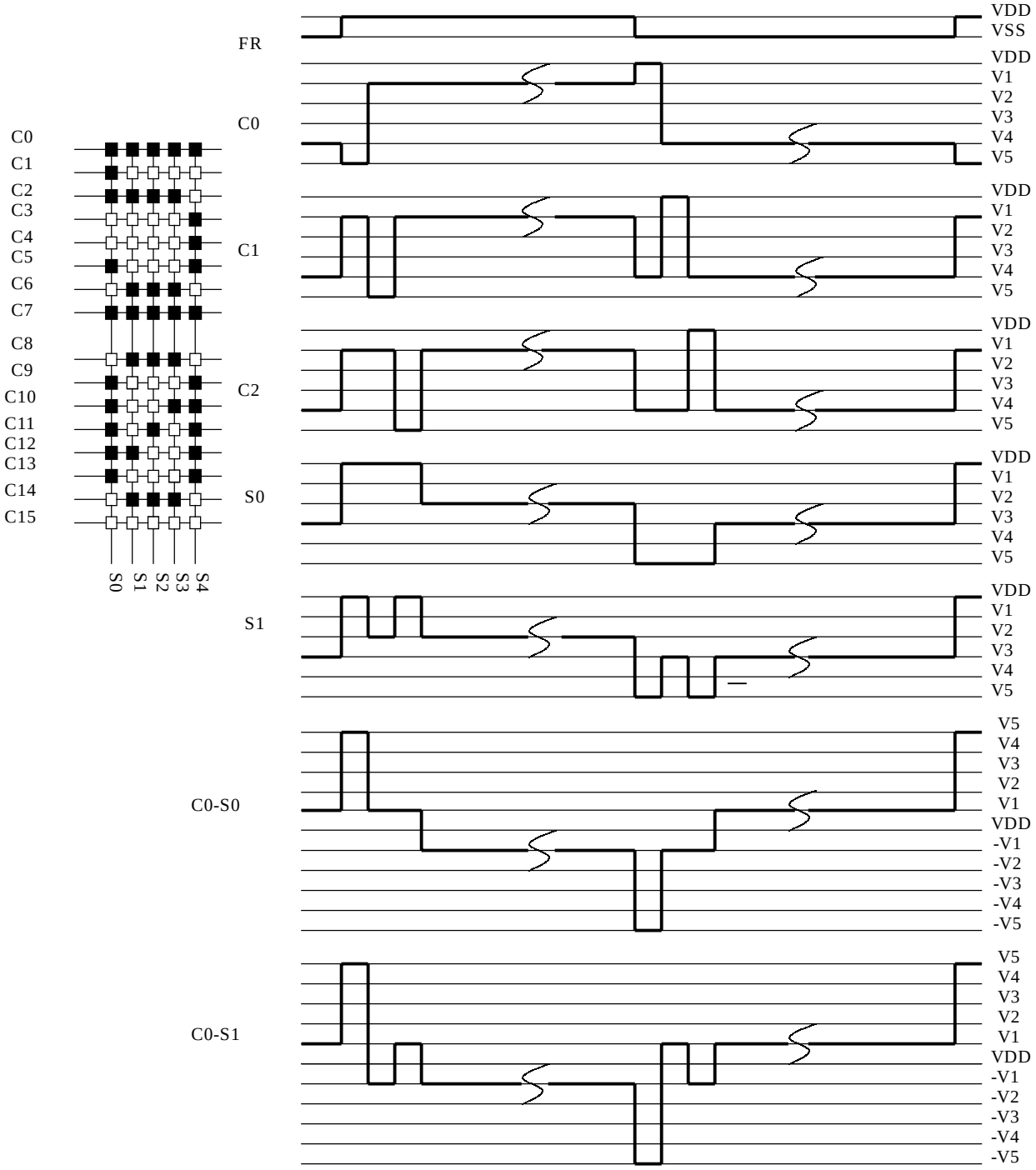



Fig 4

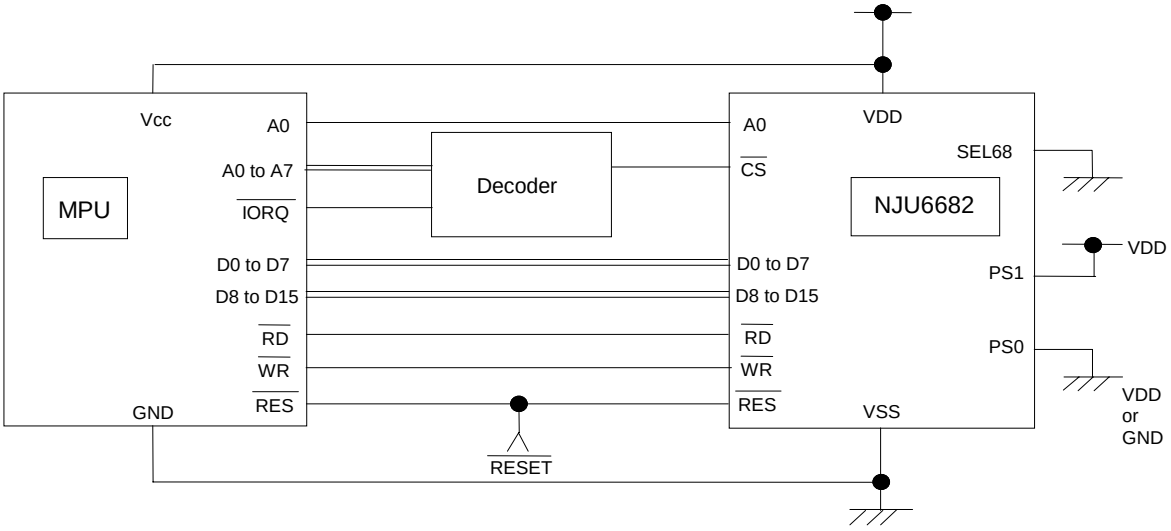
■APPLICATION CIRCUIT

MPU Interface Example

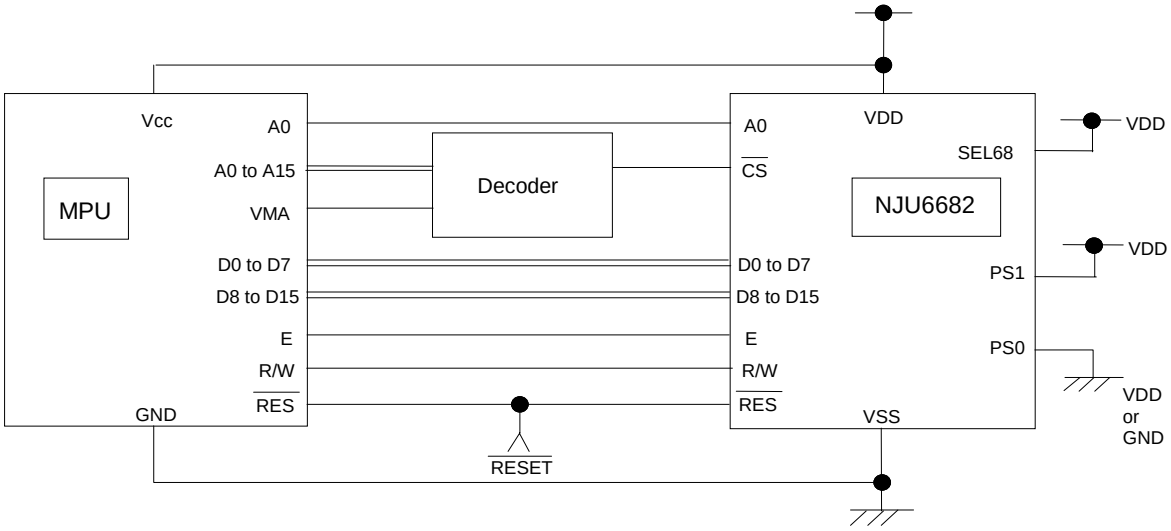
NJU6682 can direct connection with 80 type MPU and 68 type MPU. Moreover, with to use a serial interface, it is possible to control by the signal line with the more small being.

*:CEL68 terminal should be connect VDD or VSS.

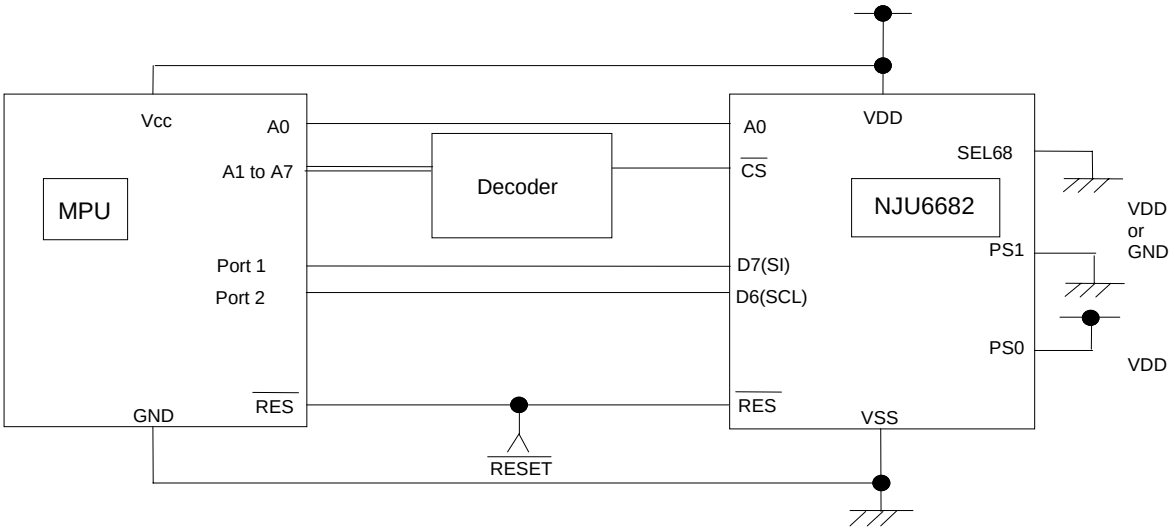
•80 type MPU




•68 type MPU




•Serial Interface (4-Wire)



MEMO

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