8bit 3ch D/A Converter

■ GENERAL DESCRIPTION

The NJW5210 is 8bit 3ch D/A converter for electronic adjustment. 3ch DC out put can be independently controlled by three-wire serial interface.

The NJW5210 features low operating voltage(2.7V) and can be full-swing outputted regardless of supply voltage.

The small package(TVSP8) is suitable for portable applications.

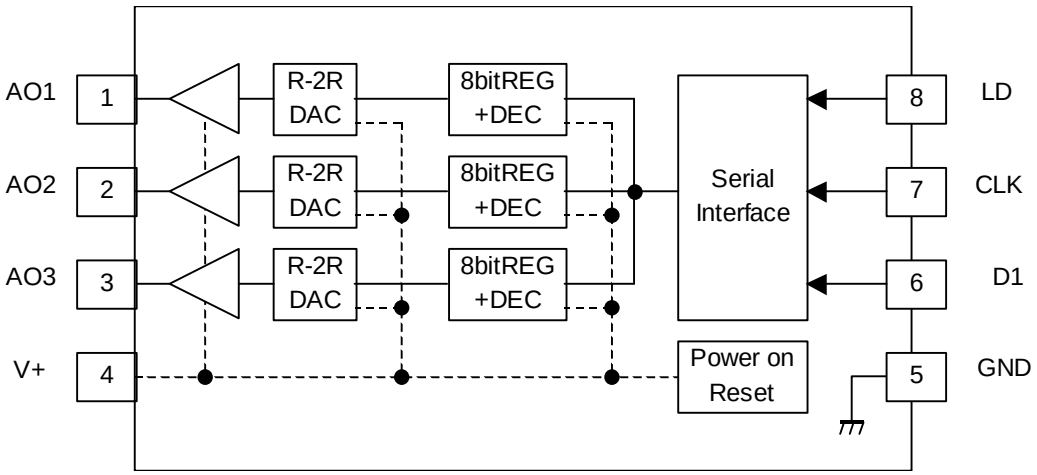
■ PACKAGE OUTLINE

NJW5210RB1

■ FEATURES

- Low Operating Voltage 2.7 to 5.5V
- 8bit 3ch D/A Converters Adopting R-2R System
- 3-wire 10-bit Serial Interface
- Internal POWER ON RESET Circuit
- Bi-CMOS Technology
- Package Outline TVSP8

■ BLOCK DIAGLAM and PIN DIAGRAM



Pin No.	Pin Name	IN/OUT	Function
1	AO1	OUT	Analog Output
2	AO2	OUT	Analog Output
3	AO3	OUT	Analog Output
4	V+	-	V+
5	GND	-	GND
6	DI	IN	Serial Data Input
7	CLK	IN	Serial CLK Input
8	LD	IN	Serial Load Input

■ **ABOSOLUTE MAXIMUM RATINGS** (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+	-0.3 to 7.0	V
Terminal Voltage	Vin	-0.3 to V^+	V
Power Dissipation	P_D	300	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +150	°C

■ **RECOMMENDED OPERATING CONDITION** (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	Vopr		2.7	-	5.5	V
Analog Output Source Current	IOL		-	-	1.0	mA
Analog Output Sink Current	IOH		-	-	1.0	mA
Serial Clock Frequency	FSCLK		-	1.0	-	MHz
Limit Road Capacitance	CL		-	-	0.1	μF

■ **ELECTRICAL CHARACTERISTICS** (V^+ =3.0V, RL=OPEN, CL=0pF, Ta=25°C)

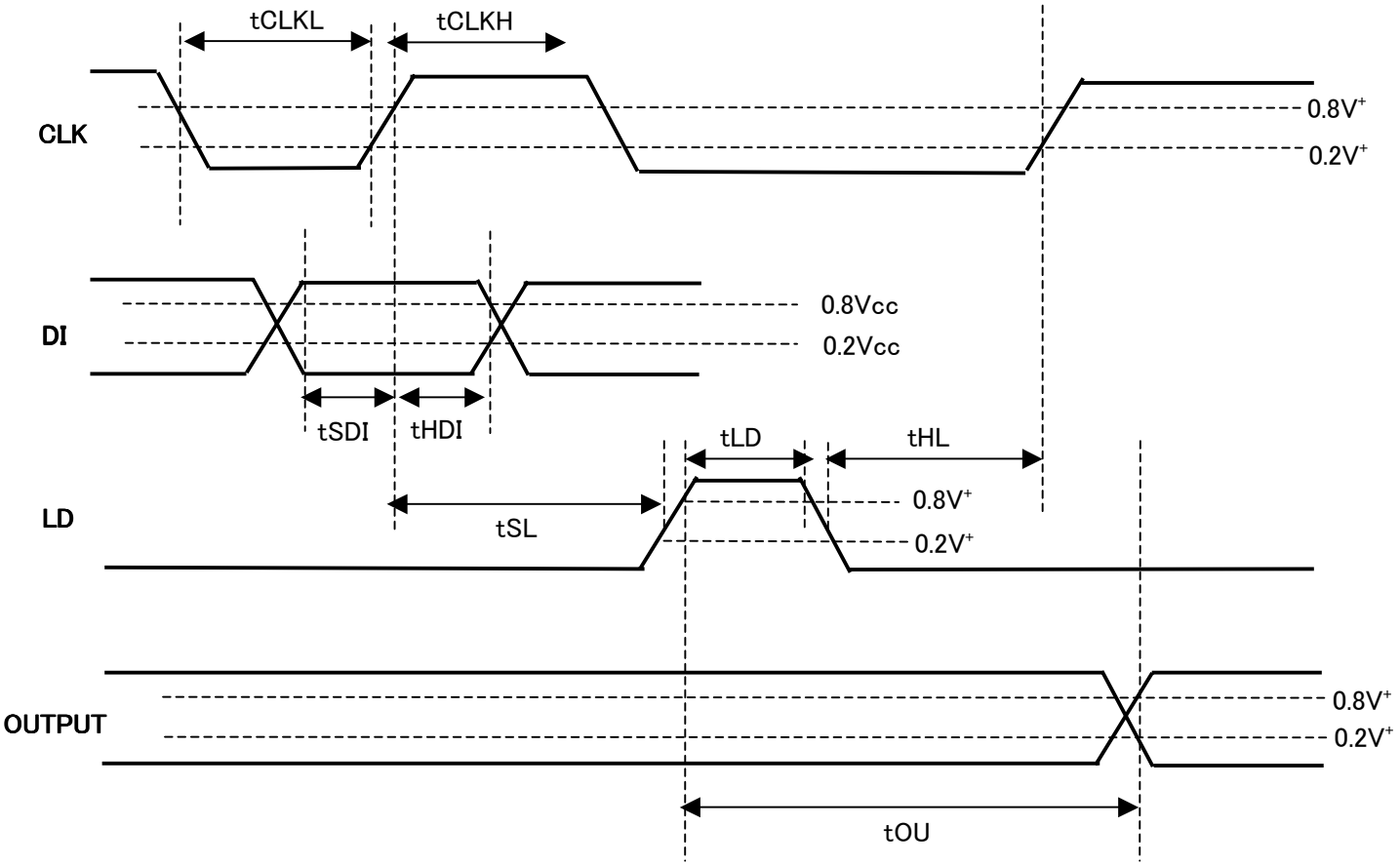
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I_{CC}	CLK=1MHz 80H set	-	0.4	0.8	mA
<Logic Interface>						
Input low voltage	VIL		0	-	0.3	V
Input high voltage	VIH		1.8	-	V^+	V
Input low current	IIL		-	-	10	μA
Input high current	IIH		-	-	10	μA
<Buffer Amplifier>						
Minimum output voltage	ZS1	00H set IOH=0.0mA	0	-	0.1	V
	ZS2	00H set IOH=0.5mA	0	-	0.2	
	ZS3	00H set IOH=1.0mA	0	-	0.3	
Maximum output voltage	FS1	FFH set IOL=0.0mA	V^+-0.1	-	V^+	V
	FS2	FFH set IOL=0.5mA	V^+-0.2	-	V^+	
	FS3	FFH set IOL=1.0mA	V^+-0.3	-	V^+	
<DAC accuracy>						
Resolution	RES		-	8	-	bit
Difference non-linearity error	DNL	Input code 02H to FDH	-1.0	-	1.0	LSB
Integral non-linearity error	INL	Input code 02H to FDH	-1.5	-	1.5	LSB

■ **POWER ON RESET**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V^+ supply voltage rise time	trVcc	V+=0→2.7V	10	-	-	ms
Power on reset voltage	VPOR		-	1.9	-	V

■ **Condition of operating timing**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
CLK L level pulse width	tCLKL		200	-	-	ns
CLK H level pulse width	tCLKH		200	-	-	ns
DI setup time	tSDI		30	-	-	ns
DI hold time	tHDI		60	-	-	ns
LD setup time	tSLD		200	-	-	ns
LD hold time	tHLD		100	-	-	ns
LD "H" level pulse width	tLDH		100	-	-	ns
Analog output delay time voltage	tOUT	CL=50pF, RL=10kΩ	-	-	300	μA



*A signal level is judged at 80% or 20% of V^+

■ Command sending

Control command is 3wire 10bit serial interface.(MSB first)
Data is taken in with rise edge og the CLK and output data is fixed in the LD high section.
Data is maintained in the LD low section.

LSB(LAST) MSB(FIRST)

Data set								Channel select	
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9

Data Set

D0	D1	D2	D3	D4	D5	D6	D7	Analog output voltage level
0	0	0	0	0	0	0	0	GND
1	0	0	0	0	0	0	0	$(V^+$-GND)/256x1
0	1	0	0	0	0	0	0	$(V^+$-GND)/256x2
1	1	0	0	0	0	0	0	$(V^+$-GND)/256x3
0	0	1	0	0	0	0	0	$(V^+$-GND)/256x4
:	:	:	:	:	:	:		:
0	1	1	1	1	1	1	1	$(V^+$-GND)/256x254
1	1	1	1	1	1	1	1	$(V^+$-GND)/256x255

Channel select

D8	D9	Address select
0	0	AO1
1	0	AO2
0	1	AO3
1	1	Don’t care