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## NTE6860 Integrated Circuit NMOS – FSK Digital Modem, 600bps

### **Description:**

The NTE6860 is a MOS subsystem in a 24-Lead DIP type plastic package designed to be integrated into a wide range of equipment utilizing serial data communications.

The modem provides the necessary modulation, demodulation and supervisory control functions to implement a serial data communications link, over a voice grade channel, utilizing frequency shift keying (FSK) at bit rates up to 600 bps. The NTE6860 can be implemented into a wide range of data handling systems, including stand alone modems, data storage devices, remote data communication terminals and I/O interfaces for minicomputers.

N-channel silicon-gate technology permits the NTE6860 to operate using a single-voltage supply and be fully TTL compatible.

The modem is compatible with the NTE6860 microcomputer family, interfacing directly with the Asynchronous Communications Interface Adapter to provide low-speed data communications capability.

### **Features:**

- Originate and Answer Mode
- Crystal or External Reference Control
- Modem Self Test
- Terminal Interfaces TTL-Compatible
- Full-Duplex or Half-Duplex Operation
- Automatic Answer and Disconnect
- Compatible Functions for 100 Series Data Sets
- Compatible Functions for 1001A/B Data Couplers

### **Absolute Maximum Ratings:**

Supply Voltage, $V_{CC}$ .....	-0.3 to +7.0V
Input Voltage, $V_{in}$ .....	-0.3 to +7.0V
Operating Temperature Range, $T_A$ .....	0° to 70°C
Storage Temperature Range, $T_{stg}$ .....	-55° to +150°C
Thermal Resistance, Junction-to-Ambient, $R_{thJA}$ .....	+120°C/W

Note 1. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g. either  $V_{SS}$  or  $V_{CC}$ ).

## Power Considerations:

The average chip-junction temperature,  $T_J$ , in °C can be obtained from:

$$1. T_J = T_A + (P_D \cdot R_{\theta JA})$$

Where:

$T_A$  ≡ Ambient Temperature, °C

$R_{\theta JA}$  ≡ Package Thermal Resistance, Junction to Ambient, °C/W

$P_D$  ≡  $P_{INT} + P_{PORT}$

$P_{INT}$  ≡  $i_{CC} \times V_{CC}$ , Watts – Chip Internal Power

$P_{PORT}$  ≡ Port Power Dissipation, Watts – User Determined

For most applications  $P_{PORT} \ll P_{INT}$  and can be neglected.  $P_{PORT}$  may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{PORT}$  is neglected) is:

$$2. P_D = K \div (T_J + 273^\circ\text{C})$$

Solving equations 1 and 2 for K gives:

$$3. K = P_D \cdot (T_A + 273^\circ\text{C}) + R_{\theta JA} \cdot P_D^2$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of K the values of  $P_D$  and  $T_J$  can be obtained by solving equations 1 and 2 iteratively for any value of  $T_A$ .

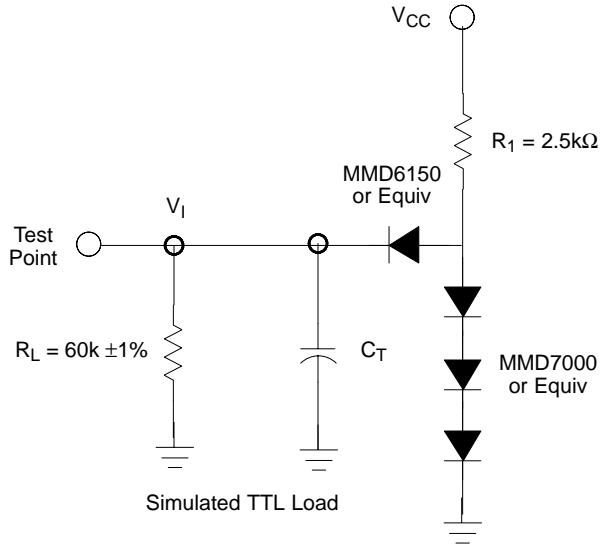
**DC Electrical Characteristics:** ( $V_{CC} = 5V \pm 5\%$ , all voltages referenced to  $V_{SS} = 0$ ,  $T_A = 0^\circ$  to  $+70^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input High Voltage	$V_{IH}$	All Inputs Except Crystal	2.0	–	$V_{CC}$	V
Input Low Voltage	$V_{IL}$	All Inputs Except Crystal	$V_{SS}$	–	0.80	V
Crystal Input Voltage	$V_{in}$	Crystal Input Driven from an External Reference, Input Coupling Capacitor = 200pF, Duty Cycle = 50 ±5%	1.5	–	2.0	$V_{P-P}$
Input Current	$I_{in}$	$V_{in} = V_{SS}$ All Inputs Except Rx Car, Tx Data, $\overline{TD}$ , TST, $\overline{RI}$ , SH	–	–	–0.2	mA
		$\overline{RI}$ , SH Inputs	–	–	–1.6	mA
Input Leakage Current	$I_{IL}$	$V_{in} = 7V$ , $V_{CC} = V_{SS}$ , $T_A = +25^\circ\text{C}$	–	–	1.0	$\mu\text{A}$
Output High Voltage	$V_{OH1}$	All Outputs Except An Ph and Tx Car, $I_{OH1} = -0.04\text{mA}$ , Load A	2.4	–	$V_{CC}$	V
Output Low Voltage	$V_{OL1}$	All Outputs Except An Ph and Tx Car, $I_{OL1} = 1.6\text{mA}$ , Load A	$V_{SS}$	–	0.40	V
	$V_{OL2}$	An Ph, $I_{OL2} = 0$ , Load B	$V_{SS}$	–	0.30	V
Output High Current	$I_{OH2}$	An Ph, $V_{OH2} = 0.8V$ , Load B	0.30	–	–	mA
Input Capacitance	$C_{in}$	$f = 0.1\text{Mhz}$ , $T_A = +25^\circ\text{C}$	–	5.0	–	pF
Output Capacitance	$C_{out}$	$f = 0.1\text{Mhz}$ , $T_A = +25^\circ\text{C}$	–	10	–	pF
Transmit Carrier Output Voltage	$V_{CO}$	Load C	0.20	0.35	0.50	$V_{RMS}$
Transmit Carrier Output 2 <sup>nd</sup> Harmonic	$V_{2H}$	Load C	–25	–32	–	dB
Input Transition Times	$t_r$	All Inputs Except Crystal, Operating in the Crystal Input Mode; from 10% to 90% Points, Note 2	–	–	1.0	$\mu\text{s}$
	$t_f$		–	–	1.0	$\mu\text{s}$
	$t_r$	Crystal Input, Operating in External Input Reference Mode	–	–	30	$\mu\text{s}$
	$t_f$		–	–	30	$\mu\text{s}$
Output Transition Times	$t_r$	All Outputs Except Tx Car, From 10% to 90% Points	–	–	5.0	$\mu\text{s}$
	$t_f$		–	–	5.0	$\mu\text{s}$
Internal Power Dissipation	$P_{INT}$	All Inputs at $V_{SS}$ and All Outputs Open, $T_A = 0^\circ\text{C}$	–	–	340	mW

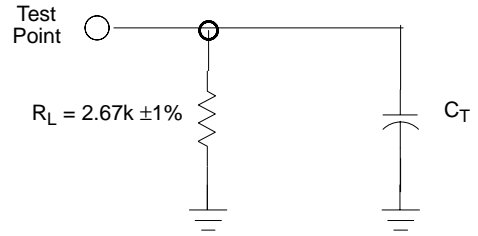
Note 2. Maximum Input Transition Times are  $\leq 0.1 \times$  Pulse Width or the specified maximum of 1 $\mu\text{s}$ , whichever is smaller.

### Output Test Loads

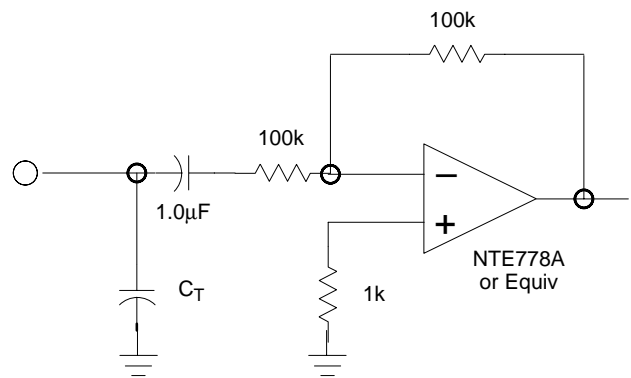
**Load A:** TTL Output Load for Receive Break, Digital Carrier, Mode, Clear-to-Send, and Receive Data Outputs



**Load B:** Answer Phone Load



**Load C:** Transmit Carrier Load



$C_T = 20\text{pF}$  = total parasitic capacitance, which includes probe, wiring, and load capacitance

### Pin Connection Diagram

