**Peripheral
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PRODUCT SPECIFICATION

Color Contact Image Sensor (CIS)

Model PI630MC-A6C Data Sheets

1. DESCRIPTION

This data sheet covers the PI630MC-A6C specification. The PI630MC-A6C is a color contact image sensor module. The module contains 7 image-sensor chips, PI3045B, a product of PIC. These chips are sequentially cascaded to provide a line array of photo-detectors. Each photo-detector in the image sensor posses its own independent processing circuit. As the photo-sensors' digital shift register scans the image sensor chip, it sequentially produces the video signals at the output of image array. The PI630MC-A6C's schematic and its mechanical outline drawing are located on page 9 and 10 respectively.

2. OVERVIEW

The PI630MC-A6C has 102 mm read width. Its minimum line rate is 520 μs/line with a maximum CP, clocking speed, equal to 2.5 MHz (PRATE, pixel rate 5 MHz). Consistent with its typical operational frequencies, CP = 2.0 MHz and PRATE = 4.0MHz, the data are given with integration time of 640 μs/line. Its sensor photo-site density is 23.64 elements/mm. The module has one analog video output; two clock inputs, CP and SP (the start pulse); one reference voltage input for the amplifier output bias level control; one power supply input; and four LED inputs.

2.1 Special Feature: Flush Mode

A special added feature is the Flush Mode that functions as an electronic shutter. It is not a true electronic shutter in its classical sense. Instead of an instantaneous reset time, it resets duration is one sensor chip's line scan time, rather than taking whole line scan time that includes all seven sensor chips. Its operational description is included in under the discussion of the schematic, section 10.0 Schematic Diagram, page 9.

3. SCAN OUTLINE

TABLE 3.1 SCAN OUTLINE

ITEM	SPECIFICATION	NOTE
READABLE WIDTH	102 mm	
SENSOR PHOTO-SITE DENSITY	23.64 elements/mm	
NUMBER OF ACTIVE SENSOR PHOTO-SITES	2408 elements	
LINE READ TIME [1]	~520 µs/line	Tested @ 5.0 MHz Pixel Rate (PRATE)
CLOCK FREQUENCY [1]	2.5 MHz	MAX RATE
PIXEL RATE [1]	5.0 MHz	MAX RATE

Note (1) unless otherwise noted, although the module is tested at 5.0MHz, all of the data were tested and specified with a typical clock frequency of 4.0MHz. Since the light power is fixed, if the line-scan rate is set proportional to the clock rate, then the integration time reduces as clock frequency is increased, hence its exposure. The reduction in the exposure proportionately reduces the video output. Accordingly, the signal-to-noise ratio reduces as the frequency increased.

4. PHYSICAL OUTLINE

TABLE 4.1 PHYSICAL OUTLINE

ITEM	SPECIFICATION	NOTE
IMAGE SENSORS	PERIPHERAL IMAGING CORP. PI3045B	SEE IMAGE SENSOR DATA SHEET
Module Outside Dimension	$\cong$125 mm X 18.9 mm X 12 mm	ATTACHED TO DATA SHEET
CIRCUIT POWER SUPPLY	TYPICAL 5.0V @ 30 ma	
DATA OUTPUT	1 ANALOG OUTPUT	
SCHEMATIC DIAGRAM		On page 9

5. RECOMMENDED OPERATING CONDITIONS
(All tests was conducted at typical pixel rate of 4.0MHz)

TABLE 5.1 RECOMMENDED OPERATING CONDITIONS (25 ^{o}C)

ITEM	SYMBOL	MIN	TYPICAL	MAX	UNITS
POWER SUPPLY	VDD	4.5	5.0	5.5	V
	IDD		30	40	ma
VIDEO OUTPUT LEVEL	VP [1]	0.7	1.0	1.3	V
REFERENCE VOLTAGE INPUT (LEAVE FLOATING, UNCONNECTED)	VREF [2]				UNCON NECTED
INPUT VOLTAGE FOR DIGITAL HIGH (INPUT CLOCKS, SP AND CP.)	VIH	VDD-1.0	VDD-.5	VDD+0.3	V
INPUT VOLTAGE FOR DIGITAL LOW (INPUT CLOCKS SP AND CP)	VIL	0		0.8	V
CLOCK FREQUENCY	FCLK [3]	0.25		2.5	MHz
PIXEL FREQUENCY	PRATE [3]	0.50		5.0	MHz
CLOCK PULSE HIGH DUTY CYCLE	DUTY [4]	45	50	55	%
CLOCK PULSE HIGH DURATION	TPW	200			ns
INTEGRATION TIME	TINT [5]	~520		10000	µs
OPERATING TEMPERATURE	TOP [6]		25	50	^{0}C

Notes:

Note (1)   VP is a symbol representing the average value Vp(n) for all n in line scan, where n is the sequential number of a pixel. This signal pixel level should be operated under saturation levels, i.e., <1.7 Volts.

Note (2)   VREF is used to adjust the video output bias. Under normal operation it is left unconnected and floating.

Note (3) FREQ is the input clock (CP) frequency and its corresponding PRATE is 2 X FREQ. Where PRATE is the video pixel rate. The minimum rate for FREQ and PRATE should be consistent with the maximum TINT, see note (5).

Note (4) DUTY is the ratio of the clock's pulse width over its pulse period.

Note (5) TINT is the time interval between two start pulses, SP. Hence, if SP is generated from a clock count down circuit, it will be directly proportional to clock frequency. There must be a minimum of (56+1204) clocks cycle between the two SP. The longest integration time is determined by the degree of leakage current degradation that can be tolerated by the system.   A 10ms maximum is a typical rule-of-thumb. An experienced CIS user can use his discretion and determine the desired leakage tolerance level for the given system.

Note (6) TOP is a conservative engineering estimate. It is based on measurements of similar CIS modules. In production they are measured under standard QA practices that is under control of ISO 9000 standards.

6.0 ELECTRO-OPTICAL CHARACTERISTICS

(All tests was conducted at typical pixel rate of 4.0MHz)

TABLE 6.1 ELECTRO-OPTICAL CHARACTERISTICS (25° C)

PARAMETER	SYMBOL	TYPICAL	UNITS	NOTE
NUMBER OF ACTIVE PHOTO DETECTORS		2408	elements	
PIXEL-TO-PIXEL SPACING		42.3	µm	
LINE SCANNING RATE	TINT [1]	~640	µs/line	@ 2.0 MHz clock frequency
CLOCK FREQUENCY	FREQ [2]	2.0	MHz	
PIXEL RATE	PRATE [2]	4.0	MHz	
RED RESPONSIVITY	ExpR[3]	2500	V/µJ/cm2	See Note 3 @ 6.27ma
GREEN RESPONSITY	ExpG[3]	4250	V/µJ/cm2	See Note 3 @ 5.6ma
BLUE RESPONSITY	ExpB[3]	2630	V/µJ/cm2	See Note 3 @ 11.47ma
BRIGHT OUTPUT VOLTAGE	Vpavg [4]	1.0 (Typical)	Volts	
BRIGHT OUTPUT NON-UNIFORMITY	Up [5]	<+/-30	%	
BRIGHT OUTPUT NONUNIFORMITY TOTAL	Uptotal [6]	<60	%	
ADJACENT PIXEL NONUNIFORMITY	Uadj [7]	<25	%	
DARK NONUNIFORMITY	Ud [8]	<150	mV	
DARK OUTPUT VOLTAGE RANGE	VDL [9]	1.4<VDL<1.7	V	.

RANDOM NOISE	RNL [10]	<24 <4	p-p mV rms mV	
MODULATION TRANSFER FUNCTION	MTF [11]	45	%	

Notes:

(1) TINT is the line scan rate or integration time. TINT is determined by the time interval between two start pulses (SP). See above Table 5.1, under Note 5.

(2) FREQ is the input clock frequency and its corresponding PRATE is the pixel sample rate.

(3) The RESPONSIVITY is the ratio of video signal in volts divided by the unit exposure (Volts/micro-Joules/cm^2). The VP level was adjusted to ~1.6V with the individual LED currents as specified in table's the note column with module lying flat down on white sheet with OD between 0.05 to 0.09.

(4) Vpmax = maximum pixel value of Vp(n); Vpmin = minimum pixel value of Vp(n); Vpavg = Σ Vp(n)/2408; where Vp(n) is the nth pixel in a line scan with the module scanning a uniform white target. Vp values are measured with a uniform exposure.

(5) BRIGHT OUTPUT NONUNIFORMITY: Up(+) = [(Vpmax - Vpavg) / Vpavg] x 100% or Up(-)= [(Vpavg - Vpmin) / Vpavg] x 100%, whichever polarity with the highest absolute value is selected.

(6) BRIGHT OUTPUT TOTAL NONUNIFORMITY: Uptotal = [Vpmax -Vpmin]/Vpavg

(7) ADJACENT PIXEL NONUNIFORMITY: Upadj = MAX[| (Vp(n) - Vp(n+l) | / Vp(n)) x 100%. Upadj is the nonuniformity in percentage. It is the maximum difference amplitude between two neighboring pixels.

(8) DARK NONUNIFORMITY: Ud = Vdmax – Vdmin: Vdmax is the maximum pixel value of the video pixel with the exposure off. Vdmin is the minimum pixel value of the video pixel with exposure off. The references for these levels are the dark level, VDL.

(9) DARK OUTPUT VOLTAGE, VDL is the level between the output dark level and ground.

(10) RANDOM NOISE, RNL, its rms value was calculated from measured p-p thermal noise taken at output from a selected pixel. The rms is defined as one standard deviation of at least 64 pixels samples. The calculation of the standard deviation is based on idealized Gaussian Probability Curve.

(11) MODULATION TRANSFER FUNCTION is defined as MTF = [(Vmax - Vmin) / (Vmax + Vmin)] x 100 [%]. MTF is measure at glass surface. Vmax: maximum output voltage at 300 lp/inch (At 1/2 of the optical Nyquest Frequency)
Vmin: minimum output voltage at 300 lp/inch.

7.0   ELECTRICAL CLOCKING CHARACTERISTICS.

TABLE 7.1 CLOCK AMPLITUDE AND DUTY CHARACTERISTICS   (Ta =25°C)

ITEM	SYMBOL	CONDITION	SPECIFICATION			UNITS
			MIN	TYP	MAX	
CLOCK INPUT VOLTAGE	VIH [1] VIL [1]	For values see the notes		See note (1) for values		
CLOCK INPUT CURRENT	IIH [1] IIL [1]			See note (1) for values		
CLOCK FREQUENCY	FCLK [2]		Note (3)		2.5	MHz

PIXEL RATE	PRATE [2]		Note (3)		5.0	MHz
LINE READ TIME	TINT [4]		~0.520		~10	ms
CLOCK PULSE DUTY CYCLE	RATIO= twp / tp [5]		45	50	55	%

Note 1. These clock, CP, and start pulse, SP, values are compatible with CMOS 74HCXX series logic devices.

Note 2. FREQ is the clock frequency and PRATE (2XFREQ) is the pixel sample rate.

Note 3. Minimum values were not specified because it will be determined by maximum TINT value. See Note 4.

Note 4. TINT is the Line scan read time that depends on the interval between the start pulse entries. The minimum time is determined by (1/clock frequency) x (2408 + 150) pixels. Note, that there are a few extra pixels used to determine the typical line time of 640 μsec @ 4.0MHz PRATE. See Figure 1, TIMING DIAGRAM. There are 55 clocks required to transfer and reset the photo-sites before the video can be scanned out. The longest integration time is determined by the degree of leakage current degradation that can be tolerated by the system. A 10ms maximum is a typical rule-of-thumb. An experienced CIS user can use his discretion and determine the desired tolerance level for the given system.

Note 5. The definition for the symbols used in the RATIO is defined under the 7.2 Timing Diagram. Duty cycle of exactly 50% is recommended to maintain equal pixel duration between the odd and even pixels.

7.2 TIMING DIAGRAM
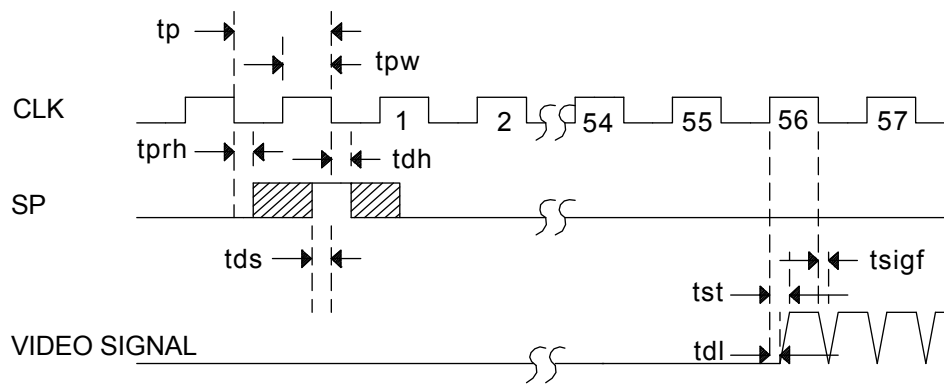
TIMING OF SP-TO-FIRST PIXEL

FIGURE 1. TIMING DIAGRAM

TABLE 7.2 CLOCK TIMING CHARACTERISTICS FOR THE TIMING DIAGRAM, FIGURE 1
(As noted under Table 3.1, all tests was conducted at typical pixel rate of 4.0MHz)

ITEM	SYMBOL	MIN.	TYPICAL	MAX.	UNITS
CLOCK CYCLE TIME	tp [1]	500			ns
CLOCK PULSE WIDTH	tpw [1]	250			ns
CLOCK DUTY CYCLE		45	50	55	%
PROHIBIT CROSSING TIME OF START PULSE	tprh	30			ns
DATA SETUP TIME	tds	30			ns
DATA HOLD TIME	tdh	30			ns
SIGNAL DELAY TIME	tdl			50	ns
SIGNAL SETTLING TIME	tst			130	ns
SIGNAL FALL TIME	tsigf			60	ns

General Note: All of the symbol definitions used in above table are given in Figure 1, TIMING DIAGRAM. The two clocks, CP, and start pulse, SP, values are compatible with CMOS 74HCXX series logic devices.

Note (1) Maximum CLOCK CYCLE TIME, as with minimum FREQ, must be consistent with maximum TINT. See under Table 5.1, Note (3).

8.0 MAXIMUM RATINGS

TABLE 8.1 MAXIMUM RATINGS (Not to be used for continuous operation)

ITEM	SYMBOL	SPECIFICATION	NOTE
DC SUPPLY VOLTAGE	VDD	7 V	
INPUT VOLTAGE	VIN	VDD	SP & CP
AMBIENT TEMPERATURE [1]	TA (PCB Surface)	0 TO 50°C (See note, below.) -10° to +75°C (See note, below.)	Operational Storage
AMBIENT HUMIDITY [1]	HA	0 to 80% (See note)	Non Condensing
MAXIMUM OPERATING CASE TEMPERATURE [1]	PCB Temperature	70°C (See note, below.)	

9.0 I/O CONNECTOR PIN CONFIGURATION

The connector is for a 12 pin-flex-strip-line cable, PDK97-1201. The connector location is shown in FIGURE 2, MECHANICAL STRUCTURE an ISO drawing of the PI630MC-A6C module. It also shows the location for pin 1.

9.1 Caution when connecting the power to the LED:

All the negative sides of the LED sources are connected to the cathodes. These I/O sources are current inputs. Constant current sources are used to control balance the color in the RGB outputs. Their typical voltage drops are between 2.3 to 2.7 Volts. Under no circumstances should the applied current be greater than 30 ma, otherwise the LED source will be damaged.

TABLE 9.1 CONNECTOR PIN OUTS

PIN NUMBER	PIN NAMES	SYMBOL	I/0	NAMES AND FUNCTIONS
1	ANALOG SIGNAL OUTPUT	VOUT	O	Analog signal output
2	GROUND	GND	I	Ground; 0V
3	POWER SUPPLY	VDD	I	Positive 5 Volts
4	SCAN INITIATE SELECTOR	SIC	I	Selects the chip for scan initiate mode (Flush Mode)
5	REFERENCE VOLTAGE	VREF	I	For externally controlling the dark bias level (left floating).
6	START PULSE	SP	I	Shift register start pulse
7	GROUND	GND	I	Ground; 0V
8	CLOCK	CP (CLK on the schematic)	I	Clock input for the module
9	COMMON	VLED (Common Anode on the schematic)	I	Common anodes for all LED. Plus 5.0 Volts terminal
10	LED GREEN	GLED	I	Cathode green LED input
11	LED RED	RLED	I	Cathode red LED input
12	LED BLUE	BLED	I	Cathode blue LED input

10.0 SCHEMATIC DIAGRAM

A Schematic diagram is attached for the reference. The module is relatively simple in construction. It is composed of seven (7) image sensors that are cascaded in sequence to form the complete line scan. In the normal line scan mode SIC control, pin 4 of I/O connector, is held low. For its high condition see the paragraph below. As Figure 1 shows, when SP is entered, the line scanning process is started. The first chip allows 55 clocks of preprocess time to initialize all of the image sensors and parallel transfers the previously integrated video signal out to the sample and hold circuits. Then while the next line's incoming projected images are integrated into proportional video voltages at each of the pixel element, the previously sampled and held video signals are sequentially read out onto a common output video line. To retain a continuous stream of sequential video pixels from the seven sensors, the sensors start their scanning process as they receive a start pulse, SI, from their preceding sensor's end-of-scan, EO, pulse. After the last sensor scans its last pixel, the next line scan will initiate when SP is again entered.

The Flush Mode is a special feature. It acts as a pseudo electronic shutter. Instead of instantly clearing the stored images in all the detector elements, its reset time takes one sensor's line-scan time, rather than the whole line time of 7 image sensors. To implement the Flush Mode the input, SIC, on pin 4 of the I/O connector is used. Normally this SIC is held low, while the first sensor's SIC remains high. This provides a condition for a standard line scan operation. But pulling pin 4 on the I/O input high, between the 53 and 56 cycle, will pull every sensor chip's SIC control high, as a result, each chip on the sensor board PCB will simultaneously starts its scanning process. Hence, the reset of any accumulated dark signal will completely scan out during one sensor chip's line time. To restore the module to its normal scan process, SIC is pulled low.
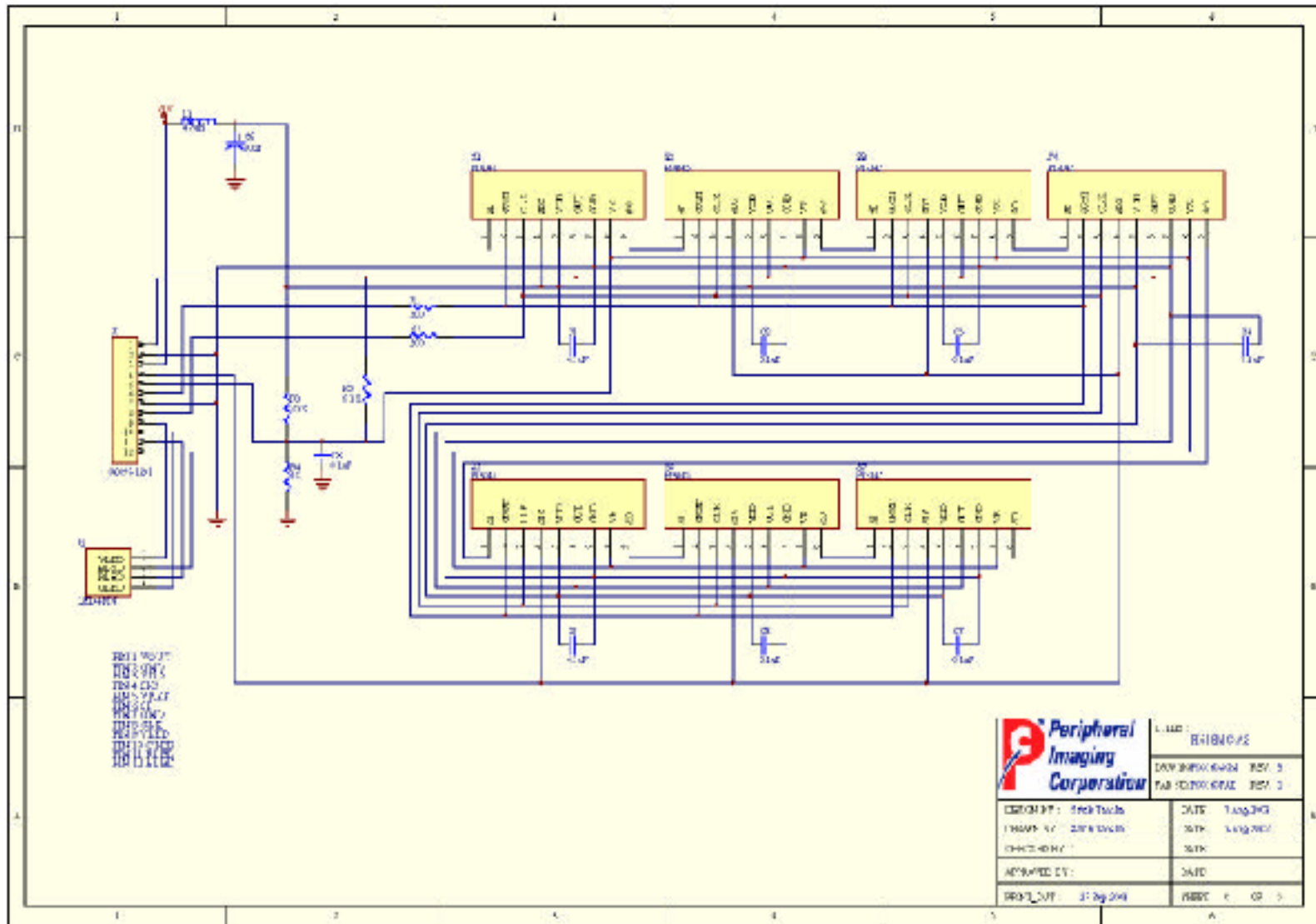 (See next page for Schematic Diagram)

FIGURE 2. PI630MC-A6C SCHEMATIC DIAGRAM

11.0 MODULE OUTSIDE DIAGRAM

A simplified ISO drawing of the module housing is shown Figure 3. Mechanical Structure. It is not to scale, but sufficient dimensions are shown for use in a preliminary application study. Furthermore, it shows the I/O connector location, its pin 1 location, the read line location and LED pad locations. For detailed design information, please contact Peripheral Image Corporation for a complete housing drawing.
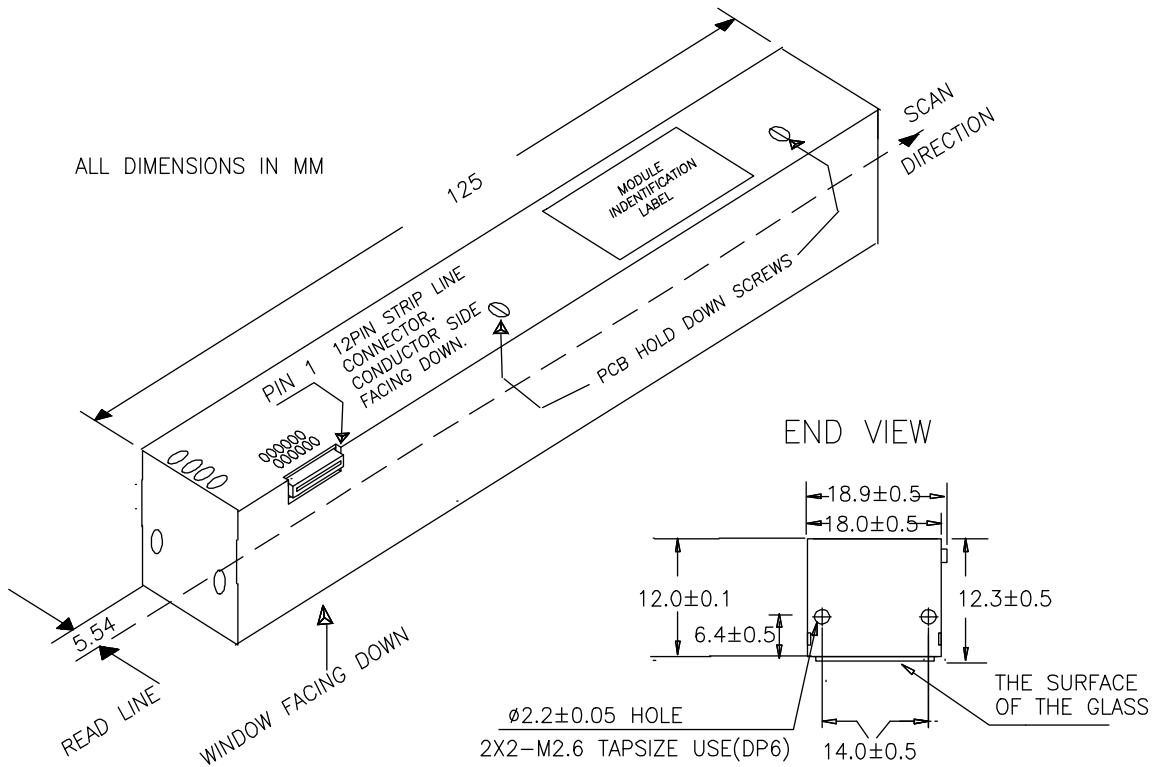

FIGURE 3. MECHANICAL STRUCTURE