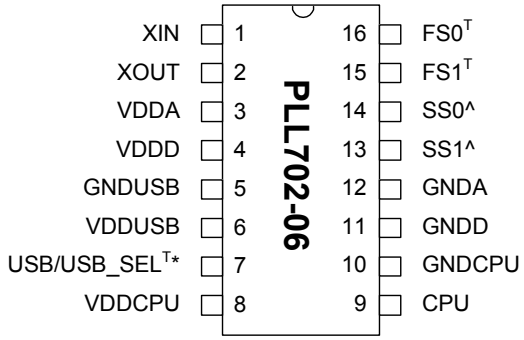
PLL702-06

Clock Generator for Printer Applications

FEATURES

- 1 CPU Clock output with selectable frequencies (50, 66.67, 75, 80, 83.3, 90, 100,125 or 133 MHz).
- 1 Selectable 48, 30 or 12MHz USB Clock output.
- Selectable Spread Spectrum (SST) for EMI reduction on CPU clock.
- PowerPC compatible CPU Clock.
- Advanced, low power, sub-micron CMOS processes.
- 14.31818MHz fundamental crystal input.
- 3.3V and/or 2.5V operation.
- Available in 16-Pin 150mil SOP.

PIN CONFIGURATION



Note : ^: Internal pull-up resistor
*: Bi-directional pin
T: Tri-level Input

DESCRIPTION

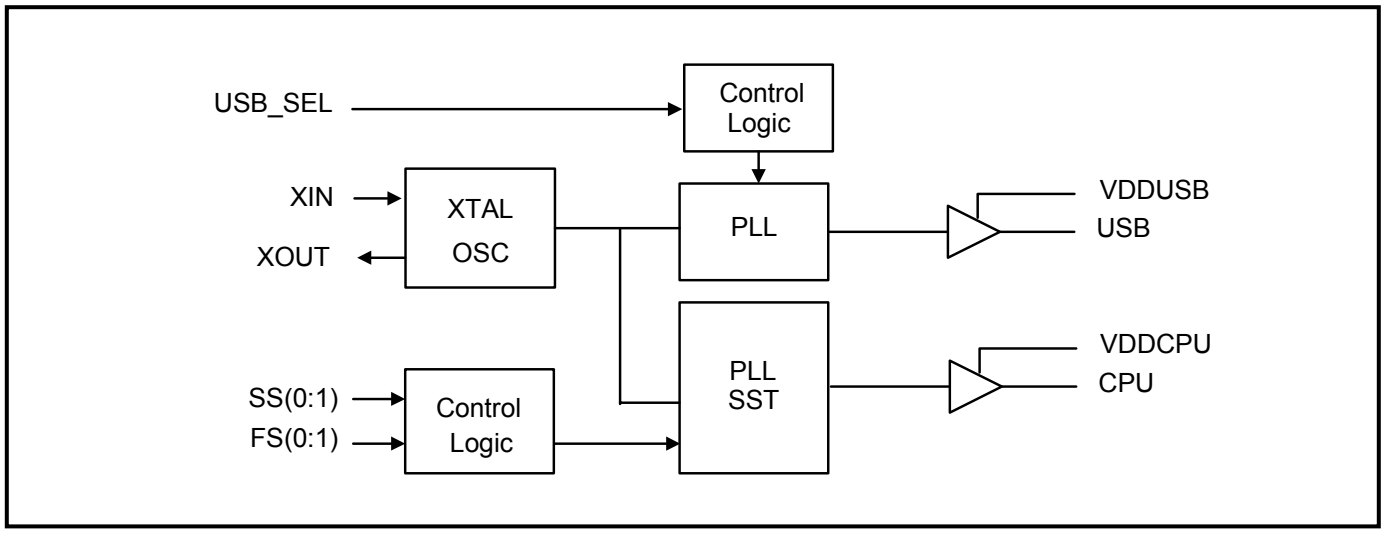
The PLL702-06 is a low cost, low jitter, and high performance clock synthesizer for generic Printer applications. It provides one CPU clock and a selectable 48, 30 or 12MHz (USB) output. The user can choose among 9 different clock frequencies and 3-selectable down-spread Spread Spectrum modulation to reduce EMI on CPU clock. All frequencies are generated from a single low cost 14.31818MHz crystal. CPU clock can be driven from an independent 2.5V or 3.3V power supply.

CPU CLOCK FREQUENCY TABLE

FS1	FS0	CPU (MHz)
0	0	50
0	M	66.67
0	1	75
M	0	80
M	M	83.33
M	1	90*
1	0	100
1	M	125
1	1	133*

***Notes**: Actual CPU frequency for 90Mhz is 88.88Mhz, 133Mhz is 130.9Mhz

BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Number	Type	Description
XIN	1	I	Crystal input to be connected to a 14.31818MHz fundamental crystal (CL = 20pF, parallel resonant mode). Load capacitors have been integrated on the chip. No external Load capacitor is required.
XOUT	2	O	Crystal Output
VDDA VDDD GNDA GNDD	3,4,11,12	P	3.3V power supply and GND.
VDDUSB VDDCPU GNDUSB GNDCPU	5,6,8,10	P	CPU and USB outputs have separate power supply pins (VDD and GND). VDDCPU can accept 3.3V and/or 2.5V power supply.
USB / USB_SEL	7	B	Bi-directional pin. Upon power-on, the value of USB_SEL is latched in and used to select the USB output (see USB selection table below). After the input has been latched-in, the pin serves as USB (48, 30 or 12 MHz) output. 0=15kΩ to GND, M=leave open, 1=15kΩ to VDD_USB
CPU	9	O	CPU clock signal output pin. The CPU clock frequency is selected as per the frequency table on page 1, depending on the value of FS(0:1).
SS(0:1)	13,14	I	Bi-level input with internal Pull-up resistor for SST control (see Spread Spectrum selection table on p.2). 0=connect to GND, 1=leave open (or to VDD).
FS(0:1)	15,16	I	Tri-level inputs for CPU clock frequency selection (see table on p.1). 0=connect to GND, M=not connected, 1=connect to VDDA.

USB FREQUENCY TABLE

USB_SEL	USB
0	48 MHz
M	30 MHz
1	12 MHz

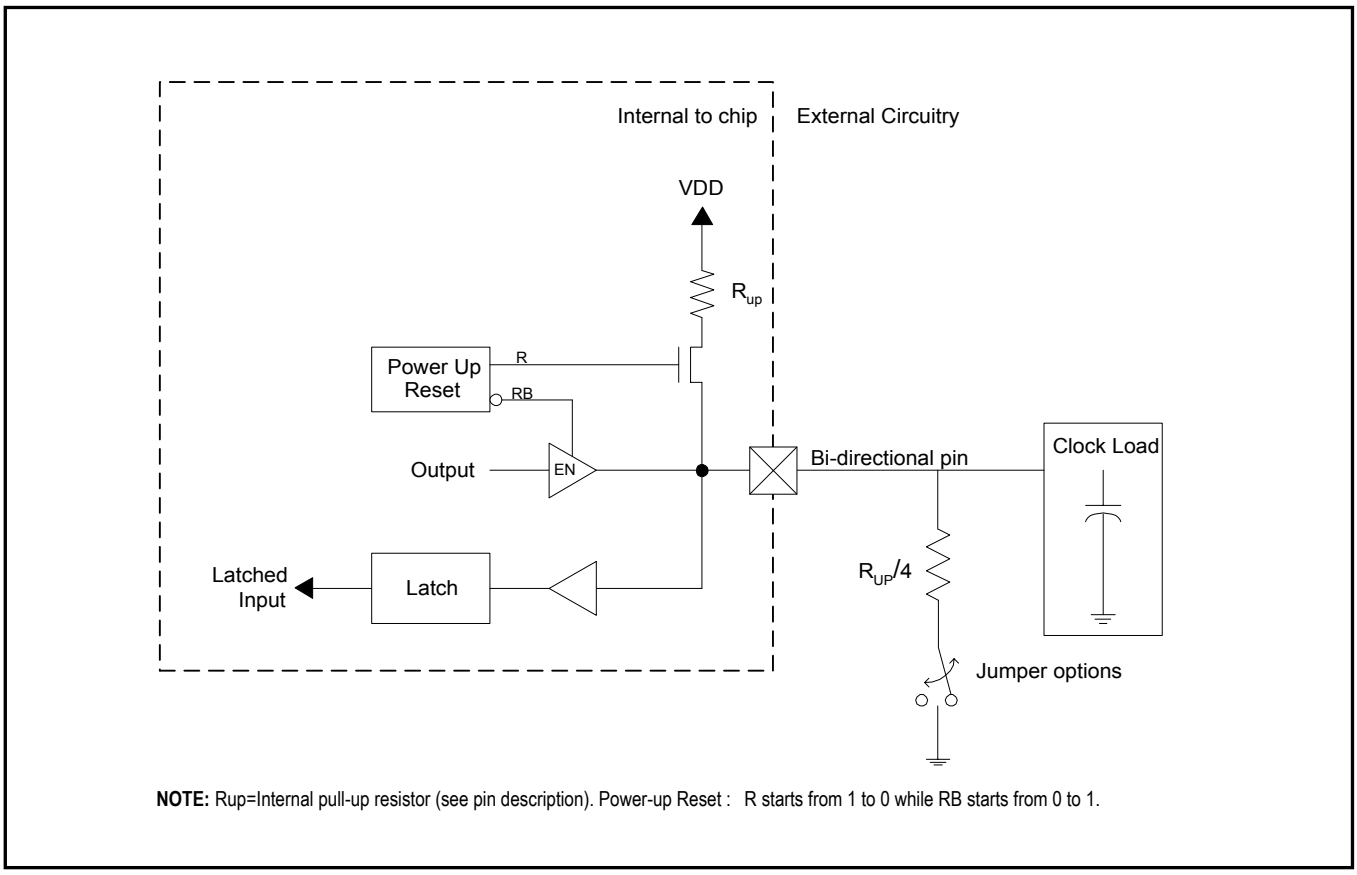
SPREAD SPECTRUM SELECTION TABLE

SS1	SS0	Spread Spectrum Modulation
0	0	OFF
0	1	- 0.50% – Down Spread
1	0	- 1.00% – Down Spread
1	1	- 1.25% – Down Spread

FUNCTIONAL DESCRIPTION

Tri-level and two-level inputs

In order to reduce pin usage, the PLL702-06 uses tri-level input pins. These pins allow 3 levels for input selection: namely, 0 = Connect to GND, 1 = Connect to VDD, M = Do not connect. Thus, unlike the two-level selection pins, the tri-level input pins are in the "M" (mid) state when not connected. In order to connect a tri-level pin to a logical "zero", the pin must be connected to GND. Likewise, in order to connect to a logical "one", the pin must be connected to VDD.



BI-DIRECTIONAL PINS WITH INTERNAL PULL-UP

Connecting a bi-directional pin

The PLL702-06 also uses bi-directional pins. The same pin serves as input upon power-up, and as output as soon as the inputs have been latched. The value of the input is latched-in upon power-up. Depending on the pin (see pin description), the input can be tri-level or a standard two-level. Unlike unidirectional pins, bi-directional pins cannot be connected directly to GND or VDD in order to set the input to "0" or "1", since the pin also needs to serve as output. In the case of two level input pins, an internal pull-up resistor is present. This allows a default value to be set when no external pull down resistor is connected between the pin and GND (by definition, a tri-level input has a default value of "M" (mid) if it is not connected). In order to connect a bi-directional pin to a non-default value, the input must be connected to GND or VDD through an external pull-down/pull-up resistor.

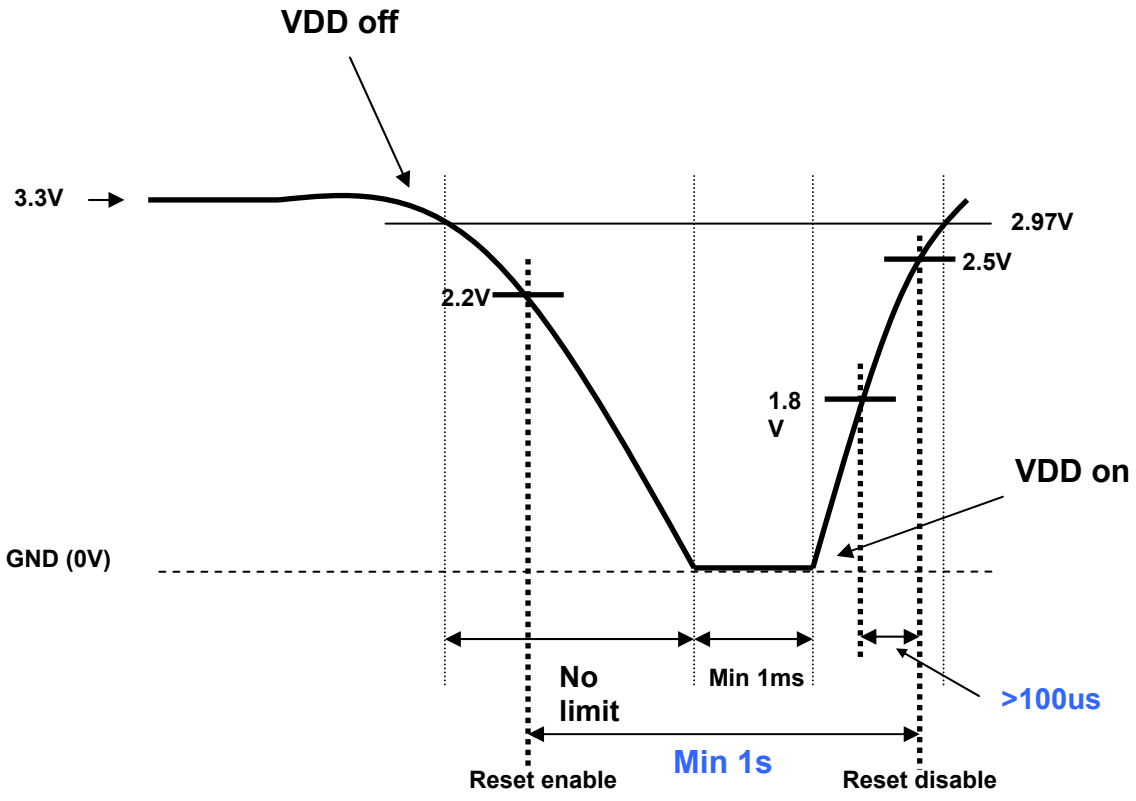
Note: *when the output load presents a low impedance in comparison to the internal pull-up resistor, the internal pull-up resistor may not be sufficient to pull the input up to a logical "one", and an external pull-up resistor may be required.*

For bi-directional inputs, the external loading resistor between the pin and GND has to be sufficiently small (compared to the internal pull-up resistor) so that the pin voltage be pulled below 0.8V (logical "zero"). In order to avoid loading effects when the pin serves as output, the value of the external pull-down resistor should however be kept as large as possible. In general, it is recommended to use an external resistor of around one sixth to one quarter of the internal pull-up resistor (see Application Diagram).

VDD Power Up Ramp Requirements:

At startup, the chip reads a lot of settings for operation according to the application's requirements. Since reading the settings is done only at startup and then frozen for the time of operation, it is important that the power-up environment is somewhat controlled to facilitate proper reading of the settings. The important VDD pins are VDDA (Pin3) and VDDD (Pin4) and they should apply to the following two-startup requirements:

- VDDD should be equally fast or slower than VDDA. VDDD performs a chip reset when VDD has reached a certain level and VDDA should have reached at least up to the same level as well to properly process the reset.
- The VDD Power Up Ramp of VDDD and VDDA should pass through the section 1.8V to 2.5V no faster than **100µs** and with a continuously increasing slope. In this section the tri-level select inputs are read.
- After VDD Power off, VDD should be allowed to go to 0V and stay there for at least **1ms** before a new VDD Power on. It is important that proper preconditions exist at every startup. Remaining charges in the chip or in circuit filter capacitors may interfere with the preconditions so it is important that VDD has been at 0V for some time before each startup.



Electrical Specifications

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	0	70	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. AC Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Input Frequency			14.31818		MHz
SST modulation sweep rate			28		kHz
Output Rise Time	0.8V to 2.0V with no load			1.5	ns
Output Fall Time	2.0V to 0.8V with no load			1.5	ns
Duty Cycle	At VDD/2	45	50	55	%
Max. Absolute Period Jitter	Long term, No SST			180	ps
Max. Jitter, cycle to cycle	Long term + Short term			150	ps

3. DC Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	VDDA VDDD	Nominal voltage is 3.3V	2.97		3.63	V
	VDDUSB VDDCPU	Nominal voltage is 2.5V	2.25		2.75	V
		Nominal voltage is 3.3V	2.97		3.63	V
Input High Voltage	V_{IH}			VDD/2		V
Input Low Voltage	V_{IL}			VDD/2	VDD/2 - 1	V
Input High Voltage	V_{IH}	For all Tri-level input	VDD-0.5			V
Input Low Voltage	V_{IL}	For all Tri-level input			0.5	V
Input High Voltage	V_{IH}	For all normal input	2			V
Input Low Voltage	V_{IL}	For all normal input			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25mA VDD = 3.3V	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25mA			0.4	V
Output High Voltage At CMOS Level	V_{OH}	I_{OH} = -8mA	VDD-0.4			V
Nominal Output Current	I_{out}		25			mA
Operating Supply Current	I_{DD}	No Load		30		mA
Short-circuit Current	I_S			±100		mA

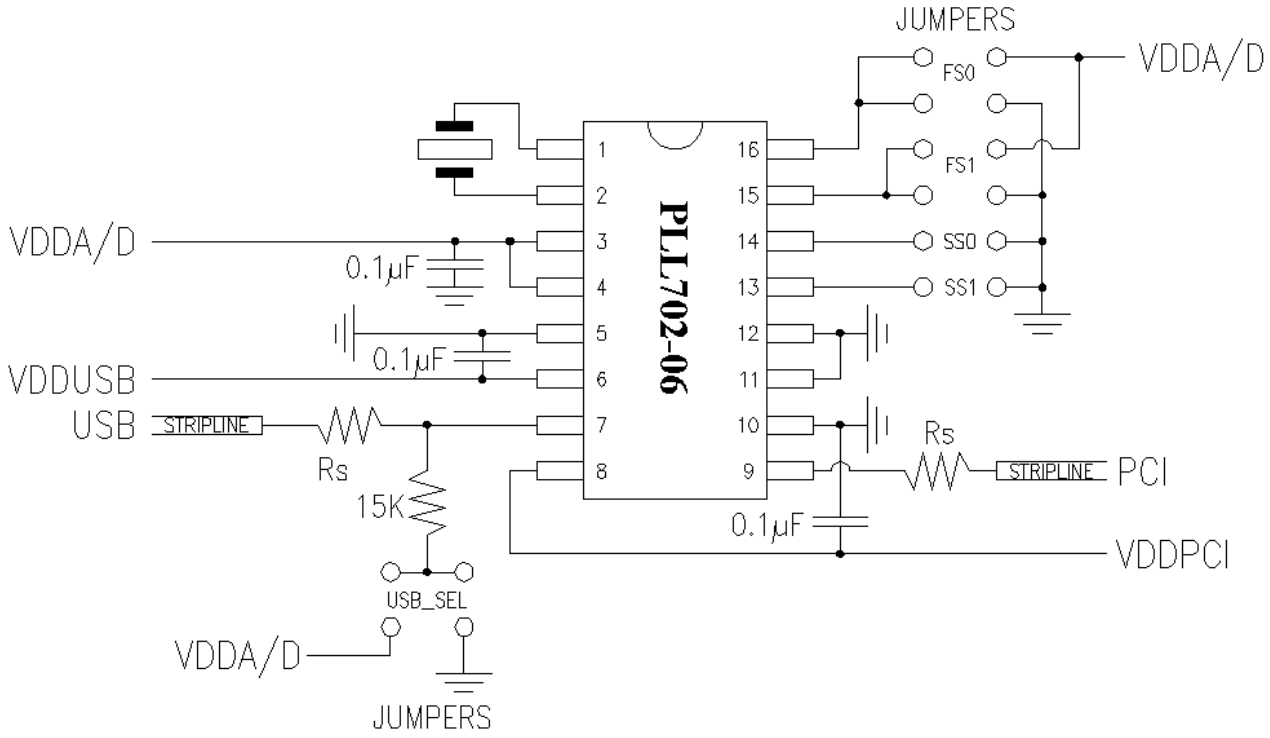
4. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode		14.31818		MHz
Crystal Loading Rating	$C_{L\ (xtal)}$			21		pF
Recommended ESR	R_E	AT cut			30	Ω

Note: A detailed crystal specification document is also available for this part.

LAYOUT RECOMMENDATION

The following is the recommended layout for PhaseLink's PLL702-06 in 16-pin SOIC package.



PCB LAYOUT CONSIDERATIONS FOR PERFORMANCE OPTIMIZATION

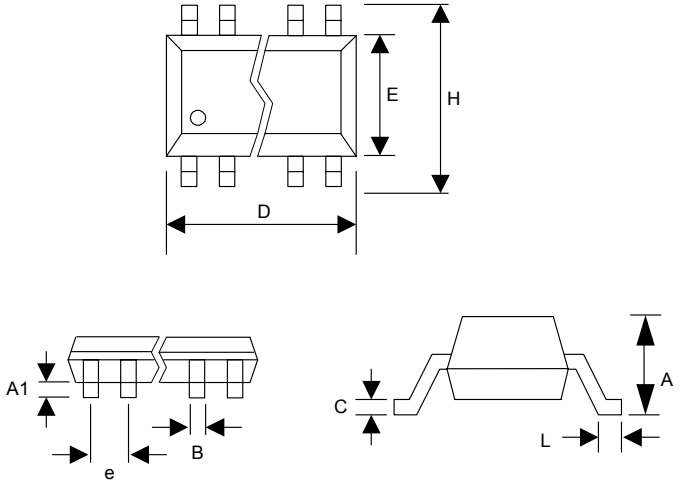
The following guidelines are to assist you with a performance optimized PCB design:

- Keep all the PCB traces to PL702-06 as short as possible, as well as keeping all other traces as far away from it as possible.
- Place the crystal as close as possible to both crystal pins of the device. This will reduce the cross-talk between the crystal and the other signals.
- Separate crystal pin traces from the other signals on the PCB, but allow ample distance between the two crystal pin traces.
- Place 0.01µF~0.1µF decoupling capacitors between VDDs and GNDs (see above diagram), on the component side of the PCB, close to the VDD pins. It is not recommended to place these components on the backside of the PCB. Going through vias will reduce the signal integrity, causing additional jitter and phase noise.
- It is highly recommended to keep the VDD and GND traces as short as possible.
- When connecting long traces (> 1 inch) to a CMOS output, it is important to design the traces as a transmission line or 'stripline', to avoid reflections or ringing. In this case, the CMOS output needs to be matched to the trace impedance. Usually 'striplines' are designed for 50Ω impedance and CMOS outputs usually have lower than 50Ω impedance so matching can be achieved by adding a resistor in series with the CMOS output pin to the 'stripline' trace.
- Please contact PhaseLink for the application note on how to design outputs driving long traces or the Gerber files for the PL702-06 layout.
- Please contact PhaseLink for a detailed crystal spec.

PACKAGE INFORMATION

16 PIN Narrow SOIC (mm)

	SOIC	
Symbol	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
H	5.80	6.20
L	0.40	1.27
e	1.27 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL702-06 X X X X

PART NUMBER

NONE= TUBE
R= TAPE AND REEL

NONE= NORMAL PACKAGE
L= GREEN PACKAGE

PACKAGE TYPE
S=SOP

TEMPERATURE
C=COMMERCIAL

Part / Order Number	Marking	Package Option	Temperature
PLL702-06SC-R	P702-06SC	SOP -Tape and Reel	0 to +70° C
PLL702-06SC	P702-06SC	SOP -Tubes	0 to +70° C
PLL702-06SCL-R	P702-06SCL	SOP -Tape and Reel Green	0 to +70° C
PLL702-06SCL	P702-06SCL	SOP –Tubes Green	0 to +70° C