PRELIMINARY

SFF1310M
SFF1310Z

SOLID STATE DEVICES, INC.
14830 Valley View Av. * La Mirada, Ca 90670
Phone: (562) 404-7855 * Fax: (562) 404-1773

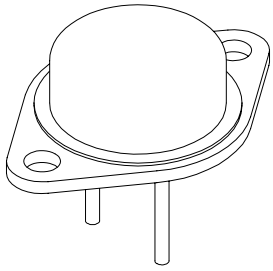
DESIGNER'S DATA SHEET

40 AMPS
200 VOLTS
0.050 Ω
N-CHANNEL
POWER MOSFET

FEATURES:

- Rugged construction with polysilicon gate
- Low RDS (on) and high transconductance
- Excellent high temperature stability
- Very fast switching speed
- Fast recovery and superior dv/dt performance
- Increased reverse energy capability
- Low input and transfer capacitance for easy paralleling
- Hermetically sealed package
- TX, TXV, and Space Level screening available
- Replaces: SMM40N20 Type

TO-3



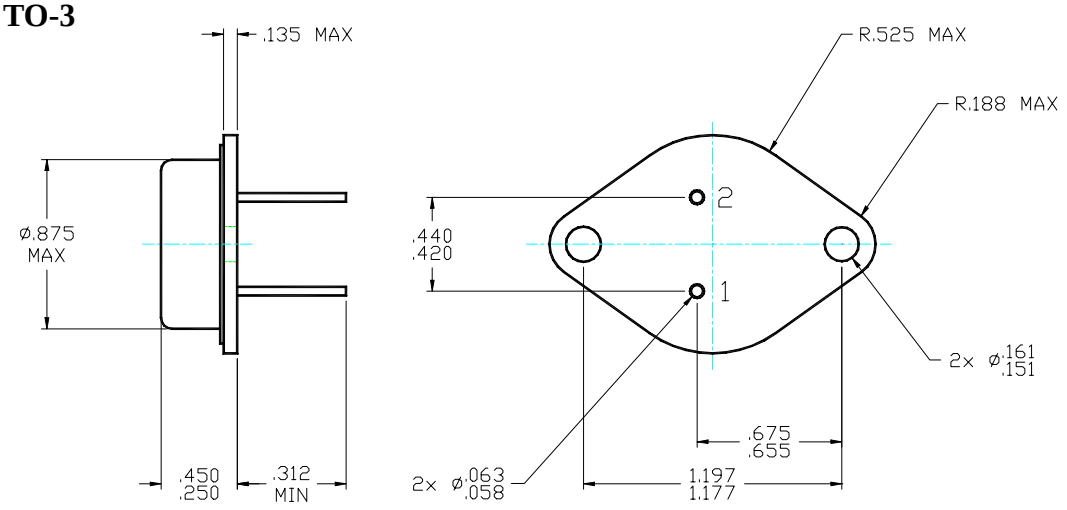
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V_{DS}	200	Volts
Gate to Source Voltage	V_{GS}	±20	Volts
Continuous Drain Current	I_D	40	Amps
Operating and Storage Temperature	T_{op} & T_{stg}	-55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.5	°C/W
Total Device Dissipation @ TC = 25°C @ TC = 55°C	P_D	250 190	Watts

PACKAGE OUTLINE: TO-3

PIN OUT:

DRAIN: **PIN 1**
SOURCE: **PIN 2**
GATE: **PIN 3**



NOTE: All specifications are subject to change without notification.
SCDs for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0004A

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ELECTRICAL CHARACTERISTICS @ T_J =25°C (Unless Otherwise Specified)

RATING		SYMBOL	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage (VGS =0 V, ID =250µA)		BV_{DSS}	200	-	-	V
Drain to Source ON State Resistance I_D = 37.5A (VGS = 10 V, 60% of Rated ID)		$R_{DS(on)}$	- -	- -	0.050	Ω
ON State Drain Current (VDS > ID(on) x RDS(on) Max, VGS = 10 V)		$I_{D(on)}$	50	-	-	A
Gate Threshold Voltage (VDS =VGS, ID = 4mA)		$V_{GS(th)}$	2.0	-	4.0	V
Forward Transconductance (VDS > ID(on) x RDS (on) Max, IDS = 50% rated ID)		g_{fs}	20	25	-	S(℧)
Zero Gate Voltage Drain Current (V_{GS} = 0V)	V_{DS} = max rated Voltage, T_A = 25°C V_{DS} = 80% rated V_{DS}, T_A = 125°C	I_{DSS}	- -	- -	250 1000	µA
Gate to Source Leakage Forward **Gate to Source Leakage Reverse**	At rated VGS	I_{GSS}	- -	- -	+100 -100	nA
Total Gate Charge **Gate to Source Charge** **Gate to Drain Charge**	VGS = 10 V 50% rated VDS 50% rated ID	**Qg** **Qgs** **Qgd**	- - -	190 35 95	220 50 120	nC
Turn on Delay Time **Rise Time** **Turn off DELAY Time** **Fall Time**	VDD =50% rated VDS 50% rated ID RG = 6.2 Ω	$t_{d(on)}$ **tr** $t_{d(off)}$ **tf**	- - - -	28 38 110 30	35 40 130 35	nsec
Diode Forvard Voltage (I_S = rated I_D, V_{GS} = 0V, T_J = 25°C)		V_{SD}	-	-	1.50	V
Diode Reverse Recovery Time **Reverse Recovery Charge**	T_J =25°C IF = 10A di/dt = 100A/µsec	t_{rr} Q_{RR}	- -	- 1.5	225 -	nsec µC
Input Capacitance **Output Capacitance** **Reverse Transfer Capacitance**	VGS =0 Volts VDS =25 Volts f =1 MHz	**Ciss** **Coss** **Crss**	- - -	4400 800 285	- - -	pF

NOTES: