



SOLID STATE DEVICES, INC.

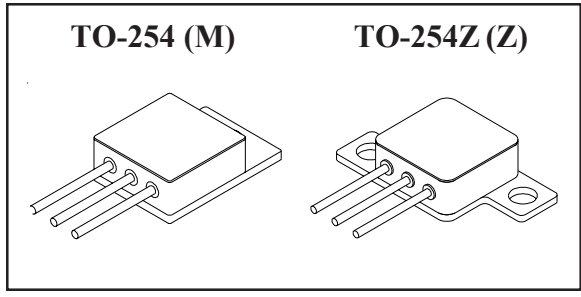
14701 Firestone Blvd * La Mirada, Ca 90638
 Phone: (562) 404-7855 * Fax: (562) 404-1773

DESIGNER'S DATA SHEET

- FEATURES:**
- Rugged construction with poly silicon gate
 - low RDS (on) and high transconductance
 - Excellent high temperature stability
 - Very fast switching speed
 - Fast recovery and superior dv/dt performance
 - Increased reverse energy capability
 - Low input and transfer capacitance for easy paralleling
 - Ceramic seals for improved hermeticity
 - Hermetically sealed package
 - TX, TXV and Space Level screening available
 - Replaces: IXTH75N10 Types

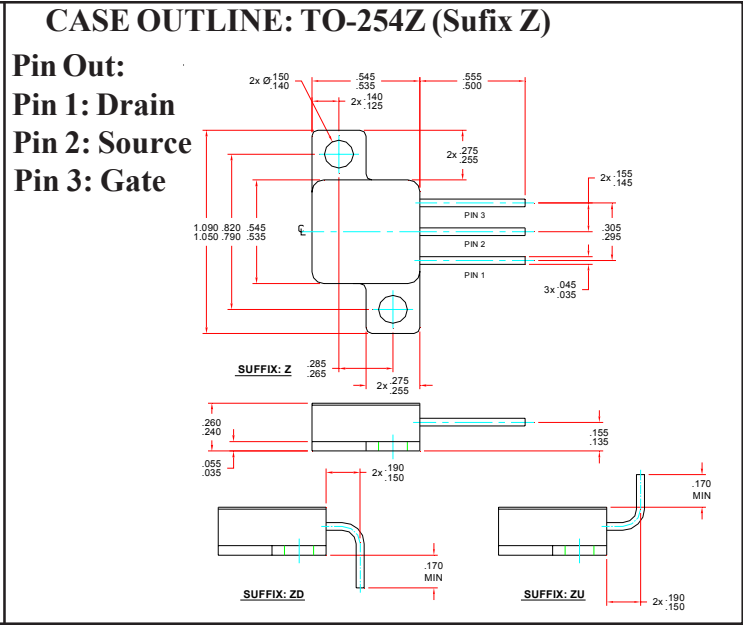
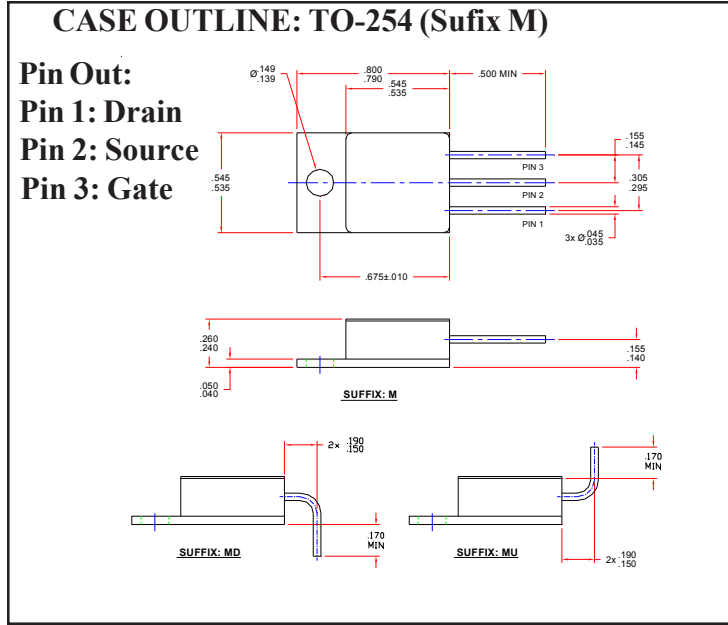
SFF75N10M
SFF75N10Z

75 AMP
100 VOLTS
0.025 Ω
N-CHANNEL
POWER MOSFET



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Drain to Source Voltage	V _{DS}	100	Volts
Gate to Source Voltage	V _{GS}	± 20	Volts
Continuous Drain Current	I _D	56 ^L	Amps
Operating and Storage Temperature	T _{op} & T _{stg}	-55 to +150	°C
Thermal Resistance, Junction to Case	R _{θJC}	0.83	°C/W
Total Device Dissipation	P _D	@ TC = 25°C	150
		@ TC = 55°C	114
Repetitive Avalanche Energy	E _{AR}	30	mJ



Available with Glass or Ceramic Seals. Contact Factory for details.

NOTE: All specifications are subject to change without notification. SCDs for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: F00153F

SFF75N10M
SFF75N10Z



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ELECTRICAL CHARACTERISTICS @ T_J = 25°C (Unless Otherwise Specified)

RATING	SYMBOL	MIN	TYP	MAX	UNIT	
Drain to Source Breakdown Voltage (V _{GS} = 0 V, I _D = 250 μA)	BV_{DSS}	100	-	-	V	
Drain to Source on State Resistance (V _{GS} = 10 V)	R_{DS(on)}	-	-	0.025 0.030	Ω	
On State Drain Current (V _{DS} > I _{D(on)} x R _{DS(on)} Max, V _{GS} = 10 V)	I_{D(on)}	75	-	-	A	
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 4mA)	V_{GS(th)}	2	-	4.0	V	
Forward Transconductance (V _{DS} > I _{D(on)} X R _{DS} (on) Max, I _{DS} = 50% rated I _D)	g_{fs}	25	30	-	Smho	
Zero Gate Voltage Drain Current (V _{DS} = max rated voltage, V _{GS} = 0 V) (V _{DS} = 80% rated V _{DS} , V _{GS} = 0V, T _A = 125°C)	I_{DSS}	-	-	250 1000	μA	
Gate to Source Leakage Forward Gate to Source Leakage Reverse	At rated V _{GS}	I_{GSS}	-	-	+200 -200	nA
Total Gate Charge Gate to Source Charge Gate to Drain Charge	V _{GS} = 10 V 50% rated V _{DS} 50% rated I _D	Q_g Q_{gs} Q_{gd}	-	160 16 50	260 70 160	nC
Turn on Delay Time Rise Time Turn off Delay Time Fall Time	V _{DD} = 50% rated V _{DS} 50% rated I _D R _G = 6.2Ω V _{GS} = 10V	t_d (on) tr t_d (off) tf	-	30 35 100 40	40 100 120 80	nsec
Diode Forward Voltage (I _S = rated I _D , V _{GS} = 0V, T _J = 25°C)	V_{SD}	-	1.3	1.75	V	
Diode Reverse Recovery Time Reverse Recovery Charge	T _J = 25°C I _F = 10A di/dt = 100A/μsec	t_{rr} Q_{RR}	-	120 -	200 -	nsec
Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{GS} = 0 Volts V _{DS} = 25 Volts f = 1 MHz	C_{iss} C_{oss} C_{rss}	-	4500 1600 800	- - -	pF

NOTES:

1/ Maximum current limited by package, die rated at 75A.

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