

OVERVIEW

The SM5865BM is a 24-bit input D/A converter for digital audio equipment. It comprises newly developed DEM (dynamic element matching) circuits, 3rd-order $\Sigma\Delta$ noise shaper and 23-level quantizer to control wide-band residual quantization noise in the signal band, making it ideal for application with high-frequency sampling formats. Also, the order of the required final-stage analog lowpass filter can be reduced, compared to filters for available devices, enhancing output tone quality. The output stage employs complementary outputs for high-accuracy analog signals, with appropriate lowpass filtering of the output signal.

A single SM5865BM IC can be used in combination with an 8-times oversampling digital filter for conversion for a single audio channel.

FEATURES

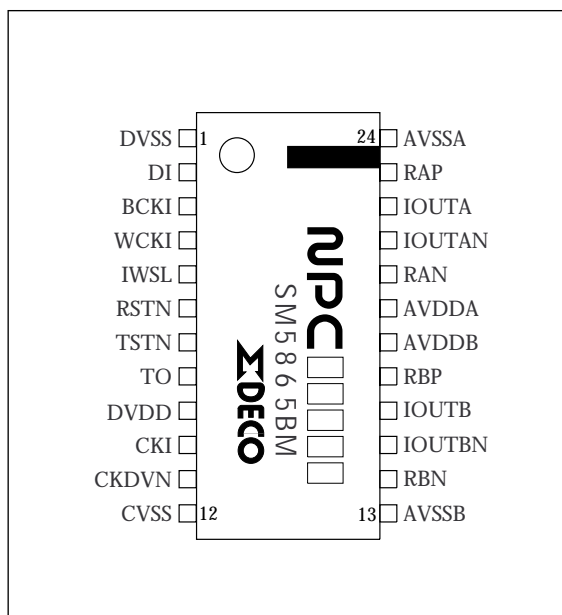
- Single-channel D/A converter built-in
- High performance
 - 0.0004% total harmonic distortion and noise
 - 114 dB dynamic range
 - 117 dB signal-to-noise ratio
- $\Sigma\Delta$ D/A converter
 - 3rd-order noise shaper
 - 23-level quantizer
- Input data format
 - 20 or 24-bit word length
 - MSB first, right-justified format
 - 8 or 4 times oversampling at $f_s = 16/32/44.1/48/88.2/96/176.4/192$ kHz
- System clock frequency
 - 192/256/384/512/768/1024 fs
- Single 5 V operating supply voltage
- 24-pin SSOP package
- Molybdenum-gate CMOS process

ORDERING INFORMATION

Device	Package
SM5865BM	24-pin SSOP

PINOUT

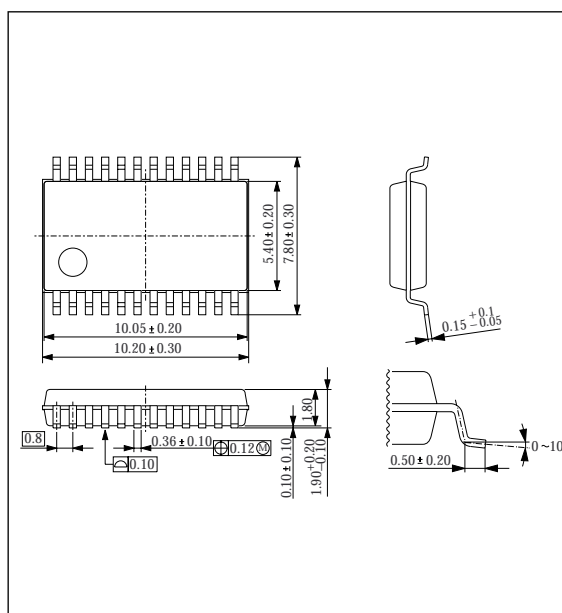
(Top view)



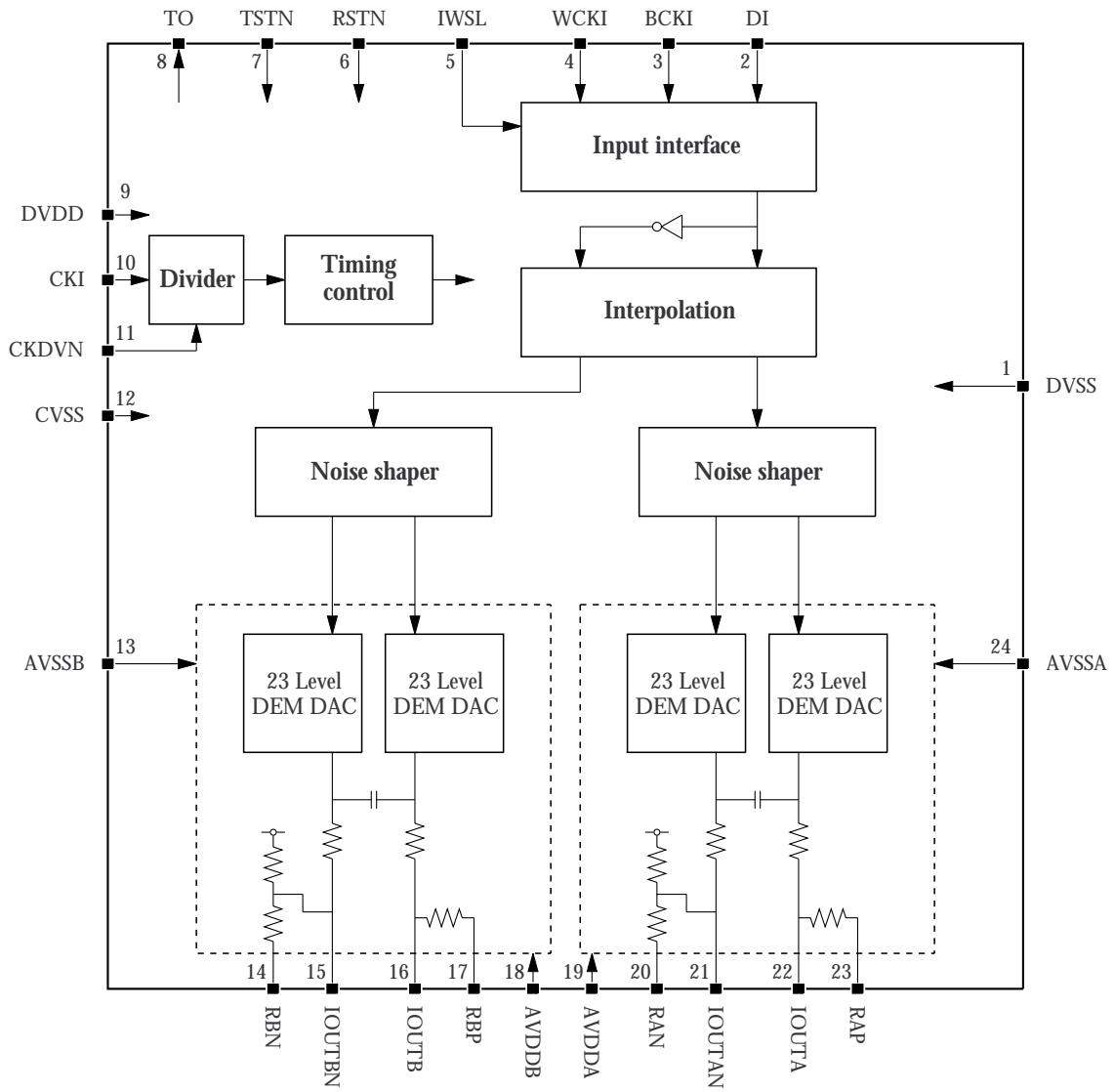
PACKAGE DIMENSIONS

(Unit: mm)

24-pin SSOP



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	DVSS	-	Digital ground
2	DI	I	Data input
3	BCKI	I	Bit clock input
4	WCKI	I	Word clock input
5	IWSL	I _p	Input data word length select. 24-bit when HIGH, and 20-bit when LOW.
6	RSTN	I _p	System reset. Reset when LOW.
7	TSTN	I _p	Test pin. Tie HIGH or leave open for normal operation.
8	TO	O	Test output
9	DVDD	-	Digital supply
10	CKI	I	System clock input
11	CKDVN	I _p	System clock frequency divider ratio select. 1 when HIGH (no division), and 2 when LOW.
12	CVSS	-	System clock ground
13	AVSSB	-	Analog ground B
14	RBN	I	Built-in resistor connection B
15	IOUTBN	O	Inverse-phase analog output B
16	IOUTB	O	In-phase analog output B
17	RBP	I	Built-in resistor connection B
18	AVDDB	-	Analog supply B
19	AVDDA	-	Analog supply A
20	RAN	I	Built-in resistor connection A
21	IOUTAN	O	Inverse-phase analog output A
22	IOUTA	O	In-phase analog output A
23	RAP	I	Built-in resistor connection A
24	AVSSA	-	Analog ground A

I_p : Pull-up input

SPECIFICATIONS

Absolute Maximum Ratings

$$DV_{SS} = AV_{SSA} = AV_{SSB} = CV_{SS} = 0 \text{ V}, DV_{DD} = AV_{DDA} = AV_{DDB}$$

Parameter	Symbol	Rating	Unit
Supply voltage range	$DV_{DD}, AV_{DDA}, AV_{DDB}$	-0.3 to 7.0	V
Input voltage range ¹	V_{IN}	$DV_{SS} - 0.3$ to $DV_{DD} + 0.3$	V
Storage temperature range	T_{stg}	-55 to 125	°C
Power dissipation	P_D	250	mW

1. Pins DI, BCKI, WCKI, CKDVN, IWSL, RSTN, TSTN.

Also applicable during supply switching.

Recommended Operating Conditions

$$DV_{SS} = AV_{SSA} = AV_{SSB} = CV_{SS} = 0 \text{ V}, DV_{DD} = AV_{DDA} = AV_{DDB}$$

Parameter	Symbol	Rating	Unit
Supply voltage range	$DV_{DD}, AV_{DDA}, AV_{DDB}$	4.5 to 5.5	V
Supply voltage variation	$DV_{DD} - AV_{DDA},$ $DV_{DD} - AV_{DDB},$ $AV_{DDA} - AV_{DDB},$ $DV_{SS} - AV_{SSA},$ $DV_{SS} - AV_{SSB},$ $AV_{SSA} - AV_{SSB},$ $DV_{SS} - CV_{SS},$ $AV_{SSA} - CV_{SS},$ $AV_{SSB} - CV_{SS}$	±0.1	V
Operating temperature range	T_{opr}	-40 to 85	°C

DC Electrical Characteristics

Recommended operating conditions, unless otherwise specified.

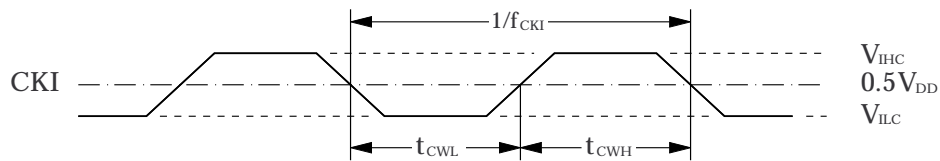
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DVDD, AVDDA, AVDDB supply current ¹	I _{DD}	f _{CKI} = 11.2896 MHz	-	6	10	mA
		f _{CKI} = 16.9344 MHz	-	9	13	mA
		f _{CKI} = 24.576 MHz	-	12	16	mA
		f _{CKI} = 36.864 MHz	-	18	23	mA
CKI HIGH-level input voltage	V _{IHC}		0.7V _{DD}	-	-	V
CKI LOW-level input voltage	V _{ILC}		-	-	0.3V _{DD}	V
CKI input voltage	V _{INAC}	AC coupling	1.0	-	-	Vp-p
HIGH-level input voltage ²	V _{IH}		2.4	-	-	V
LOW-level input voltage ²	V _{IL}		-	-	0.5	V
HIGH-level output voltage ³	V _{OH}	I _{OH} = -1 mA	DV _{DD} - 0.4	-	-	V
LOW-level output voltage ³	V _{OL}	I _{OL} = 1 mA	-	-	0.4	V
CKI HIGH-level input current	I _{IHC}	V _{IN} = DV _{DD}	30	60	120	μA
CKI LOW-level input current	I _{ILC}	V _{IN} = 0 V	30	60	120	μA
LOW-level input current ⁴	I _{IL2}	V _{IN} = 0 V	-	9	18	μA
HIGH-level input leakage current ⁵	I _{IH1}	V _{IN} = DV _{DD}	-	-	1.0	μA
LOW-level input leakage current ⁵	I _{IL1}	V _{IN} = 0 V	-	-	1.0	μA
HIGH-level input leakage current ⁶	I _{IH2}	V _{IN} = DV _{DD}	-	-	1.0	μA

1. No output load, NPC-standard input data pattern.
2. Pins DI, BCKI, WCKI, CKDVN, IWSL, RSTN, TSTN.
3. Pin TO.
4. Pins CKDVN, IWSL, RSTN, TSTN.
5. Pins DI, BCKI, WCKI.
6. Pins CKDVN, IWSL, RSTN, TSTN.

AC Electrical Characteristics

System clock Input (CKI)

Parameter	Symbol	Rating			Unit
		min	typ	max	
CKI clock frequency	f_{CKI}	5	-	60	MHz
HIGH-level clock pulsewidth	t_{CWH}	5	-	-	ns
LOW-level clock pulsewidth	t_{CWL}	5	-	-	ns



Internal System Clock

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Internal system clock frequency	f_{SYS}		5	-	46	MHz

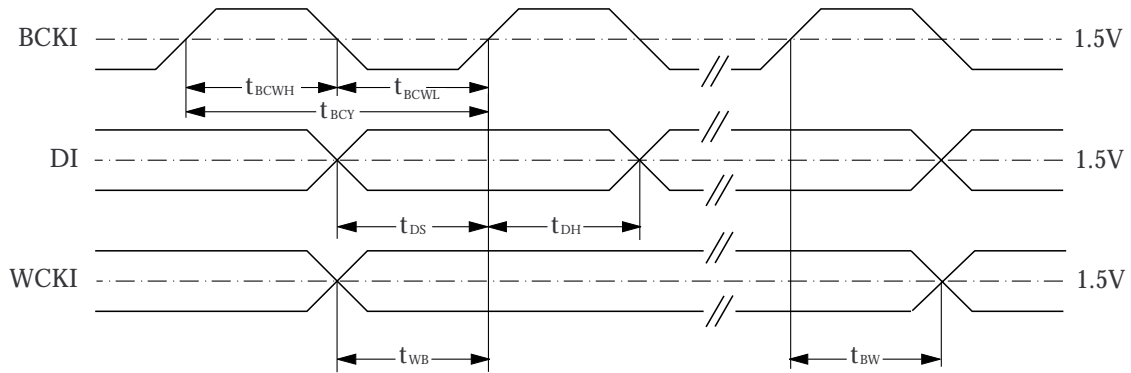
Internal system clock frequency is the same as the CKI clock frequency when CKDVN = HIGH.
Internal system clock frequency is half the CKI clock frequency when CKDVN = LOW.

Reset Input (RSTN)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
RSTN LOW-level pulsewidth	t_{RSTN}	At power ON	1	-	-	μs
		After power ON	100	-	-	ns

Serial input (BCKI, DI, WCKI)

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH}	10	-	-	ns
BCKI LOW-level pulsewidth	t_{BCWL}	10	-	-	ns
BCKI pulse cycle	t_{BCY}	22	-	-	ns
DI setup time	t_{DS}	5	-	-	ns
DI hold time	t_{DH}	5	-	-	ns
WCKI edge to first BCKI rising edge	t_{WB}	10	-	-	ns
Last BCKI rising edge to WCKI edge	t_{BW}	10	-	-	ns



AC Analog Characteristics

Measurement Conditions

External 8fs digital filter	:	NPC SM5847AF
External operational amplifier	:	JRC NJM5534D
Supply voltage SM5865BM	:	$DV_{DD} = AV_{DDA} = AV_{DDB} = 5V, DV_{SS} = AV_{SSA} = AV_{SSB} = CV_{SS} = 0V$
SM5847AF	:	+3V
NJM5534D	:	$\pm 15V$
Ambient temperature	:	25 °C
Input data of SM5847AF	:	48kHz sampling (fs), 24-bit data
System clock	:	24.576MHz (512fs)
Noise shaper operating rate	:	64fs
Audio analyzer	:	Audio Precision System Two (RMS mode)
Measurement filter condition	:	THD + N 22HzHPF, 20kHzLPF (FLP-A20K)
	:	D.R 22HzHPF, 22kHzLPF, A-weight (FIL-AWT)
	:	S/N 22HzHPF, 22kHzLPF, A-weight (FIL-AWT)
Measurement circuits diagram	:	See next page.

Analog Characteristics

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Output level ¹	V_{out}	1 kHz, 0 dB	1.22	1.27	1.32	Vrms
Total harmonic distortion	THD + N	1 kHz, 0 dB	-	0.0004 (-108dB)	0.0009 (-101dB)	%
Dynamic range	D.R	1 kHz, -60 dB	108	114	-	dB
Signal-to-noise ratio	S/N	1 kHz, 0/-∞ dB	114	117	-	dB
Gain drift	G.D		-	10	-	ppm/°C

1. V_{OUT} is the output level of the first I-V conversion stage.

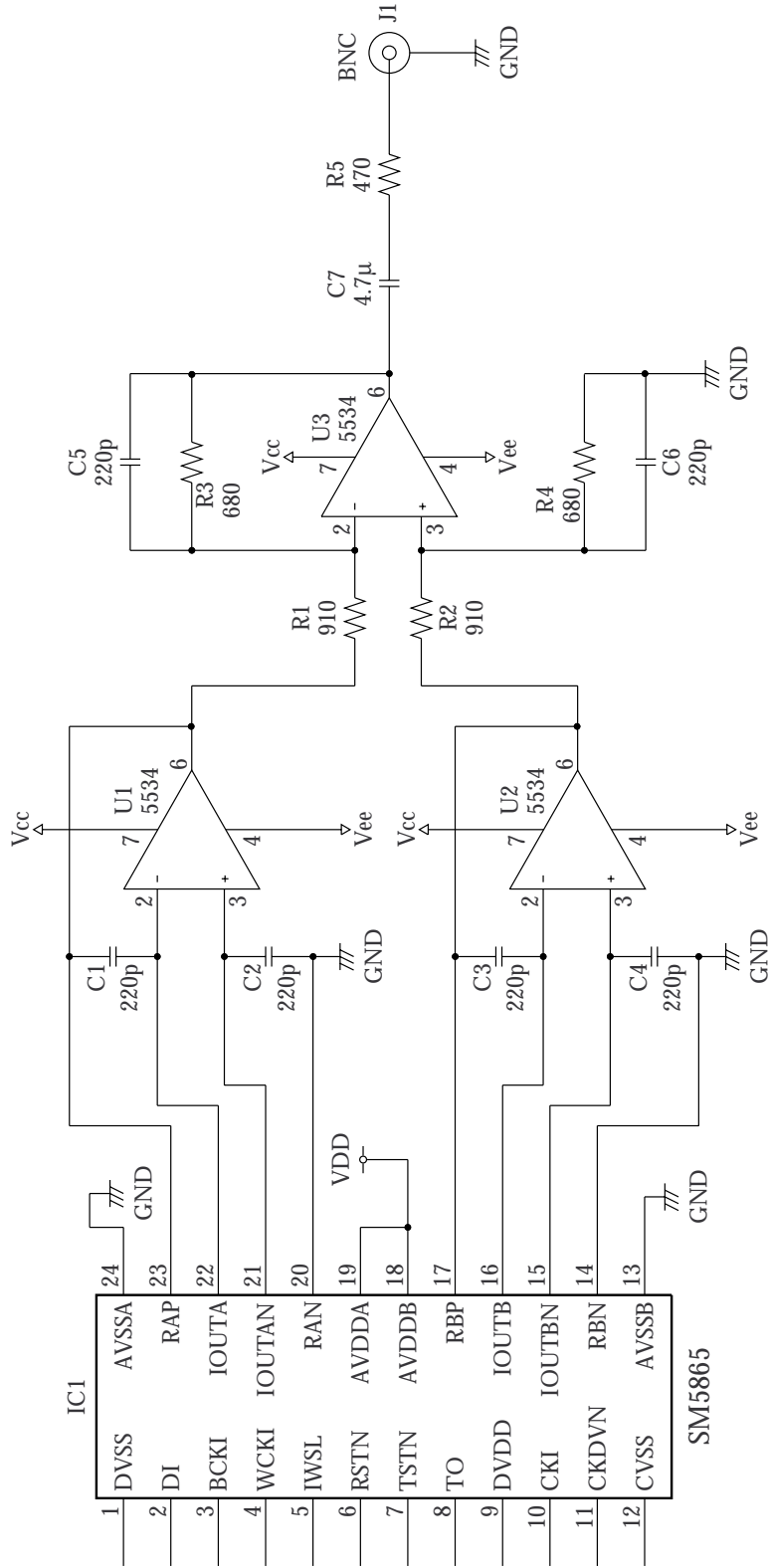
Group Delay

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Group delay ¹	T_{gd}		-	-	2/fsi	s

1. fsi is the input sampling rate of SM5865BM.

For example, fsi is 384kHz when this LSI is used in combination with an 8-times oversampling digital filter of which input sampling rate is 48kHz.

Measurement circuit



FUNCTIONAL DESCRIPTION

Quantization Noise Reduction

The SM5865BM employs a 3rd-order 23-level quantizer noise shaper to effectively reduce quantization noise in the audio band. The quantization noise component at 16fs to 96fs operation is shown in figure 1.

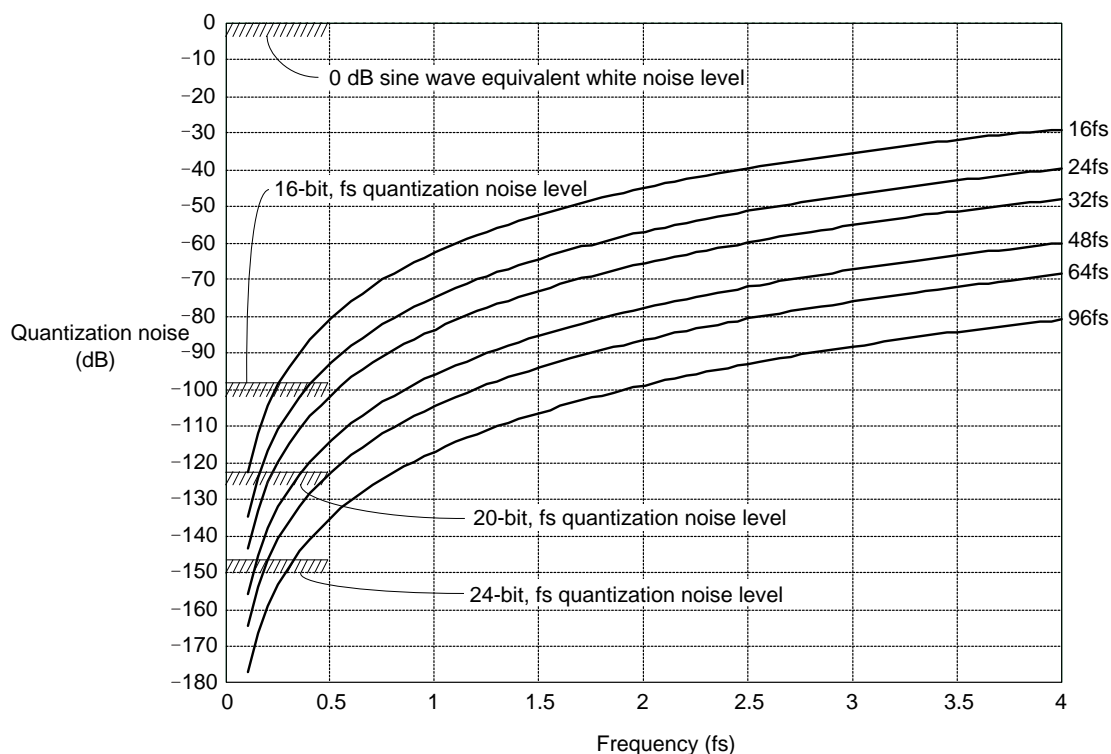


Figure 1. Quantization noise level

Internal Oversampling Operation

The SM5865BM accepts data output from an 8-times or 4-times oversampling digital filter, and oversampled internally again up to the noise shaper operating rate. The internal oversampling factor is determined automatically from the system clock input frequency and the input sampling frequency. This internal oversampling factor (n) must be an integer satisfying the conditions shown in table 1.

Table 1. Operating conditions

Parameter	CKDVN = HIGH	CKDVN = LOW
f_{WCKI} and f_{CKI} compulsory conditions ¹	$f_{CKI} = f_{WCKI} \times 8 \times n$ where $n = 1, 2, 3, \dots$	$f_{CKI} = f_{WCKI} \times 16 \times n$ where $n = 1, 2, 3, \dots$
Noise shaper operating frequency	$f_{ns} = f_{WCKI} \times n = \frac{f_{CKI}}{8}$	$f_{ns} = f_{WCKI} \times n = \frac{f_{CKI}}{16}$

1. f_{WCKI} = word clock frequency, f_{CKI} = input system clock frequency, n = internal oversampling factor

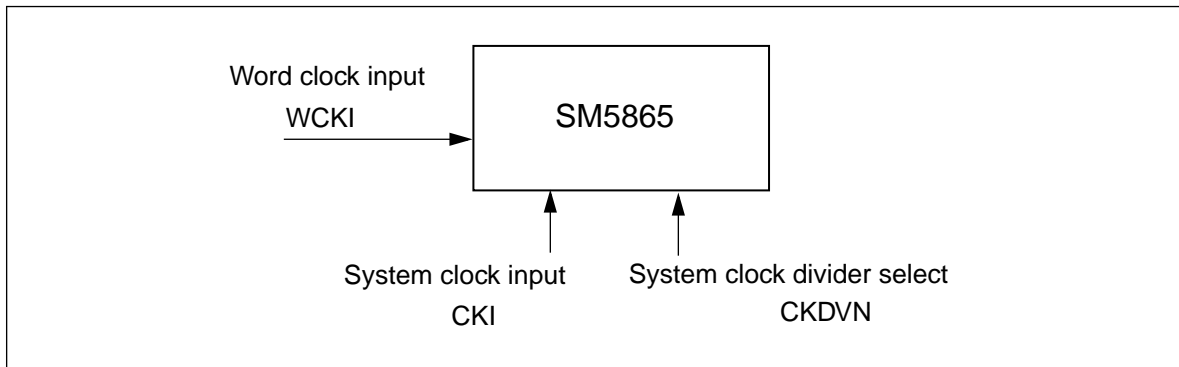


Figure 2. Clock-related inputs

Table 2 shows some possible combinations for the circuit configuration shown in figure 3.

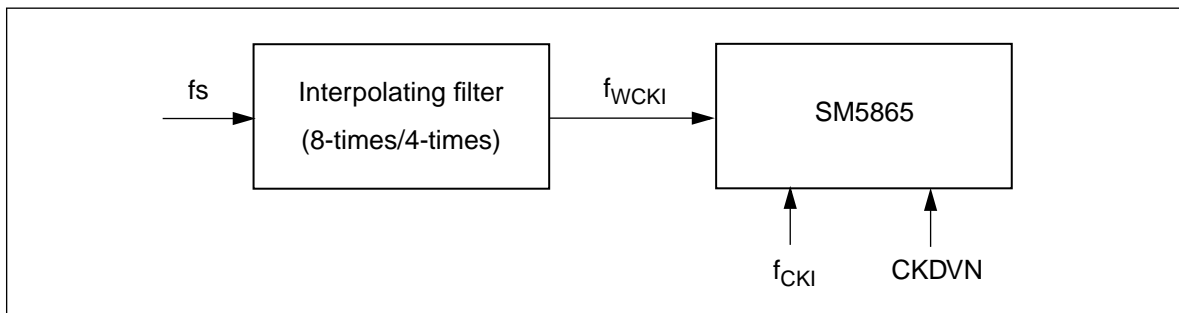


Figure 3. Circuit configuration

Table 2. System clock frequencies (CKDVN = HIGH)

fs	System clock frequency ¹ f _{CKI}	Noise shaper operating rate	Internal factor (8fs input)	Internal factor (4fs input)
16 kHz	6.144 MHz (384fs)	48fs	6	12
16 kHz	8.192 MHz (512fs)	64fs	8	16
16 kHz	12.288 MHz (768fs)	96fs	12	24
32 kHz	6.144 MHz (192fs)	24fs	3	6
32 kHz	8.192 MHz (256fs)	32fs	4	8
32 kHz	12.288 MHz (384fs)	48fs	6	12
32 kHz	16.384 MHz (512fs)	64fs	8	16
32 kHz	24.576 MHz (768fs)	96fs	12	24
44.1 kHz	8.4672 MHz (192fs)	24fs	3	6
44.1 kHz	11.2896 MHz (256fs)	32fs	4	8
44.1 kHz	16.9344 MHz (384fs)	48fs	6	12
44.1 kHz	22.5792 MHz (512fs)	64fs	8	16
44.1 kHz	33.8688 MHz (768fs)	96fs	12	24
48 kHz	9.216 MHz (192fs)	24fs	3	6
48 kHz	12.288 MHz (256fs)	32fs	4	8
48 kHz	18.432 MHz (384fs)	48fs	6	12
48 kHz	24.576 MHz (512fs)	64fs	8	16
48 kHz	36.864 MHz (768fs)	96fs	12	24

Table 2. System clock frequencies (CKDVN = HIGH)

fs	System clock frequency ¹ f _{CKI}	Noise shaper operating rate	Internal factor (8fs input)	Internal factor (4fs input)
88.2 kHz	16.9344 MHz (192fs)	24fs	3	6
88.2 kHz	22.5792 MHz (256fs)	32fs	4	8
88.2 kHz	33.8688 MHz (384fs)	48fs	6	12
88.2 kHz	45.1584 MHz (512fs)	64fs	8	16
96 kHz	18.432 MHz (192fs)	24fs	3	6
96 kHz	24.576 MHz (256fs)	32fs	4	8
96 kHz	36.864 MHz (384fs)	48fs	6	12
176.4 kHz	33.8688 MHz (192fs)	24fs	3	6
176.4 kHz	45.1584 MHz (256fs)	32fs	4	8
192 kHz	36.864 MHz (192fs)	24fs	3	6

1. When CKDVN = LOW, the system clock frequency f_{CKI} is halved, so the values shown are half the input frequency required for the same sampling rate and internal factors.

System Clock Divider (CKDVN)

The SM5865BM has a built-in divide-by-2 system clock frequency divider. The divider enables the internal system clock to operate at half the input frequency, for example when the external master clock input frequency is high.

System Reset (RSTN)

The device should be reset in the following cases.

- At power ON
- When the system clock CKI stops, or other abnormalities occur.

The device is reset by applying a LOW-level pulse on RSTN.

Audio Data Input (DI, BCKI, WCKI, IWSL)

Input data format

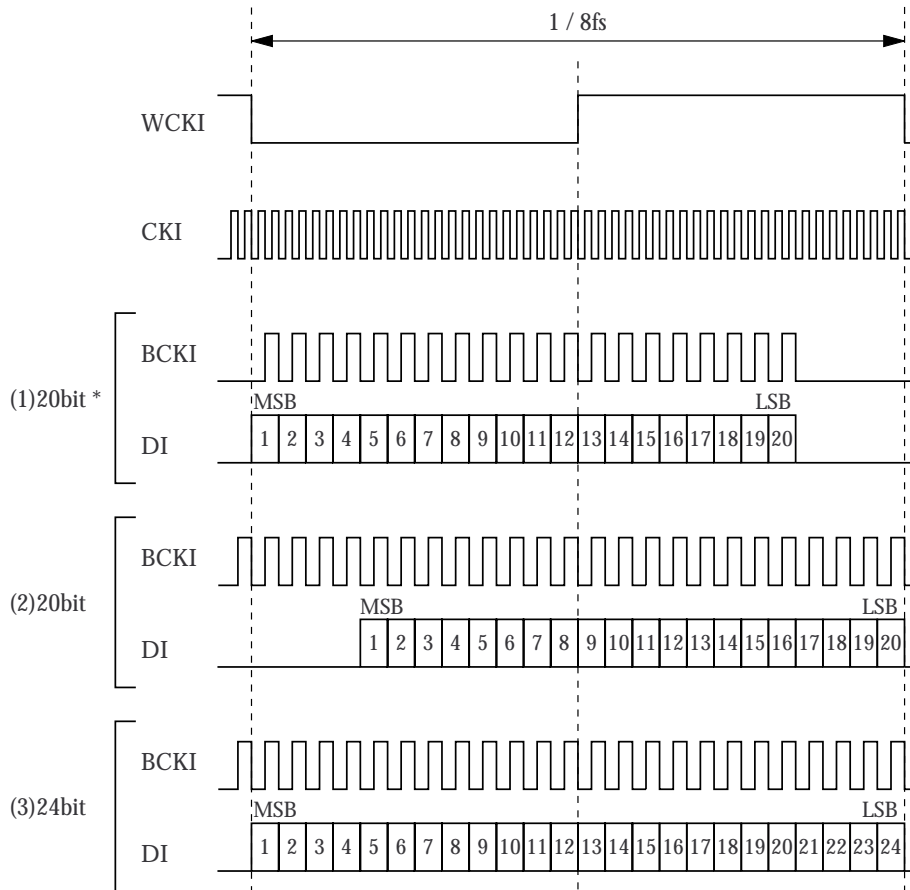
The audio data is input in MSB-first, 2s-complement, 24-bit/20-bit serial format. The input word bit length is selected by IWSL, 24-bit when HIGH or open circuit, and 20-bit when LOW.

Jitter-free function

Serial input data bits on DI are read into an SIPO register (serial-to-parallel converter register) on the rising edge of the bit clock BCKI where the serial data is converted into parallel data. The internal parallel data control timing is derived from the system clock, and is not affected by any jitter on the input data clocks (WCKI and BCKI). After a reset operation is released when RSTN goes HIGH, the internal timing and the WCKI input timing are phase compared on the first and subsequent WCKI falling edges and the comparison result is used to perform timing adjustment to maintain the word boundary relationship between the internal timing and the WCKI clock.

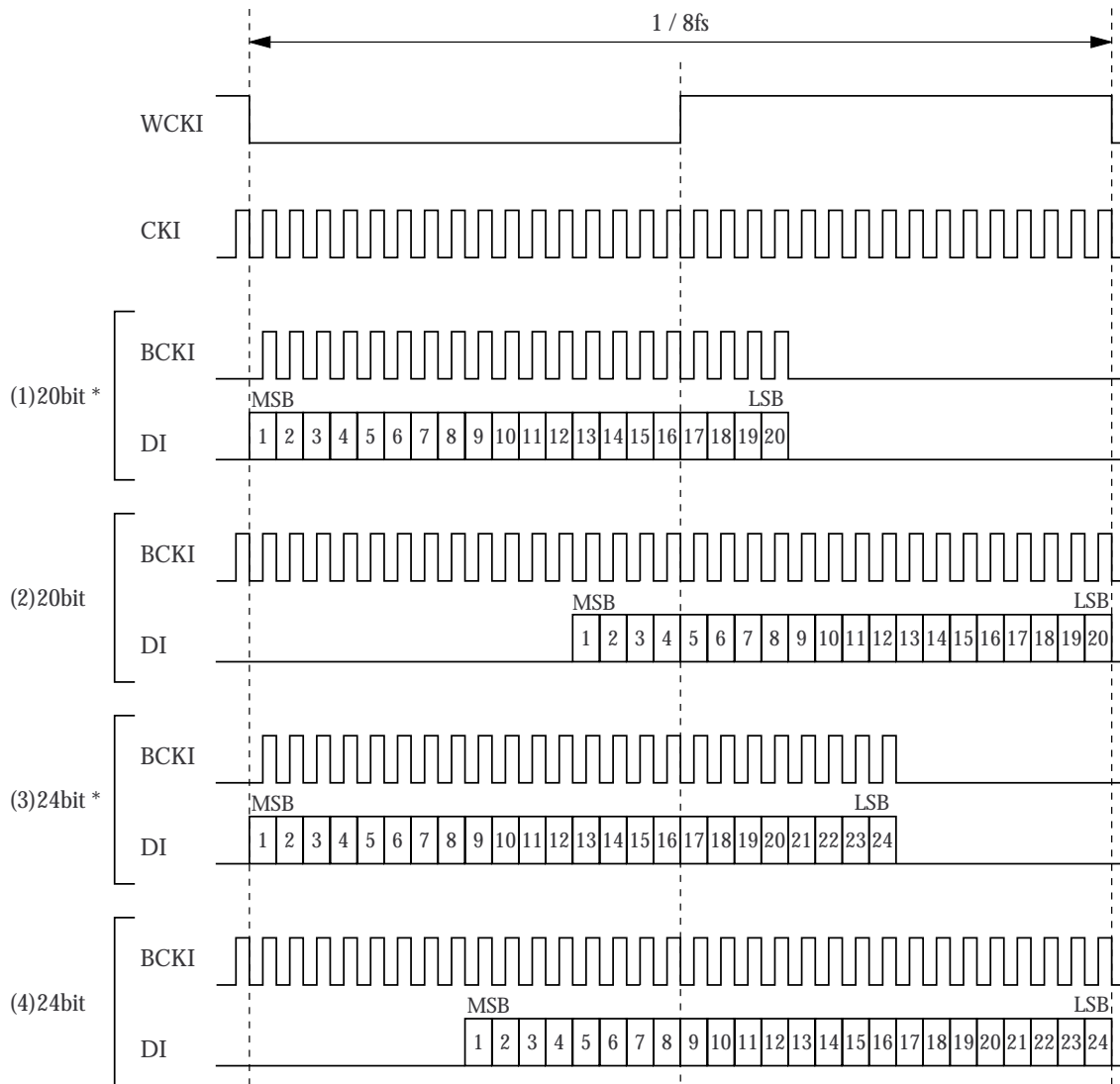
TIMING DIAGRAMS

192fs System Clock Input Timing

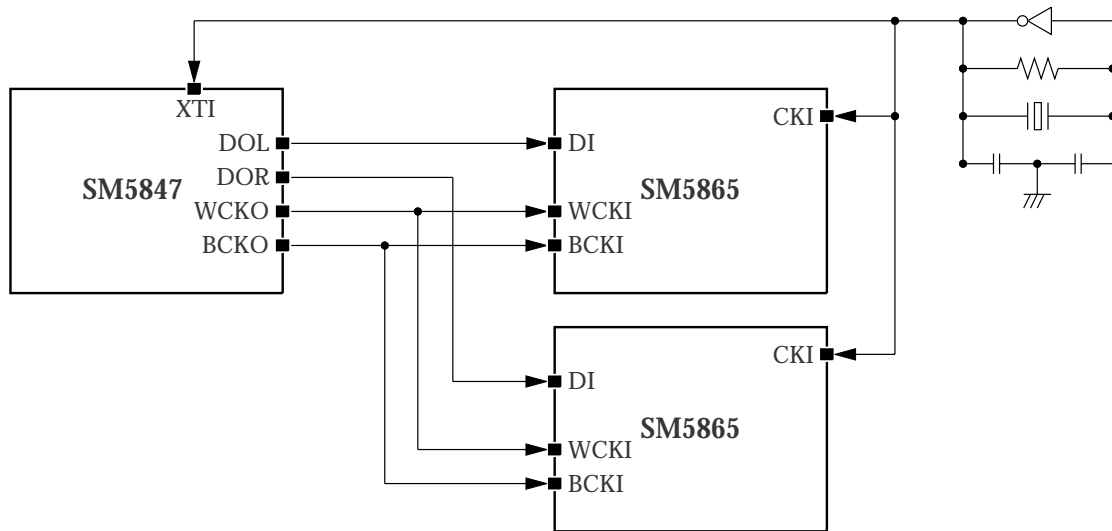


* Data can be input at any period within the word clock cycle.

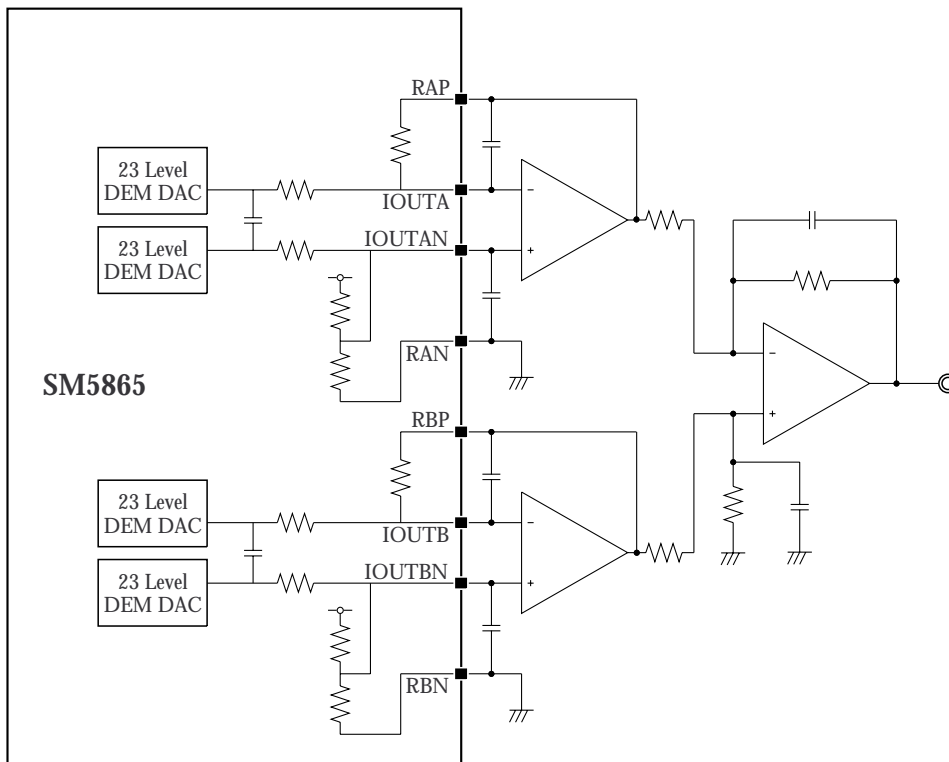
256fs System Clock Input Timing



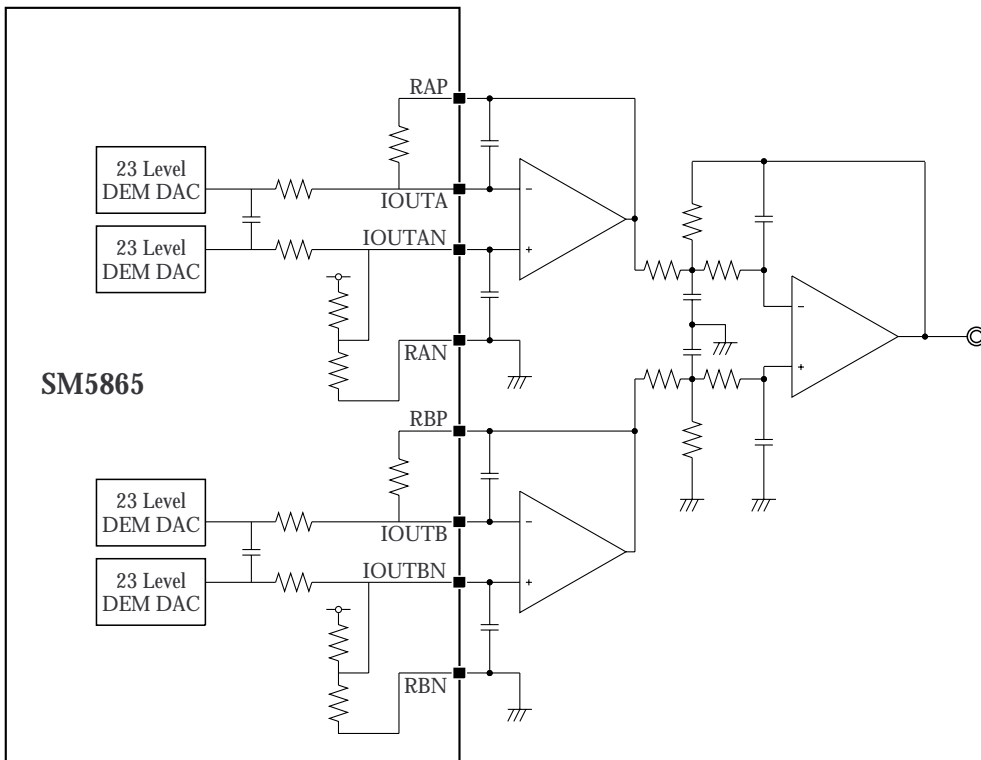
* Data can be input at any period within the word clock cycle.

TYPICAL APPLICATIONS**Input Interface Circuit**

Analog Output Circuit 1



Analog Output Circuit 2



Note that the analog output characteristics are not guaranteed for non-standard output circuit configurations.

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