

STB100NH02L

N-channel 24V - 0.0052Ω - 60A - D²PAK STripFET™ III Power MOSFET

General features

Туре	V _{DSS}	R _{DS(on)}	I _D
STB100NH02L	24V	<0.006Ω	60A ⁽¹⁾

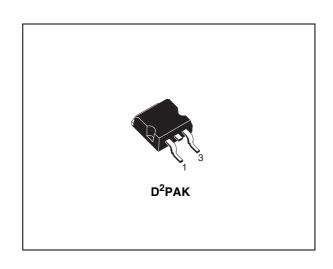
- 1. Value limited by wire bonding
- R_{DS(ON)} * Q_g industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

Description

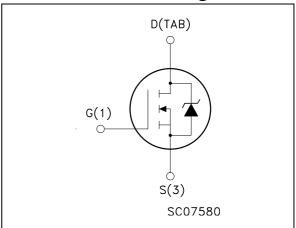
The STB100NH02L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable fot the most demanding DC-DC converter applications where high efficiency is to be achieved.

Applications

Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging	
STB100NH02LT4	B100NH02L	D ² PAK	Tape & reel	

Contents STB100NH02L

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STB100NH02L Electrical ratings

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{spike} ⁽¹⁾	Drain-source voltage rating	30	V
V _{DS}	Drain-source voltage (V _{GS} = 0)	24	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	24	V
V_{GS}	Gate- source voltage	± 20	V
I _D ⁽²⁾	Drain current (continuous) at T _C = 25°C	60	Α
I _D ⁽²⁾	Drain current (continuous) at T _C = 100°C	60	А
I _{DM} ⁽³⁾	Drain current (pulsed)	240	Α
P _{tot}	Total dissipation at T _C = 25°C	100	W
	Derating Factor	0.67	W/°C
E _{AS} (4)	Single pulse avalanche energy	600	mJ
T _{stg}	Storage temperature		
Tj	Max. operating junction temperature	-55 to 175	°C

- 1. Garanted when external Rg=4.7 Ω and $t_{\rm f}$ < tfmax.
- 2. Value limited by wire bonding
- 3. Pulse width limited by safe operating area.
- 4. Starting $T_i = 25$ °C, $I_D = 30A$, $V_{DD} = 15V$

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	1.5	°C/W
Rthj-amb	Thermal resistance junction-ambient max		°C/W
T _J	Maximum lead temperature for soldering purpose	300	°C

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Electrical characteristics STB100NH02L

2 Electrical characteristics

(T_{CASE} =25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 25mA, V _{GS} =0	24			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 20V V _{DS} = 20V, T _C = 125°C			1 10	μ Α μ Α
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1	1.8		V
R _{DS(on)}	Static drain-source on resistance	$V_{GS} = 10V, I_D = 30A$ $V_{GS} = 5V, I_D = 15A$		0.0052 0.007	0.006 0.011	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
9 _{fs} (1)	Forward transconductance	V _{DS} = 10V _, I _D = 30A		40		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 15V, f = 1MHz,$ $V_{GS} = 0$		2850 800 120		pF pF pF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 10V, I_{D} = 30A R_{G} = 4.7 Ω V_{GS} = 10V (see <i>Figure 13</i>)		13 75 50 18		ns ns ns
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 10V, I_D = 30A, V_{GS} = 10V, R_G = 4.7 Ω (see <i>Figure 14</i>)		47.5 10 7	64	nC nC nC
R_{G}	Gate input resistance	f=1 MHz gate DC Bias=0 test signal level =20 mV open drain		1		Ω

^{1.} Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current Source-drain current (pulsed)				60 240	A A
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 30A, V _{GS} = 0			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 60A$, di/dt = 100A/ μ s, $V_{DD} = 16V$, $T_{j} = 150$ °C (see <i>Figure 15</i>)		35 35 2		ns nC A

^{1.} Pulse width limited by safe operating area.

^{2.} Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %

Electrical characteristics STB100NH02L

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance

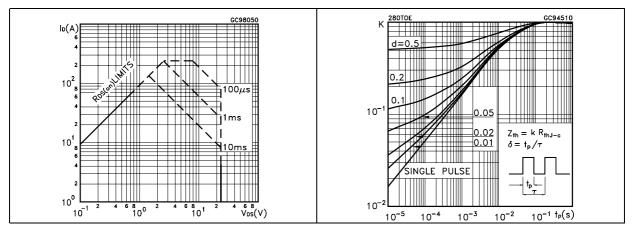


Figure 3. Output characterisics

Figure 4. Transfer characteristics

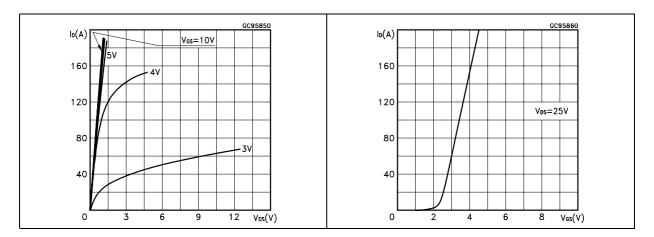
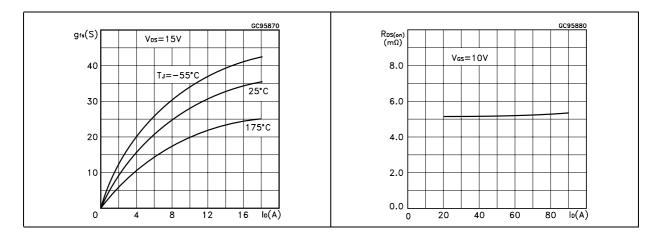


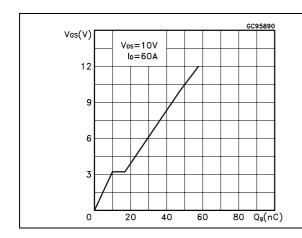
Figure 5. Transconductance

Figure 6. Static drain-source on resistance



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Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations



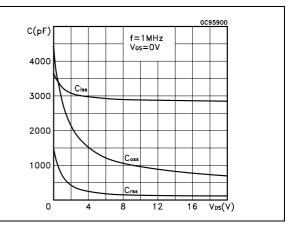
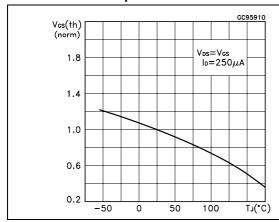


Figure 9. Normalized gate threshold voltage vs temperature

Figure 10. Normalized on resistance vs temperature



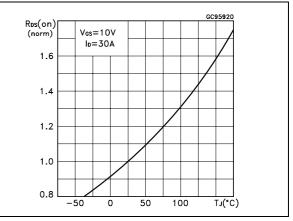
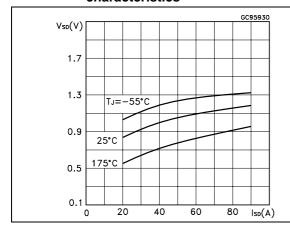
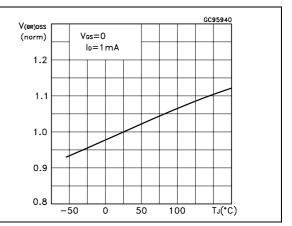


Figure 11. Source-drain diode forward characteristics

Figure 12. Normalized B_{VDSS} vs temperature





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Test circuit STB100NH02L

3 Test circuit

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

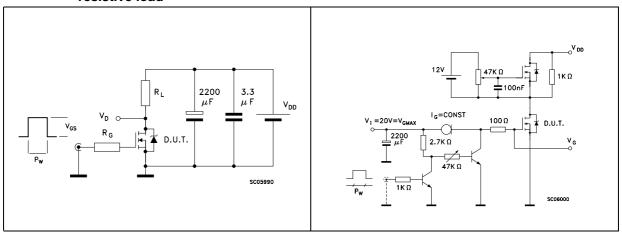


Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped Inductive load test circuit

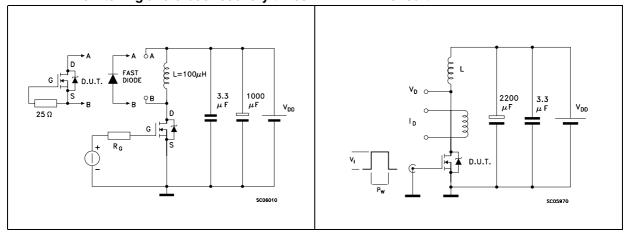
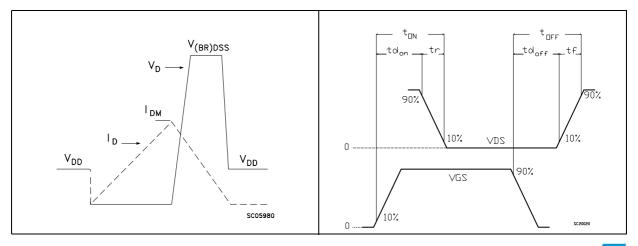


Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform



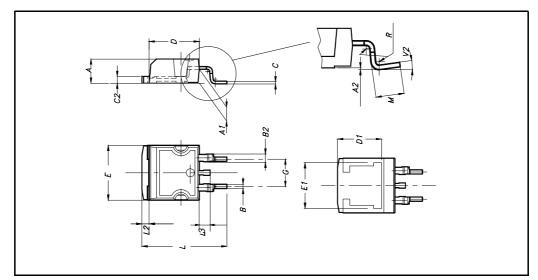
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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D²PAK MECHANICAL DATA

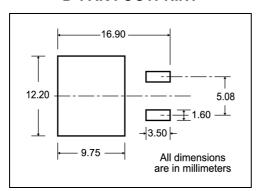
DIM.		mm.				
DIWI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
В	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
С	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
М	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0º		4º			



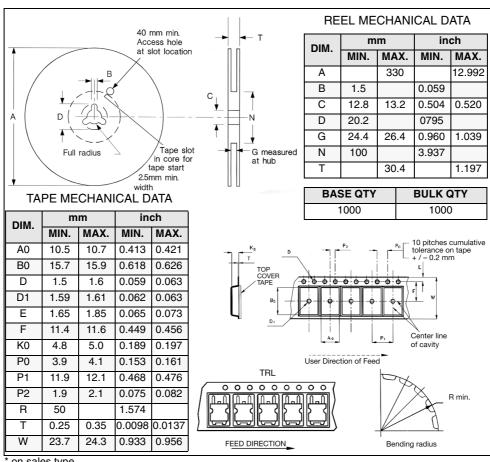
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Packaging mechanical data 5

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



Revision history STB100NH02L

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
21-Jun-2006	3	Preliminary document
12-Jun-2006	4	New template

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