



STL120NH02V

N-channel 20V - 0.0025Ω - 120A - PowerFLAT™ (6x5)
STripFET™ III Power MOSFET

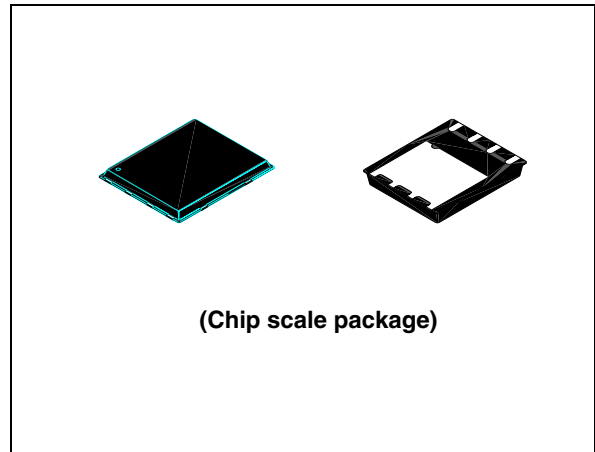
Target Specification

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STL120NH02V	20V	<0.003Ω	28A ⁽¹⁾

1. Value limited by wire bonding

- Improved die-to-footprint ratio
- Very low profile package (1mm max)
- Very low thermal resistance
- Conduction losses reduced
- 2.5V gate drive
- Switching losses reduced
- Very low threshold device



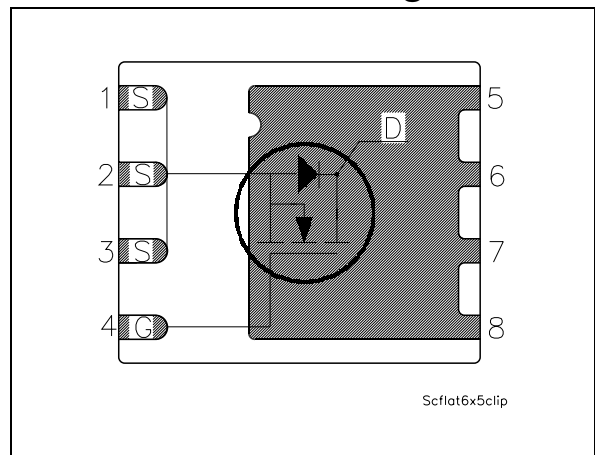
Description

The STL120NH02V utilizes the latest advanced design rules of ST's proprietary STripFET™ Technology. Thanks to a very low threshold, it is ideal for Synchronous Buck Converter in point of load brick module. The Chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STL120NH02V	L120NH02V	PowerFLAT™ (6x5)	Tape & reel

Contents

1 **Electrical ratings** 3

2 **Electrical characteristics** 4

3 **Test circuit** 6

4 **Package mechanical data** 7

5 **Revision history** 9

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	20	V
V_{GS}	Gate-source voltage	± 8	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	120	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	75	A
$I_{DM}^{(1)}$	Drain current (pulsed)	480	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	28	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25^\circ\text{C}$	100	W
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25^\circ\text{C}$	4	W
	Derating factor	0.03	W/ $^\circ\text{C}$
T_j T_{stg}	Operating junction temperature storage temperature	-55 to 175	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2. When mounted on FR-4 board of 1in², 2oz Cu. $t < 10\text{sec}$
3. The value is rated according R_{thj-C} .

Table 2. Thermal data

$R_{thj-case}$	Thermal resistance junction-case (drain) (Steady state)	1.56	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	31.2	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1in², 2oz Cu. $t < 10\text{sec}$

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	10	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	TBD	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0$	20			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}$, $T_C = 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 8\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	0.60			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 4.5\text{V}$, $I_D = 14\text{A}$ $V_{GS} = 2.5\text{V}$, $I_D = 14\text{A}$		0.0025 0.003	0.003 0.004	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 16\text{V}$, $I_D = 14\text{A}$		TBD		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		TBD TBD TBD		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 10\text{V}$, $I_D = 14\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{V}$ (see Figure 1)		TBD TBD TBD TBD		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 10\text{V}$, $I_D = 28\text{A}$, $V_{GS} = 2.5\text{V}$, $R_G = 4.7\Omega$ (see Figure 2)		33 TBD TBD	44	nC nC nC
R_G	Gate Input Resistance	$f=1\text{MHz}$ Gate DC Bias =0 Test Signal Level =20mV Open Drain		1.8		Ω

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				28 112	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 28A$, $V_{GS} = 0$			TBD	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 28A$, $di/dt = 100A/\mu s$, $V_{DD} = 16V$ (see Figure 3)		TBD TBD TBD		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 28A$, $di/dt = 100A/\mu s$, $V_{DD} = 16V$, $T_j = 150^\circ C$ (see Figure 3)		TBD TBD TBD		ns nC A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

3 Test circuit

Figure 1. Switching times test circuit for resistive load

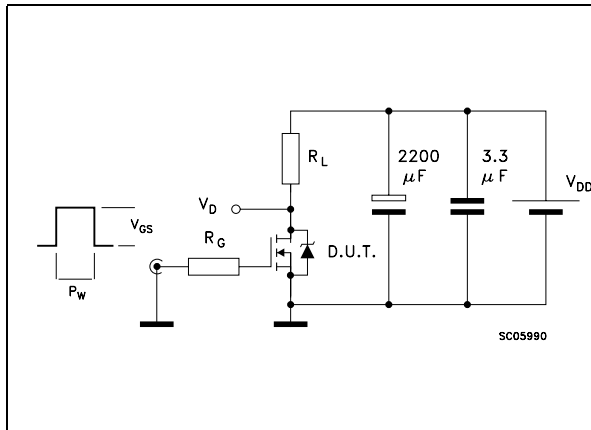


Figure 2. Gate charge test circuit

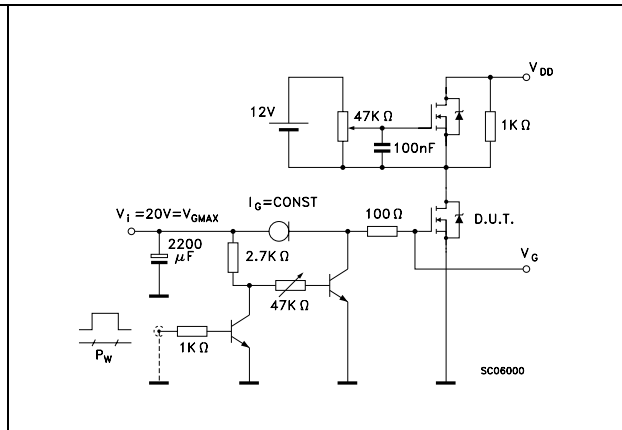


Figure 3. Test circuit for inductive load switching and diode recovery times

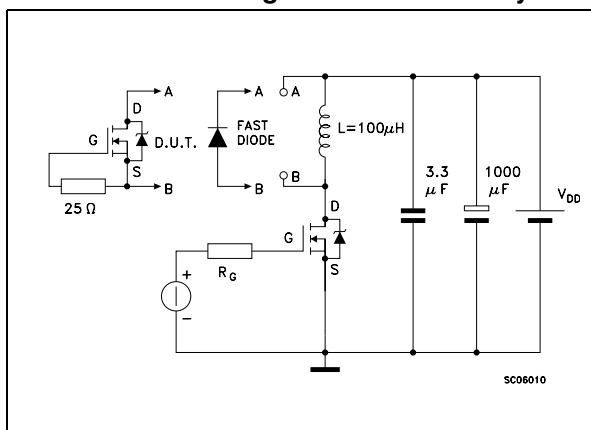


Figure 4. Unclamped Inductive load test circuit

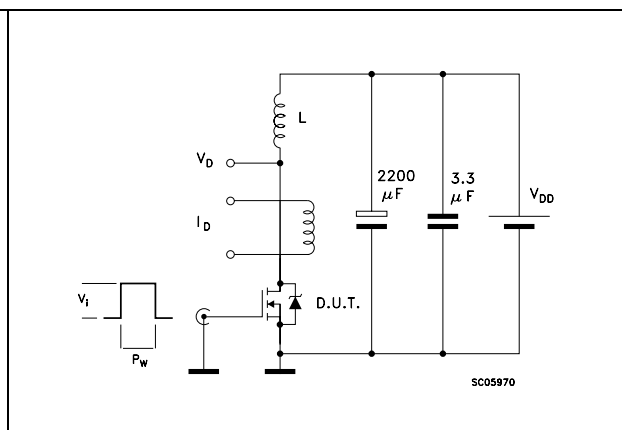


Figure 5. Unclamped inductive waveform

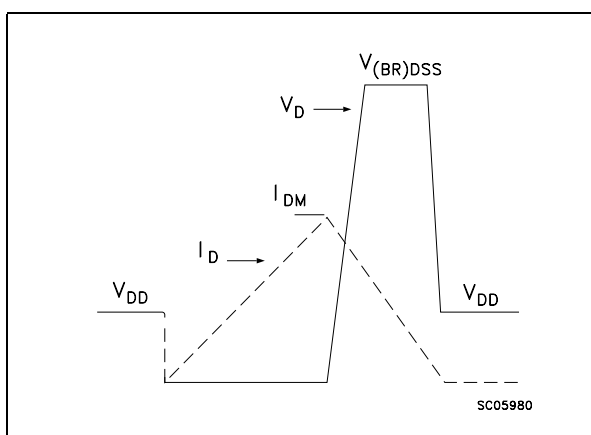
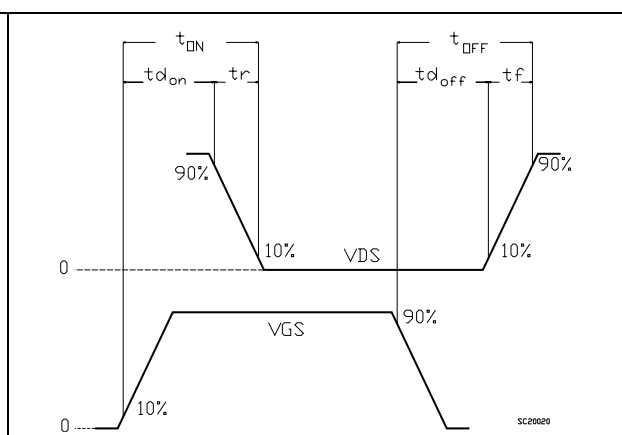


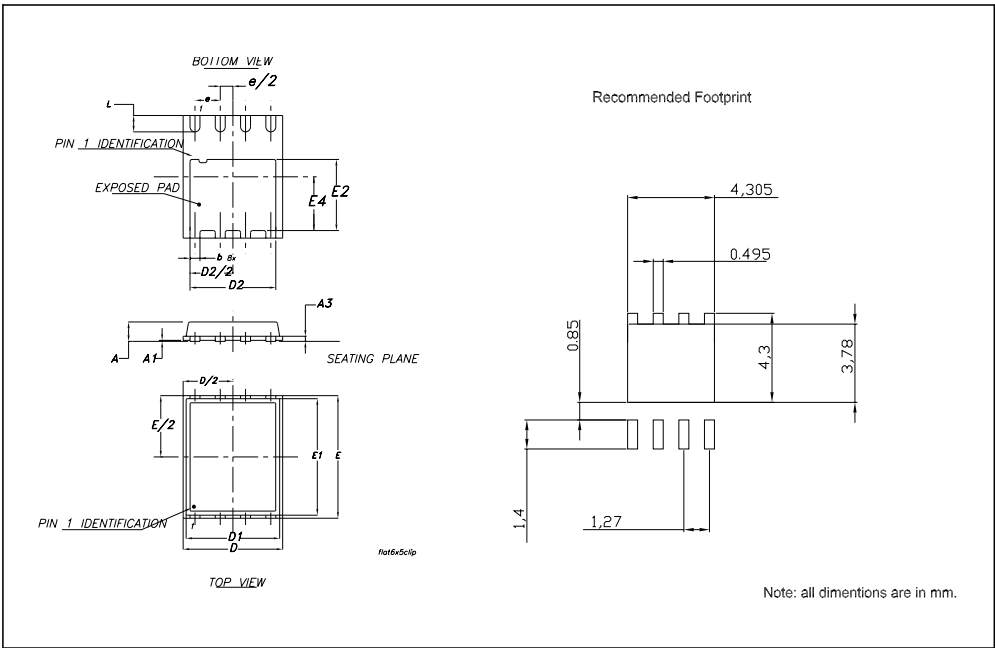
Figure 6. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

PowerFLAT™ (6x5) MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035



5 Revision history

Table 7. Revision history

Date	Revision	Changes
24-Jun-2005	1	New document
04-Sep-2006	2	New template, no content change

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