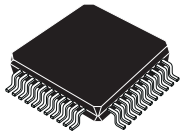
STLC30R81

INTEGRATED RINGING SLIC FOR SHORT LOOP APPLICATIONS

- MONOCHIP SLIC SUITABLE FOR SHORT LOOP APPLICATIONS
- 3.3V SUPPLY
- IMPLEMENTS ALL KEY FEATURES OF THE BORSHT FUNCTION
- DIFFERENTIAL OR SINGLE-ENDED Rx INPUTS
- INTEGRATED TRAPEZOIDAL WAVEFORM RINGING plus SINUSOIDAL and PWM WAVEFORM RINGING CAPABILITY
- TWO SELECTABLE PATH FOR SINUSOIDAL RING INJECTION
- SOFT BATTERY REVERSAL WITH PROGRAMMABLE TRANSITION TIME
- ON HOOK TRANSMISSION
- LOW POWER DISSIPATION IN ALL OPERATING MODES
- AUTOMATIC DUAL BATTERY OPERATION
- LOOP START, GROUND START FEATURES
- SURFACE MOUNT PACKAGE
- -40 TO +85°C OPERATING RANGE
- TEST FUNCTION
- NO EXTERNAL COMPONENTS FOR POWER DISSIPATION



TQFP44 (10 x 10) with slug

ORDERING NUMBER: STLC30R81

DESCRIPTION

The STLC30R81 is a low voltage SLIC suitable for short loop applications. All the BORSHT and test functions (phone detection, loop-back, short circuit detection) are integrated in this device. It provides three ringing modes: Sinusoidal, Trapezoidal and PWM waveform.

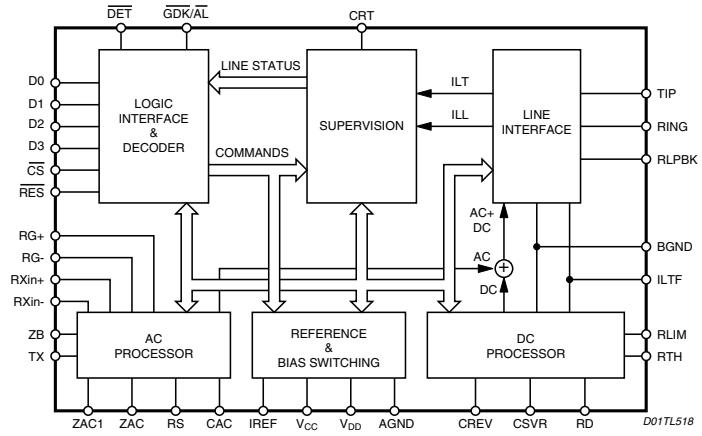
In sinusoidal ringing modes, depending on the CODEC's functionalities and characteristics Rxin+/Rxin- or Rg+/Rg- paths can be selected. When CODEC can manage low frequency signals Rxin+/ Rxin- will be used.

This device can also limit the peak current during On-Hook/Off-Hook transition and Ring-trip detection.

The device is based on BCD3S 90V technology and it can work at 3.3V power supply.

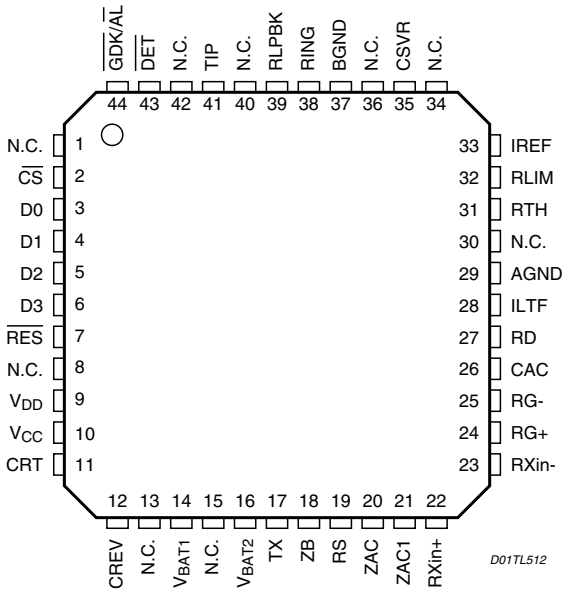
The TQFP44 Package with SLUG increases the SLIC performance in terms of power dissipation making unnecessary the use of any external power components.

BLOCK DIAGRAM



Rev. 2

PIN CONNECTION (Top view)



PIN DESCRIPTION

N°	Pin	Type	Function
1	N.C.		No Connection
2	CSI	In	Chip-Select for input control bits; active low.
3	D0	In	Control Interface input bit 0. *
4	DI	In	Control Interface input bit 1. *
5	D2	In	Control Interface input bit 2. *
6	D3	In	Control Interface input bit 3. *
7	RES	In	Reset pin active low
8	N.C.		No Connection
9	VDD	In	Control Interface Power Supply
10	VCC	In	Positive Power Supply.
11	CRT	In	GNDK detection capacitor
12	CREV	In	Reverse polarity transition time programming capacitor
13	N.C.		No Connection
14	VBAT1	In	Negative Battery Supply 1 (-38V Typ)
15	N.C.		No Connection
16	VBAT2	In	Negative Battery Supply 2 (-74V Typ)
17	TX	Out	4 wires output stage (transmitting port)
18	ZB	In	Canceling input of balance network for 2 to 4 wires conversion.
19	RS	In	Protection resistors image. It is connected between this node and ZAC
20	ZAC	In	AC impedance synthesis
21	ZAC1	In	RX buffer output / AC impedance is connected between this node and ZAC
22	Rxin+	In	4 wires input stage (receiving port). A 100K external resistor must be connected to AGND to bias the input stage
23	Rxin-	In	4 wires input stage (receiving port). A 100K external resistor must be connected to AGND to bias the input stage. If not used must be tied to ground.

PIN DESCRIPTION (continued)

N°	Pin	Type	Function
24	RG+	In	Sinusoidal ring signals input stage. A 100K external resistor must be connected to AGND to bias the input stage
25	RG-	In	Sinusoidal ring signals input stage. A 100K external resistor must be connected to AGND to bias the input stage. If not used must be tied to ground.
26	CAC	In	AC feed back input / AC-DC split capacitor is connected between this node and ILTF
27	RD	In	Ring trip threshold setting resistor
28	ILTF	In	Transversal Line Current Image
29	AGND	In	Analog Ground
30	N.C.		No Connection
31	RTH	In	Off-Hook threshold programming pin
32	RLIM	In	Limiting current programming pin
33	IREF	In	Voltage reference output to generate internal reference current
34	N.C.		No Connection.
35	CSVR	In	Battery supply filter capacitor.
36	N.C.		No Connection
37	BGND	In	Battery Ground
38	RING	Out	B wire termination output. IB is the current sunk into this pin.
39	RLPBK	In	External loop back resistor connects with this pin and tip
40	N.C.		No Connection.
41	TIP	Out	A wire termination output. IA is the current sourced from this pin.
42	N.C.		No Connection.
43	DET	Out	Off-Hook and Ring-Trip detection bit active low
44	GDK/AL	Out	Ground-key detection bit active low

* Input pins provided with 15µA sink to AGND pull-down

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{BAT}	Battery voltage	-82 +V_{CC}	V
V_{CC}	Positive supply voltage	-0.4 to +7	V
V_{DD}	Control interface Supply Voltage	-0.4 to +7	V
A/R/BGND	AGND respect BGND	-2 to +2	V

Note: 1. In case of power up, power failure or hot insertion with V_{BAT1}, V_{CC} present and V_{BAT2} floating the Absolute Maximum Rating can be exceeded. This effect can be prevented ensuring that V_{BAT2} is always present before $V_{BAT1}$and V_{CC} or connecting one schottky diode (e.g. BAT49X or equivalent between .$V_{BAT1}$and V_{BAT2}).

OPERATING RANGE

Symbol	Parameter	Value	Unit
T_{opt}	Operating temperature range	-40 to 85	°C
V_{CC}	Positive supply voltage	3.3 to 3.6	V
V_{DD}	Control interface Supply Voltage	3 to 5.5	V
V_{BAT1}	Battery voltage	-40 to –22	V
V_{BAT2}	Battery voltage	-74 to –65	V
A/BGND	AGND respect BGND	-0.3 to +0.3	V

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance Junction to Ambient (2 layer board) Typ.	32	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance Junction to Ambient (1 layer board) Typ.	56	°C/W

OPERATING MODES

It is possible to choose several operating modes just setting the proper Input D0, D1, D2, and D3. The table below (Tab.1) shows these modes:

Table 1. Ctrl Interface

Inputs				Operating Mode	Output	
D0	D1	D2	D3		DET	GDK/AL
0	0	0	0	Power down	Disable	Disable
0	0	0	1	Power down	Disable	Disable
1	1	0	1	Power down	Disable	Disable
0	0	1	0	Stand-by	Off-Hook	Gnd-Key
0	1	0	0	Active normal polarity	Off-Hook	Gnd-Key
0	1	1	0	Active reverse polarity	Off-Hook	Gnd-Key
1	0	0	0	Trapezoidal ringing normal polarity	Ringing trip	Gnd-Key
1	0	1	0	Trapezoidal ringing reverse polarity	Ringing trip	Gnd-Key
1	1	0	0	Ground start	Off-Hook	Gnd-Key
1	1	1	0	High impedance feeding	Off-Hook	Disable
0	1	0	1	Active normal polarity (On-Hook transmission)	Off-Hook	Gnd-Key
0	1	1	1	Active reverse polarity (On-Hook transmission)	Off-Hook	Gnd-Key
1	0	0	1	Ringing In Sinusoidal (or PWM) wave Rxin+/- In	Ringing trip	Gnd-Key
1	0	1	1	Ringing In Sinusoidal (or PWM) wave Rg+/- In	Ringing trip	Gnd-Key
0110⇒1110				Test mode: phone detection	Phone detect	Disable
0	0	1	1	Test mode: loop back	Off-Hook	Disable
1	1	1	1	Test mode: short circuit detection	Phone short	Disable

Power Down

It's an idle state characterized by very low power consumption; any functionality is disabled. It can be set during out of service periods just to reduce the power consumption.

It is worth remarking that two other conditions can set the SLIC in IDLE state but with some differences as reported in the table below.

Table 2. Power down

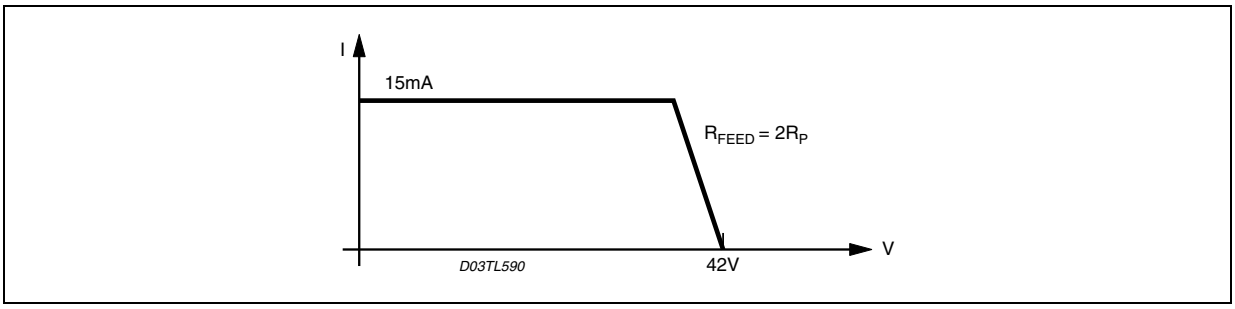
IDLE STATE	DET	GDK/AL
Power down command	Disable	Disable
Reset	Disable	Disable
Thermal alarm	Low	Low

Stand By

Mode selected in On-Hook condition when high immunity to the common mode currents is needed to prevent false Off-Hook detection. To reduce the current consumption, AC feedback loop is disabled. Only DET and

GDK/AL detectors are active. DC line loop current is limited at 15mA (not programmable). DC characteristic is shown in Fig.1. The line feeding voltage in On-Hook is typically 42V @ VBAT2 = -74V.

Figure 1. Characteristic in StBy Mode

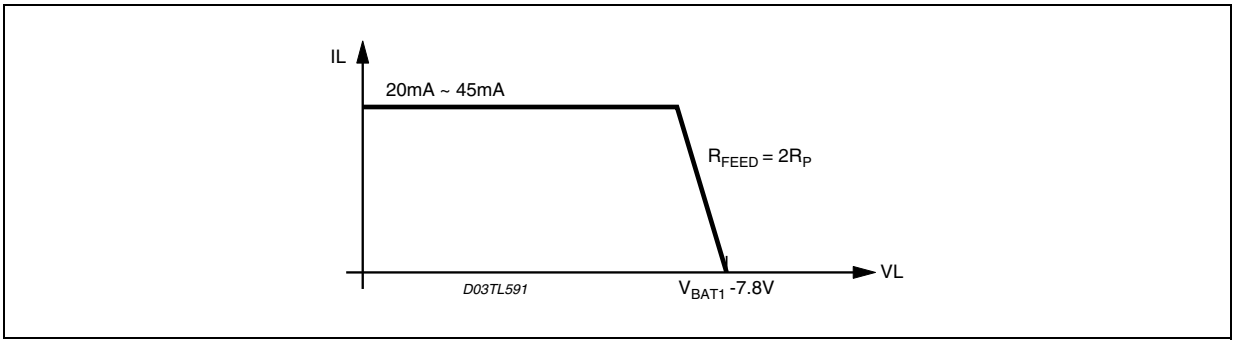


Active - NP (normal polarity) or RP (reverse polarity)

Mode selected to allow voice signal transmission. When in ACTIVE mode V_{BAT1} is selected automatically and the voltage drop in on-hook condition is 7.8V. Concerning AC characteristic the STLC30R81 allows to set 2Wire termination impedance by means of external scaled impedance.

In ACTIVE mode the SLIC can perform battery reversal in a soft way, with programmable transition time, without affecting the AC signal transmission. It is possible to program, by means of an external resistor RLIM, the value of the current limitation in a range of 20 to 45mA. During On/Off-Hook transition, the SLIC line drivers limit the transient current at Ilim +13mA.

Figure 2. DC Characteristic in Active mode



Active - ON-Hook transmission

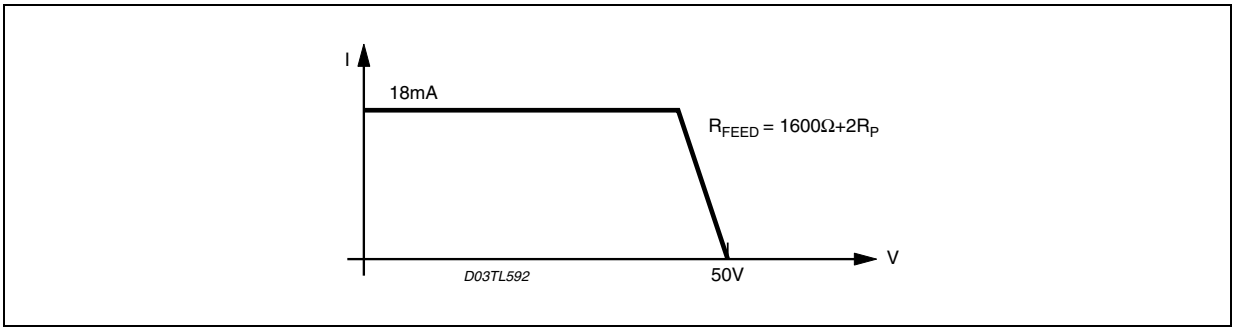
This mode is selected to allow caller ID transmission in On-Hook line condition. The line feeding voltage in On-Hook transmission is 42V @ V_{BAT2} = -74V.

High Impedance feeding

As in Stand-By, this mode is set in On-Hook condition, with further reduced power consumption. Higher power efficiency turns back to a lower immunity of the Off-Hook detector to line common mode currents. The DC feeding shows a constant current characteristic (Ilim = 18mA) followed by a resistive range with an equivalent series resistance Rfeed = 1600Ω+ 2Rp (Fig.3). The line feeding voltage in On-Hook is 50V @ V_{BAT2} = -74

Thermal protection circuit is still active, preventing the junction temperature, in case of fault condition, to exceed 150°C. In High Impedance Feeding most of the circuit is switched off, only the circuit, dedicated to Off-Hook detection, is powered. This allows reducing the total power consumption in On-hook to 30mW (typical).

Figure 3. DC Characteristic in Hi-Z Feeding



RINGING

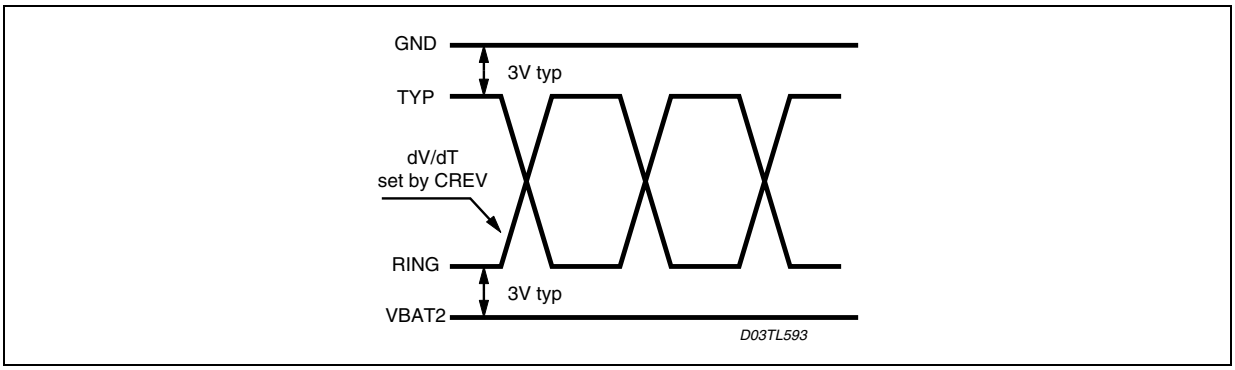
The STLC30R81 can provide three kind of signal waveform modes: Sinusoidal, trapezoidal, PWM. When this mode is selected, the SLIC is switched to VBAT2 (-74V); both DC/AC feedback loop are disabled and the SLIC line drivers operate as voltage buffers.

Trapezoidal Ringing Waveform

The ring waveform is obtained toggling the D2 control bit at the desired ring frequency. This bit in facts, controls the line polarity: 0 = direct, 1 = reverse. The transition between the two polarities is performed in a "soft" way. This means that TIP and RING wire exchange their polarities following a ramp transition (see Fig.4).

The CREV is capacitor sets the shape of the ringing trapezoidal waveform. Once ring trip is detected, the DET output is set low and remains latched keeping the STLC30R81 in Stand-by mode until the operative mode is modified by any Input Word.

Figure 4. Typical Ringing Waveform



CREV	Crest Factor @ 20Hz	Crest Factor @ 25Hz
22nF	1.2	1.26
27nF	1.25	1.32
33nF	1.33	Not significant (*)

* Distortion already less than 10%

Sinusoidal Ringing Waveform

The STLC30R81 has two couple of inputs: Rxin+/Rxin- and Rg+/Rg-; this means that it is possible to select two different paths to generate the sinusoidal waveform ringing.

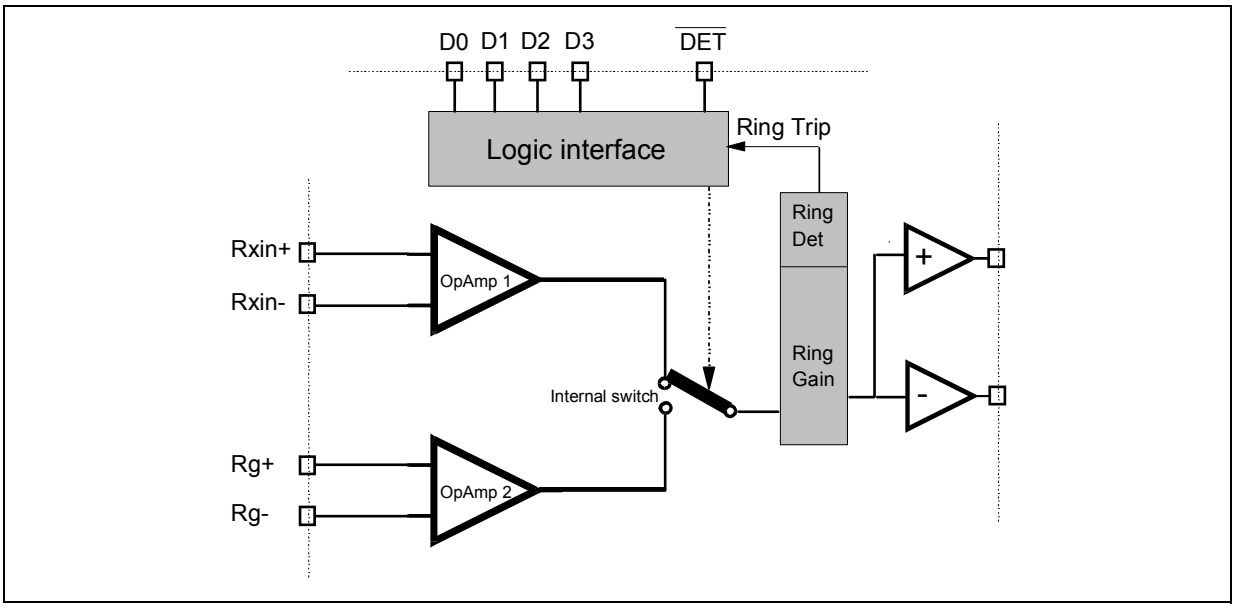
– Selecting Rxin+/Rxin- (first path), the sinusoidal waveform can be applied in differential mode (using both inputs) or single ended mode (connecting one of the two input pins directly to the GND). This signal comes from STLC5048 or other Codec
– Selecting Rg+/Rg- (second path), the sinusoidal (or PWM) waveform ringing, can be applied in differential mode (using both inputs) or single ended mode (connecting one of the two input pins directly to the GND). The ring source (codec, waveform generators) can be always active and shared by multiple lines.

Both DC/AC feedback loops are disabled except for the first path (Rxin+/Rxin-) that remains enabled. This functionality will be managed through an "Input Word" that allows the ringing signal, to flow through the line. The Table 3 shows how to select the proper input word.

Table 3. Control Word

Control Word				Input Selected Mode
D0	D1	D2	D3	
1	0	0	1	Rxin+/ Rxin- Input selected
1	0	1	1	Rg+/Rg- Input selected

Figure 5. Ringing internal block



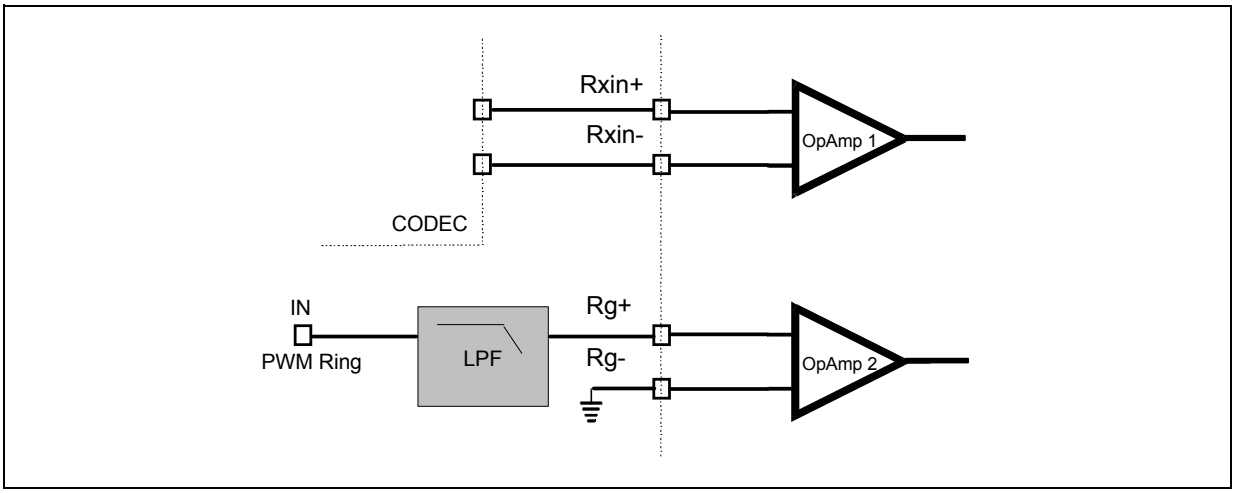
In On-Hook condition, Tip and Ring are biased at -VBAT2/2; the input signal is typically amplified at 35dB.

Ring trip detection is performed sensing the variation of the AC line impedance from High (On-Hook) to Low (Off-Hook). This particular ring trip method, allows to operate without DC offset superimposed on the ring signal and therefore, obtain the maximum possible load driving capability, from a given negative battery. After Ring/ Trip detection, DET pin is set Low and remains latched keeping the STLC30R81 in Stand-by mode until the operative mode is modified by Input Word.

PWM Ringing Waveform

A pulse-width modulated (PWM) signal may be used to provide the ringing input to Rg inputs. The signal is applied through a low-pass filter and AC-coupled into Rg+. This approach gives a sine wave output at tip and ringing circuit.

Figure 6. PWM signal Input vs Sinusoidal Output



GROUND START

This mode is selected when the SLIC is adopted in a system using the Ground Start feature.
In this mode, the TIP termination is set in High Impedance (100KΩ) while the RING one is active and fixed at -33V @ Vbat1 (= -38V). In case RING termination is connected to GND the sinked current is limited to 35mA.

When RING is connected to GND both Off-Hook and Ground-Key detectors are set low.

TEST MODES

This device can provide three kind of tests:

1. Phone Detection
2. Short circuit
3. Loop back

Phone Detection

This test feature checks whether a phone is connected to the line.

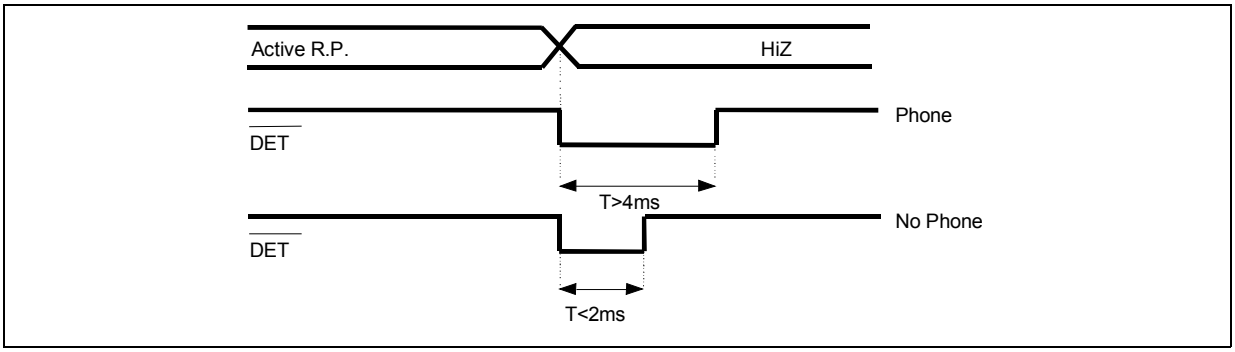
Starting from Active Reverse Polarity status, just changing the D0 input bit, it is possible to perform the Phone Detection function.

The MCU measures the time span of DET. Time longer then 4ms indicates that a phone is hooked up with the line, if no phone is connected, the time span is less than 2ms.

Table 4. Phone detection - D0 variation

Control Word				Operating Mode
D0	D1	D2	D3	
0	1	1	0	Active - Reverse Polarity
1	1	1	0	High Impedance Feeding - Normal Polarity

Figure 7. Phone detection Diagram



Short Circuit

DET signal pin changes its logical level depending on the presence (or not) of short circuit at the output of the Line Card (See Tab.5).

Table 5. Short Circuit Detection

Control Word				DET	
D0	**D1**	**D2**	**D3**	Short Circuit	No Short Circuit
1	1	1	1	0	1

Loop back

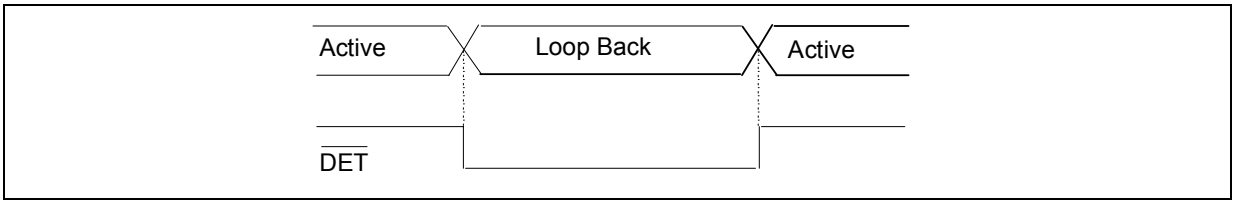
The test is aimed at cheking detection and feeding circuitry functionalities as described in fig. 8. The external resistor RLPCK is closed internally between TIP and RING and emulates the phone resistance. Starting from ACTIVE mode, when loop back mode is selected DET pin will change its level.

If DET pin is low it means that detection and feeding circuits work properly. If DET remains high it means that a failure has been detected.

Table 6. Loop Back Detection

Control Word				DET	
D0	**D1**	**D2**	**D3**	Good	Fail
0	0	1	1	0	1

Figure 8. loop back detection diagram



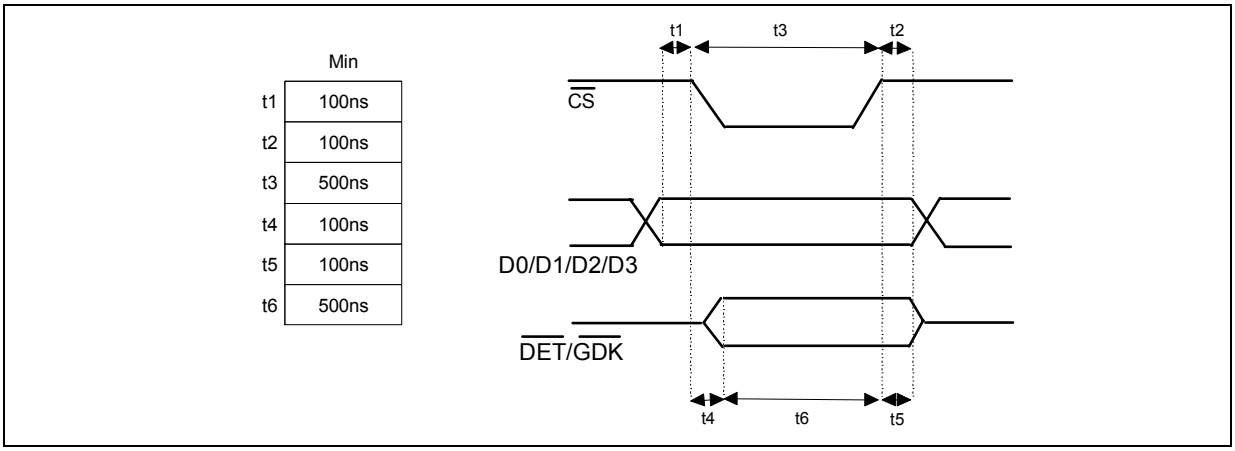
Protection Mode

Suggested protection circuit is based on programmable LCP1521S Trisil and the surge current is limited by the resistors R_{PT2} and R_{PR2}, which are PTC types, protecting the device against both lightning and power-cross.

Thermal overload: the integrated thermal protection is activated when T_j reaches 150°C typ.; the Slic is forced in Power-down mode, DET and AL are set Low.

For external applications, two diodes 1N4148 are suggested (Pls. see application diagram).

Figure 9. Logic interface Input Timing



EXTERNAL COMPONENTS

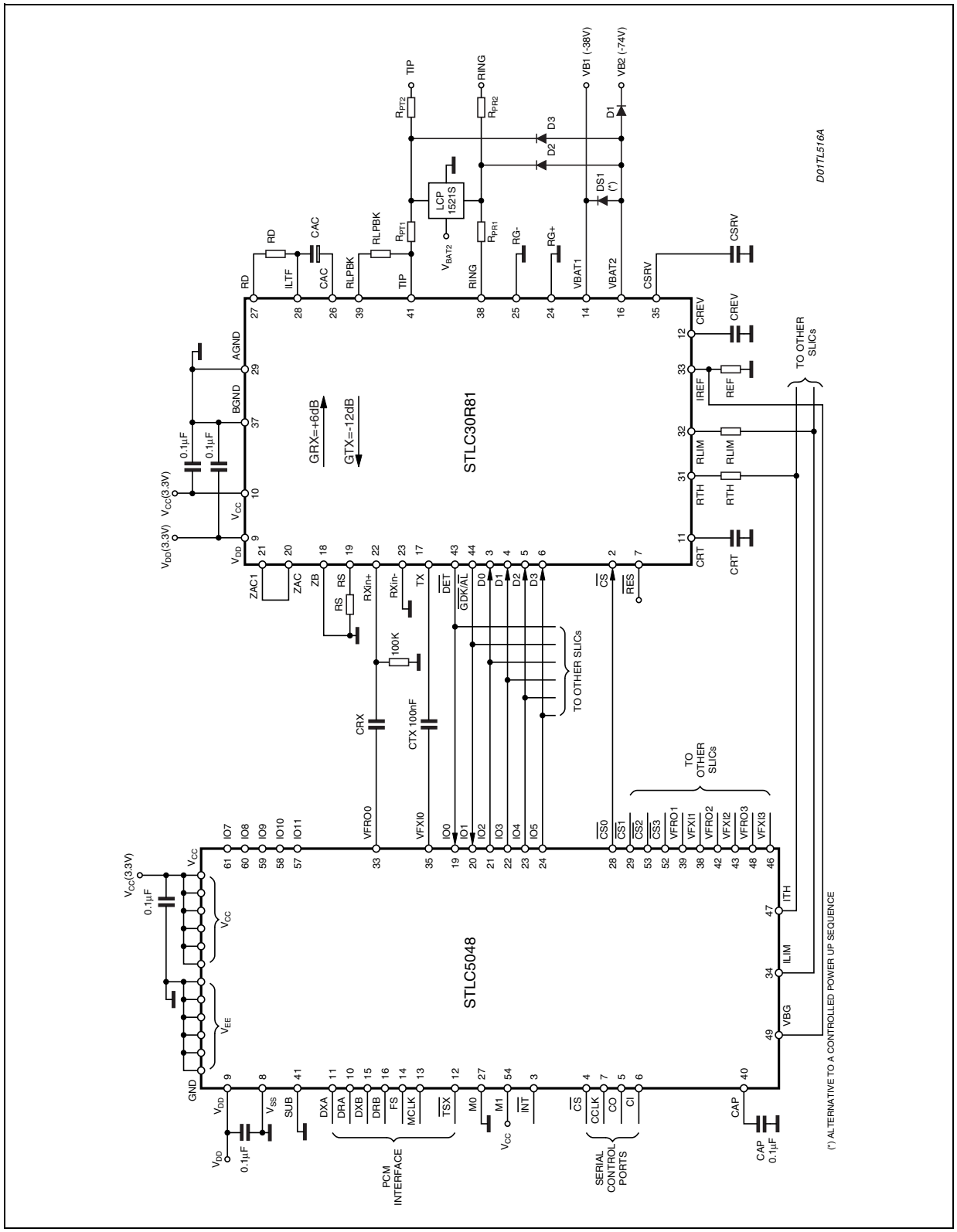
Table 7. External Components

Name	Function	Formula	Typ. Value
R_{REF}	Internal current programming resistor	$I_{REF} = 0.6/R_{REF}$	30.1KΩ±1%
C_{SVR}	Battery ripple rejection capacitance	CSVR = $1/(2\pi \cdot f_P \cdot 1.3M\Omega)$	100nF ±10% 100V @ 1.22Hz
C_{VCC}	Power supply filter		100nF±20%
C_{VB1}	Battery supply filter		100nF±20% 100V
C_{VB2}	Battery supply filter		100nF±20% 100V
RD	Ring Trip threshold setting resistor	$RD=100/I_{RT}$(*); 2KΩ<RD<5KΩ	4.12KΩ±1% @I_{RTH} =24mA
C_{RT}	Ground Key capacitance	C_{RT} = (25/Fring) · 470nF	470nF±20% 6V @25Hz
C_{AC}	AC/DC splitter Capacitance	$C_{AC} = 1/(2\pi \cdot fsp/R_D)$	10µF ±20% 15V @$f$sp = 10Hz
R_S	Protection resistor image	$Rs = 25*2R_P$	2.5KΩ±1%
ZAC	2 Wire AC impedance	$Z_{AC} = 25[Z_S-2R_P]$	12.5KΩ±1%
ZA	SLIC impedance balancing network	$ZA= 25 \cdot Z_S$	15KΩ±1%
ZB	Line impedance balancing network	$ZB = 25 \cdot Z_L$	15KΩ±1%
C_{COMP}	AC feedback compensation Capacitance	$C_{COMP} = 2 / (2\pi \cdot f_o \cdot 100 \cdot R_P])$	220pF ±20% @ f_o = 250KHz
RPT1	Line series Resistor	≥30	30Ω - 1/4W±1%
RPT2	Line series Resistor	≥15Ω	20Ω
RPR1	Line series Resistor	≥30	30Ω - 1/4W±1%
RPR2	Line series Resistor	≥15Ω	20Ω
R_{LIM}	Current limiting setting resistor	$R_{LIM} = 10^3 \cdot (0.6)/I_{LIM}$	26KΩ±1%
R_{TH}*	OFF/HOOK detection threshold setting resistor	$R_{TH} = 200 \cdot [(0.6)/I_{TH}]$ 23.7KΩ to 86.6KΩ	26.1KΩ±1%
C_{REV}	Polarity/reversal/transition time programming	$C_{REV} = K/(\Delta V_{TR}/\Delta T)$; K= 1/3750	47nF for 5.67V/ms
CH	Trans-Hybrid Freq. Comp Cap	CH=Ccomp	220pF ±20%
LCP15xx			
R_{LPCK}	Loop Back resistor		500Ω 1.5W ±20%
D1	Over voltage protection		1N4148
D2	Over voltage protection		1N4148
D3	Over voltage protection		1N4148
DS1 (**)	Power Up sequencer		BAT 49X

(*) $I_{RT} \leq I_{LIM}$+10mA. The line drivers have output current limitation correspond to I_{LIM} during the Ringing mode.
(**) Alternative to a controlled power up sequence

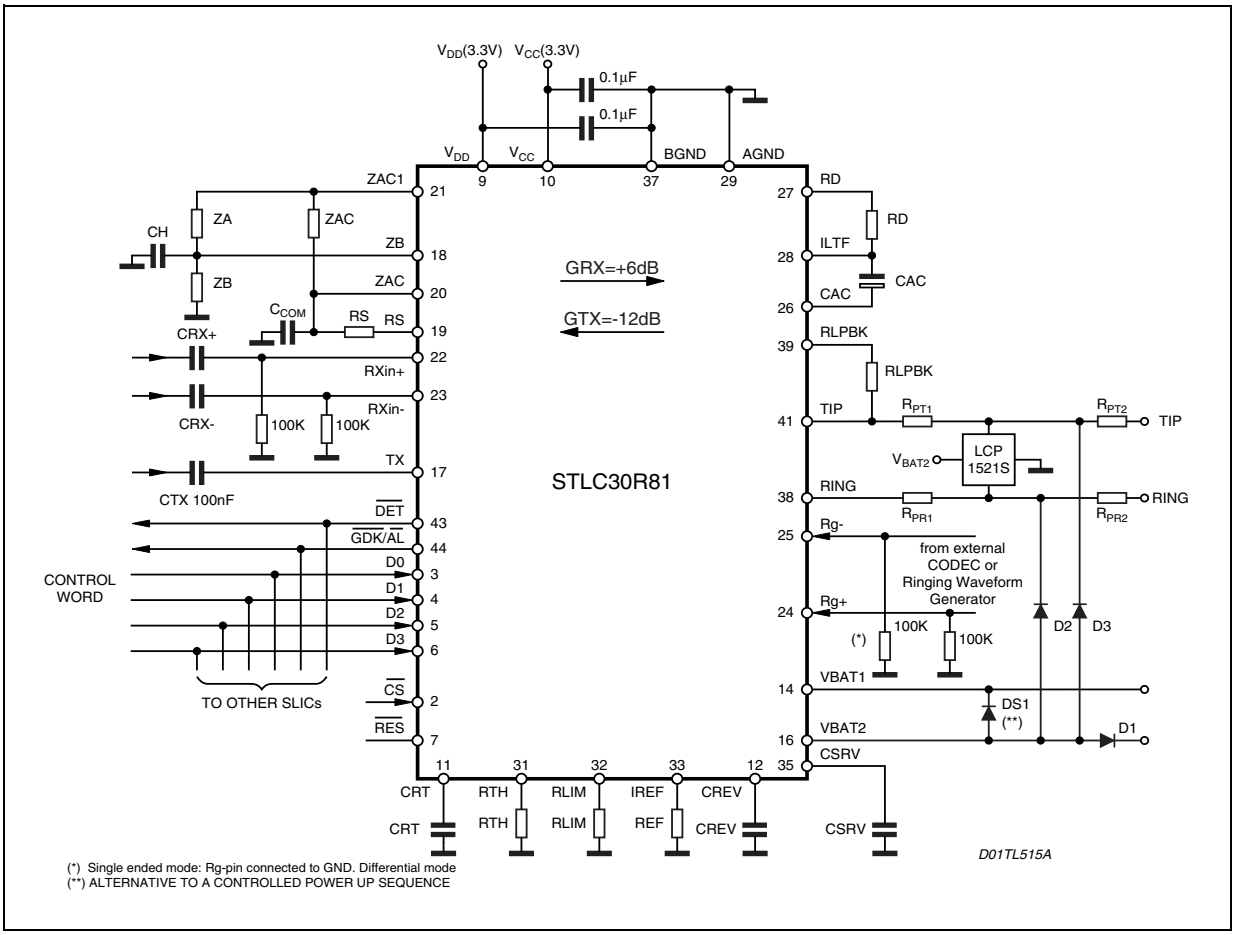
STLC5048 plus STLC30R81: Application Diagram

Figure 10. STLC5048 / STLC30R81 Application Diagram. (Single Ended Configuration)



STLC30R81 plus external generic CODEC or Ringing Waveform Generator

Figure 11. STLC30R81 plus Generic Ringing Source - Application Diagram



ELECTRICAL CHARACTERISTICS

The limits listed below are guaranteed with the specified test condition and in the 0 to 70°C temperature range. Performance over -40 to +85°C range are guaranteed by product characterization.

(Test condition, unless otherwise specified: V_{CC} and V_{DD} = 3.3V, $VBAT_1$=-38V, $VBAT_2$=-74V, T_{amb}=25°C)

AC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_{il}	Long Impedance	Each Wire			40	Ω
I_{il}	Long Current Capability AC	H.I feeding / wire (On-Hook)		5		mApk
		Standby		13		mApk
		Active per wire Ilim=current limited in active mode (see also Rlim) I_T = transversal current(*)		Ilim+ 13-I_T		mApk
L/T	Long. To Transv.	With normal Rp value @ f = 1KHz	60			dB
T/L	Transv. To Long.		40			dB
2wRL	2W return loss	300 to 3400Hz	22			dB

AC CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
THL	Trans-hybrid loss	1020Hz; 20Log $\|V_{RX}/V_{TX}\|$	30			dB
O_{VI}	2W overload level	Active Mode at line terminals on Ref. impedance	3.2			dBm
G24	Transmit gain abs	0dBm 1020Hz	-11.95	-12.11	-12.25	dB
G42	Receive gains abs.	0dBm 1020Hz	5.75	5.90	6.05	dB
G24fq	Tx gain variation vs frequency	Rel. 1020Hz, 0dBm 300 to 3400Hz	-0.1		0.1	dB
G42fq	Rx gain variation vs frequency		-0.1		0.1	dB
V2wp	Idle channel noise at line terminals	Psophometric, Active on-Hook		-82	-78	dBmp
V4wp	Idle channel noise at TX port	Psophometric, Active On Hook		-90	-84	dBmp
T_{hd}	Total harm. Dist. 2w-4w, 4w-2w	0dBm, 1KHz, I_l = 20 to 45mA			-50	dB

DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{loih}	Line voltage	I_l = 0, H.I. feeding	48	50.1	52	V
V_{lo}	Line voltage	I_l = 0, Stby	40	42	44	V
V_{lo}	Line voltage	Active On-Hook TX	28	29.5	31	V
I_{lims}	Short circuit current	R_{loop} = 0, STby		15	18	mA
I_{limb}	Short circuit current	R_{loop} = 0, H.I.feeding		18	22	mA
I_{lima}	Lim. current accuracy	Rel to progr. Val. 20 to 45mA Active NP, RP	-10		10	%
V_{IREF}	Band GAP reference		0.56	0.60	0.64	V
$R_{feed\ H.I.}$	Feeding resistance	H.I. feeding	1100	1600	2100	Ω
I_{TIP}	Tip leakage current	Ground Start			100	µA
I_{GS}	Ring lead current	Ground Start Ring to GND	25	35	45	mA
TX_{off}	TX output offset	Active Mode	-200		200	mV

DETECTORS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{det}	Off-Hook current threshold Stby, Active	Rel. to progr. Val. 6 to 11mA Active, NP, RP	-10		+10	%
		Rel. to progr. val. 3 to 6mA	-10		+20	%
$I_{det\ H.I.}$	Off-Hook current thershold	H.I. feeding	5		8	mA
Hys	Off/On Hook Hyst.	Stby Active	10%	20% I_{det}	30%	mA
T_d	Dialling distortion	Active	-1		+1	ms
I_{LL}	Ground Key current	TIP and RING to GND or Ring to GND		-9.4		mA
I_{gst}	Ground Start detection threshold $I_{LL}=I_B-I_A$	I_{gst} = 2 x I_{det}	-5		+5	%
I_{RTA}	Rintrip detection threshold Accuracy		-15		+15	%

DIGITAL INTERFACE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Inputs: D0, D1, D2, D3, CSIN						
V_{ih}	Input high voltage	V_{DD} = 3.3V	2			V
V_{il}	Input low voltage	V_{DD} = 3.3V			0.8	V
I_{ih}	Input High current				30	µA
I_{il}	Input low current				10	µA
Outputs: DET, GDK/AL						
V_{oh}	Input high voltage	I_{ol} = 0.1mA; CS = low	2			V
V_{ol}	Input low voltage	V_{DD} = 3.3V			0.5	V

Note: All digital inputs are TTL compatible

POWER SUPPLY REJECTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
PSRRC	V_{CC} to 2W port	V_{ripple} = 0.1 Vrms 50 to 4KHz	27			dB
PSRRB	V_{BAT} to 2W port	V_{ripple} = 0.1 Vrms 50 to 4KHz	30			dB

POWER CONSUMPTION

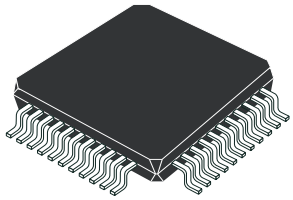
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CC}	V_{CC}	H.I. feeding On-Hook (Open Line)			1.0	mA
		Stby On-Hook			3.5	mA
		Active On-Hook			6.0	mA
		Power Down			1.0	mA
		On-Hook Tx			6.0	mA
I_{BAT1}	V_{BAT1} supply current	H.I. feeding On-Hook (Open Line)			100	µA
		Stby On-Hook			200	µA
		Active On-Hook			5.0	mA
		Power Down			100	µA
		On-Hook Tx			3.0	µA
I_{BAT2}	V_{BAT2} supply current	H.I. feeding On-Hook (Open Line)			0.5	mA
		Stby On-Hook			2.5	mA
		Active On-Hook			0.5	mA
		Power Down			0.5	µA
I_{DD}	V_{DD} supply current	Any operating mode			300	µA

SINUSOIDAL RING

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Line Offset	No Signal	-3		+3	V
	Gain	From Rx and Rg input Both differential and Single Ended	33	35	37	dB
	THD	Vin 1Vpp / 1 REN		3	5	%

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.30	0.37	0.45	0.012	0.014	0.018
c	0.09		0.20	0.003		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
e		0.80			0.031	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
H		5.89			0.232	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
S	6.00			0.236		
S1	6.00			0.236		
K	0° (min.), 3.5° (typ.), 7°(max.)					
ccc			0.10			0.004

OUTLINE AND MECHANICAL DATA



TQFP44 (10x10x1.40mm)
with Slug Down

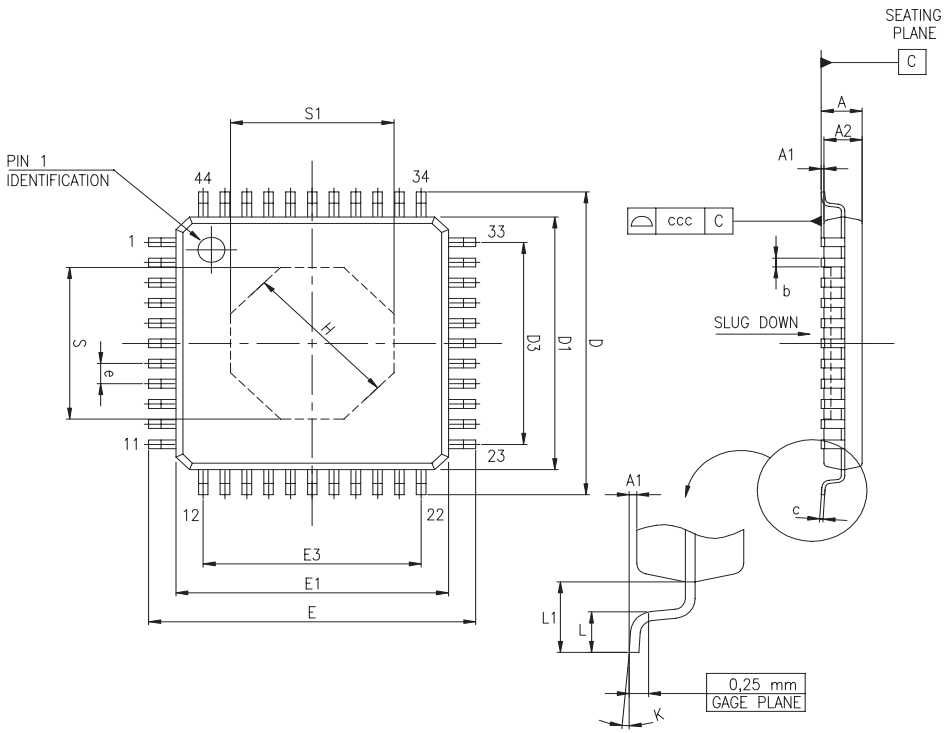


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Table 8. Revision History

Date	Revision	Description of Changes
July 2003	1	First Issue
January 2006	2	Modified Table 7 (RPR2 and RPT2 formula) and the Figures 10 and 11.