

## Description

- High speed switching application.
- Analog switch application.

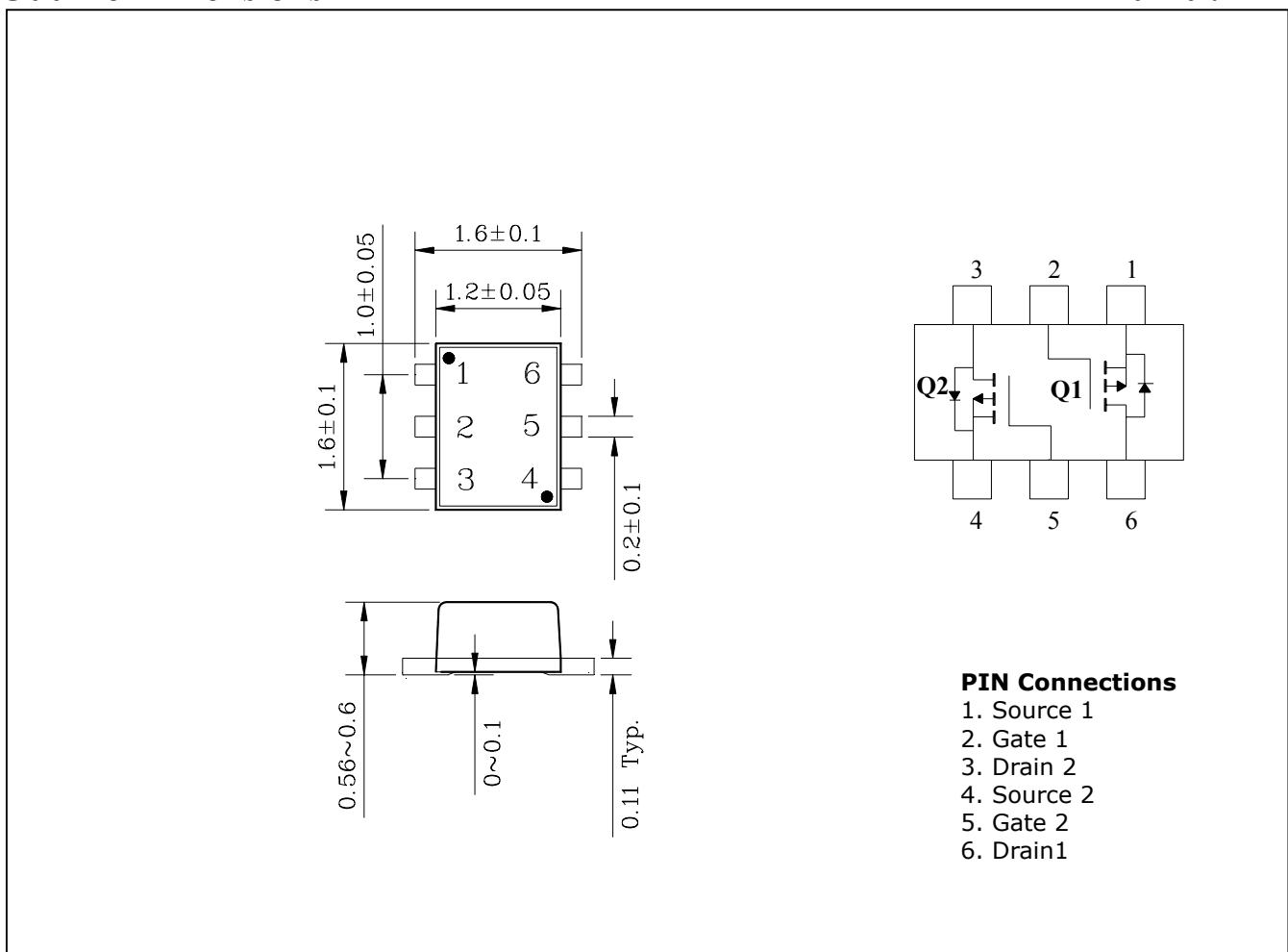
## Features

- Low threshold voltage
- Two STJ828 Chips in SOT-563F Package.

## Ordering Information

Type NO.	Marking	Package Code
SUF620EF	X	SOT-563F

## Outline Dimensions

**unit : mm**


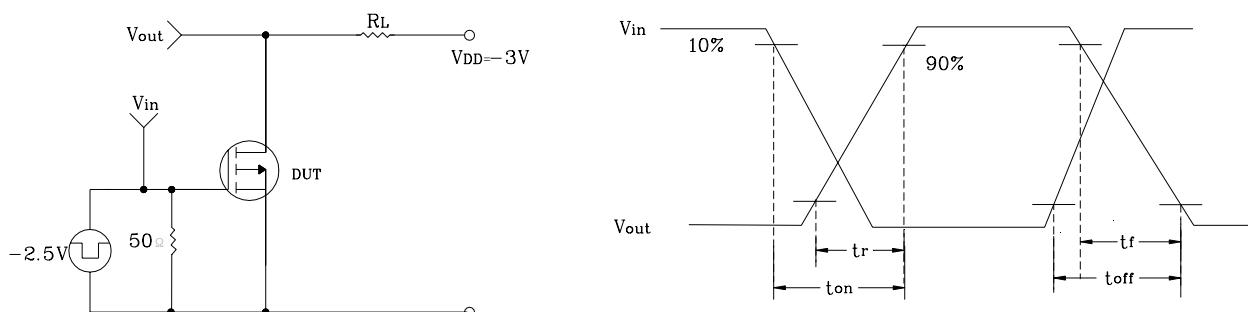
## Absolute maximum ratings (Q1,Q2 Common) (Ta=25°C)

Characteristic	Symbol	Ratings	Unit
Drain-Source voltage	V <sub>DS</sub>	-20	V
Gate-Source voltage	V <sub>GSS</sub>	±7	V
DC Drain current	I <sub>D</sub>	-50	mA
Drain Power dissipation	P <sub>D</sub>	100	mW
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature range	T <sub>stg</sub>	-55~150	°C

## Electrical Characteristics (Q1,Q2 Common) (Ta=25°C)

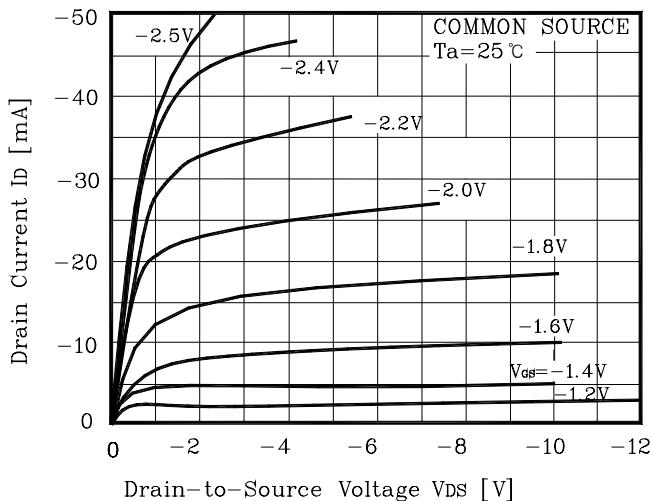
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-Source breakdown voltage	BV <sub>DSS</sub>	I <sub>D</sub> =-100μA, V <sub>GS</sub> =0	-20			V
Gate-Threshold voltage	V <sub>th</sub>	I <sub>D</sub> =-0.1mA, V <sub>DS</sub> =-3V	-0.5		-1.5	V
Drain cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0			-1	μA
Gate leakage current	I <sub>GSS</sub>	V <sub>GS</sub> =±7V, V <sub>DS</sub> =0			±1	μA
Drain-Source on-resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-10mA			40	Ω
Forward transfer admittance	Y <sub>fs</sub>	V <sub>DS</sub> =-3V, I <sub>D</sub> =-10mA	15			mS
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-3V, V <sub>GS</sub> =0, f=1MHz		10.4		pF
Output capacitance	C <sub>oss</sub>	V <sub>DS</sub> =-3V, V <sub>GS</sub> =0, f=1MHz		8.4		pF
Reverse Transfer capacitance	C <sub>rss</sub>	V <sub>DS</sub> =-3V, V <sub>GS</sub> =0, f=1MHz		2.8		pF
Turn-on time	t <sub>ON</sub>	V <sub>DD</sub> =-3V, I <sub>D</sub> =-10mA V <sub>GEN</sub> =0~ -2.5V		0.15		μs
Turn-off time	t <sub>OFF</sub>	V <sub>DD</sub> =-3V, I <sub>D</sub> =-10mA V <sub>GEN</sub> =0~ -2.5V		0.13		μs

\*. Switching Time Test Circuit

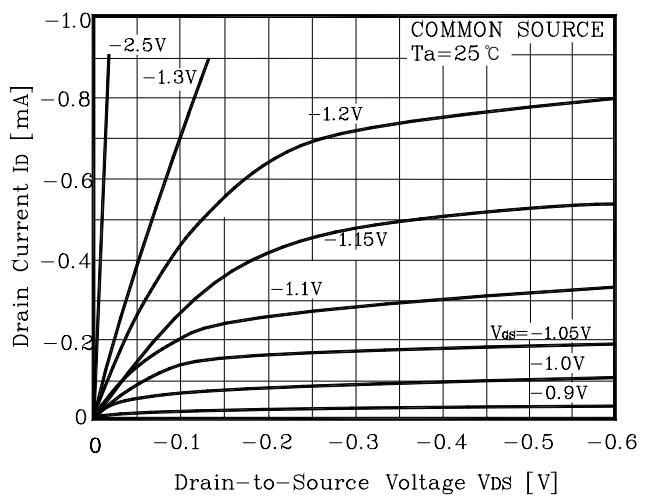


## Electrical Characteristic Curves

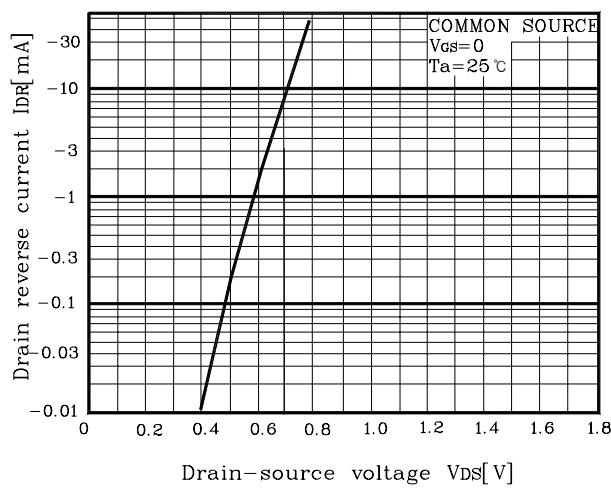
**Fig1 Id - VDS**



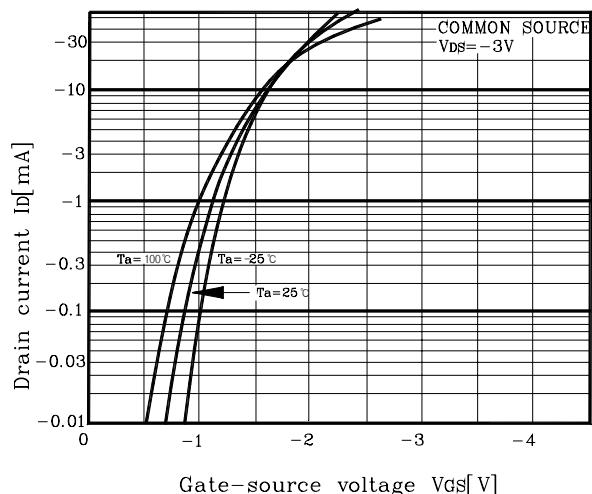
**Fig2 Id - VDS**



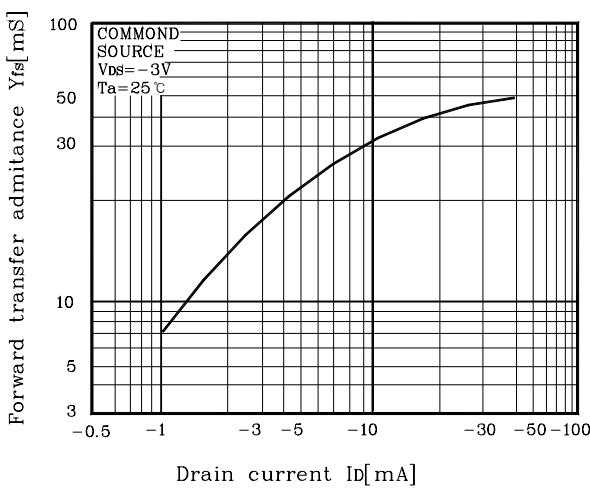
**Fig3 IDR - VDS**



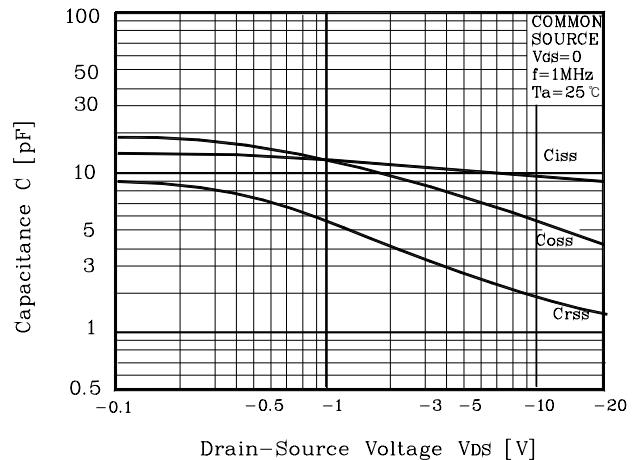
**Fig4 Id - VGS**



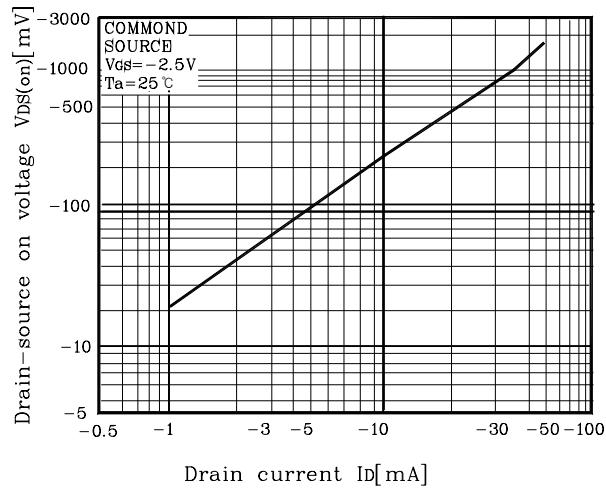
**Fig5  $|Y_{fs}|$  - Id**



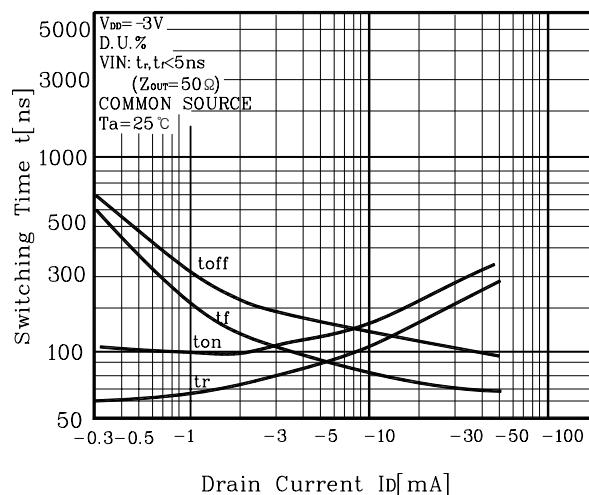
**Fig6 C - VDS**



**Fig7 VDS(on) - ID**



**Fig8 t - ID**



**Fig9 PD - Ta**

